Realtek
RTL8721F Datasheet

This document provides features and information on RTL8721F microcontroller.

Rev. 0.5.1

July, 2025

Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

©2024 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

DISCLAIMER

Please Read Carefully:
Realtek Semiconductor Corp., (Realtek) reserves the right to make corrections, enhancements, improvements and other changes to its products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

Reproduction of significant portions in Realtek data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Realtek is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions.

Buyers and others who are developing systems that incorporate Realtek products (collectively, “Customers”) understand and agree that Customers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Customers have full and exclusive responsibility to assure the safety of Customers' applications and compliance of their applications (and of all Realtek products used in or for Customers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Customer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Customer agrees that prior to using or distributing any applications that include Realtek products, Customer will thoroughly test such applications and the functionality of such Realtek products as used in such applications.

Realtek’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation kits, (collectively, “Resources”) are intended to assist designers who are developing applications that incorporate Realtek products; by downloading, accessing or using Realtek’s Resources in any way, Customer (individually or, if Customer is acting on behalf of a company, Customer’s company) agrees to use any particular Realtek Resources solely for this purpose and subject to the terms of this Notice.

Realtek’s provision of Realtek Resources does not expand or otherwise alter Realtek’s applicable published warranties or warranty disclaimers for Realtek’s products, and no additional obligations or liabilities arise from Realtek providing such Realtek Resources. Realtek reserves the right to make corrections, enhancements, improvements and other changes to its Realtek Resources. Realtek has not conducted any testing other than that specifically described in the published documentation for a particular Realtek Resource.

Customer is authorized to use, copy and modify any individual Realtek Resource only in connection with the development of applications that include the Realtek product(s) identified in such Realtek Resource. No other license, express or implied, by estoppel or otherwise to any other Realtek intellectual property right, and no license to any technology or intellectual property right of Realtek or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Realtek products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of Realtek Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from Realtek under the patents or other Realtek’s intellectual property.

Realtek’s Resources are provided “as is” and with all faults. Realtek disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any epidemic failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights.

Realtek shall not be liable for and shall not defend or indemnify Customer against any claim, including but not limited to any infringement claim that related to or is based on any combination of products even if described in Realtek Resources or otherwise. In no event shall Realtek be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of Realtek’s Resources or use thereof, and regardless of whether Realtek has been advised of the possibility of such damages. Realtek is not responsible for any failure to meet such industry standard requirements.

Where Realtek specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Customers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any Realtek products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death. Such equipment includes, without limitation, all medical devices identified by the U.S.FDA as Class III devices and equivalent classifications outside the U.S.

Customers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Customers’ own risk. Customers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Customer will fully indemnify Realtek and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s

non-compliance with the terms and provisions of this Notice.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the engineer's reference and provides detailed development information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

All information provided in this document is subject to legal disclaimers.

© REALTEK 2025. All rights reserved.

Contents

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Conventions

The following abbreviations apply to indicate the MCUs of Realtek.

Real-M300 (KM4)	Arm® Cortex®-M55 compatible instruction set core based on Armv8.1-M architecture, running at a frequency of up to 334MHz.
AP	Application Processor, designed for user application.
NP	Network Processor, designed for network protocol, provides network and power management services to AP.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

1 General Description

The RTL8721F is a low-power single-chip microcontroller integrating dual RISC cores (Arm® Cortex®-M55 compatible instruction set). The microcontroller is designed for optimized power efficiency, RF performance, and low-power consumption. It encompasses all the characteristics of low-power chip, including fine-grained clock gating, multiple power modes, and dynamic power scaling.

The RTL8721F integrates two Real-M300 (or KM4 thereafter) processors: KM4TZ and KM4NS.

- KM4TZ: KM4 with TrustZone-M security technology, usually works as Application Processor (AP)
- KM4NS: KM4 without TrustZone-M security technology, usually works as Network Processor (NP)

The KM4 is a 3-staged pipelined 32-bit processor that bases on Armv8.1-M architecture supporting Cortex-M55 compatible instruction set, running at a frequency of up to 334MHz. It offers system enhancements such as low power consumption, enhanced debug features, TrustZone-M security for hardware-enforced isolation, and a high level of support block integration.

The RTL8721F is a dual-band (2.4GHz and 5GHz) communication controller that integrates the specifications of Wi-Fi (Wi-Fi 6) and Bluetooth (Bluetooth 5.0). It supports 802.11 a/b/g/n/ac/ax wireless LAN (WLAN) network with 20MHz bandwidth. It consists of WLAN MAC, a 1T1R capable WLAN baseband, RF, and Bluetooth, providing complete Wi-Fi and Bluetooth functionalities.

A variety of peripheral interfaces, including UART, SPI, I2C, A2C (compatible with ISO 11898-1, CAN Specification 2.0), etc., as well as sensor controllers (such as ADC, Cap-Touch, and thermal) are integrated into RTL8721F devices. High-speed connectivity interfaces, SDIO and USB, are also provided. Besides, the RTL8721F has audio features with a dedicated digital microphone (DMIC) interface and I2S. Abundant general-purpose I/O (GPIOs) can be configured to different functions according to different IoT (Internet of Things) applications flexibly. The user-friendly development kits (SDK and HDK) are provided to customers for developing applications.

The RTL8721F also incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash controller provides a flexible and efficient way to access Flash (e.g., byte and block access). A multilayer AXI bus interconnect supports internal and external memory access.

The RTL8721F family offers devices in three different packages ranging from 48 pins to 100 pins. The included peripherals changes with the device.

All information provided in this document is subject to legal disclaimers.

© REALTEK 2025. All rights reserved.

2 Features

Item	Features
Number of Cores	2
KM4TZ	● Arm Cortex-M55 compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 334MHz ● TrustZone-M security technology ● Memory Protection Unit (MPU) with up to 8 regions with non-secure state and 4 regions with secure state ● Built-in Nested Vectored Interrupt Controller (NVIC) ● SWD with 4 instruction breakpoints and 1 data watchpoint
KM4NS	● Arm Cortex-M55 compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 334MHz ● Memory Protection Unit (MPU) with up to 8 regions with non-secure state ● Built-in Nested Vectored Interrupt Controller (NVIC) ● SWD with 4 instruction breakpoints and 1 data watchpoint
Memory Supported	● On-chip SRAM ● PSARM (optional) ● NOR Flash (optional)
Security	● Secure boot ● Arm TrustZone-M ● AES/SHA engine ● ECC/RSA Engine ● Whole or partial Flash decryption ● Secure JTAG/SWD ● 2K bytes OTP ● True Random Number Generator (TRNG)
WLAN Controller	● Full compliance with IEEE and Wi-Fi Alliance (WFA) Wi-Fi 6 specifications ● CMOS MAC, Baseband PHY, and RF in a single chip for 802.11a/b/g/n/ac/ax compatible WLAN ● Complete 802.11ax solution at 2.4GHz/5GHz ● 114.7Mbps of data rate using 20MHz bandwidth for 802.11ax ● Backward compatible with 802.11b/g/n devices while operating in 802.11ax mode
WLAN MAC	● Frame aggregation for increased MAC efficiency (A-MPDU) ● Low latency immediate Block Acknowledgement (BA) ● PHY-level spoofing to enhance legacy compatibility ● Power saving mechanism ● Supports Target Wake Time (TWT) function for power saving ● Channel management and co-existence ● Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth ● Supports Enhanced Distribution Channel Access (EDCA) and MU EDCA ● Supports for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges ● Supports 2 Network Allocation Vector (NAV) ● Supports Basic Service Set (BSS) color ● Supports Time Synchronization Function (TSF) auto-sync ● IEEE 802.11i (WPA, WPA2, WPA3), open, shared key, and pair-wise key authentication services ● Rx trigger frame (except GCR MU-BAR and NFRP) ● Supports AP/STA/Concurrent mode (802.11ax AP not supported) ● Supports Multi Channel Concurrent (MCC) mode by software TDMA ● Supports Neighbor Awareness Networking (NAN) ● Supports Wi-Fi Tunnel (WTN) ● Supports Wi-Fi-based Audio TSFT Sync ● Supports Wake-On-WLAN via Magic Packet and Wake-up frame ● Transmitting beamforming as beamformee ● Support group key update
WLAN PHY	● Integrated 2.4GHz/5GHz PA and LNA, and T/R switch ● Integrated 2.4GHz/5GHz balun ● Supports both internal and external PA ● Adjustable transmitting power

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

	● Supports Channel State Info (CSI) ● Supports Dynamic Frequency Selection (DFS) ● Supports Tx Low-density Parity Check (LDPC), Tx Binary Convolutional Code (BCC), and Rx BCC ● Supports Rx STBC 2x1 ● Supports SU/MU beamformee report ● Supports Rx DL-OFDMA, Tx UL-OFDMA ● Support 802.11ax Dual Carrier Modulation (DCM)/ER Tx/Rx ● Supports Spatial Reuse to maximize parallel transmissions ● Short guard interval ● Supports digital pre-distortion to enhance PA performance ● Smoothing for channel estimation ● Antenna diversity
Bluetooth Baseband	● Compliant with Bluetooth Core Specification including LE-1M/LE-2M/LE-Coded (Long Range) ● Fast AGC control to improve receiving dynamic range ● Supports serial Flash for firmware storage and parameter upgrade ● Supports channel map update to dynamically detect channel quality to improve transmission quality
Bluetooth Controller	● Bluetooth Low Energy 5.4 certified (featured with BLE 5.0) ● Integrated MCU to execute Bluetooth protocol stack ● LE advertising extensions ● Supports piconets in a scatter-net ● Enhanced Bluetooth/WLAN Co-existence Control to improve transmission quality in different profiles ● Supports multiple Low Energy states
RF	● Antenna diversity ● Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna
Display	● RGB interface: 6-/16-bit RGB565, 8-/24-bit RGB888 ● MCU interface: 8-/16-bit RGB565, 8-/24-bit RGB888 ● PPE: pixel format conversion, image geometric transformation, multi-layer image blending, and rotation ● MJPEG: including a JPEG decoder and a post-processing unit
Serial Communication	● SPI x 2 ● I2C x 2 ● I2C-like ● UART x 5 ● IR ● USB (Host/Slave) ● SDIO Host ● SDIO Slave ● A2C x 2, compatible with ISO 11898-1 (CAN Specification 2.0) ● Ethernet MAC ● I2S x 1
VDD Input	2.97V ~ 3.63V
Package	● QFN48, 6mm x 6mm, 0.4mm pitch ● QFN68, 8mm x 8mm, 0.4mm pitch ● QFN100, 10mm x 10mm, 0.35mm pitch

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

3 System Applications

With integrated WLAN and Bluetooth, wide range of solutions can be deployed in various fields, such as:

- Smart home
  - Lighting (dimming) control, switch and plugs
  - Home and kitchen appliances
- Industrial 4.0
- Low-power IoT
  - Smart door lock
  - Low-power Wi-Fi camera
- Smart docking and monitor
- Health-care devices
- Wearables
- Portable devices
- Gaming accessories
- Wireless audio
- New energy field

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

4 Functional Block Diagram

The functional block diagram is shown in *Figure 4-1*. This diagram provides a view of the chip's major functional components and core complexes.

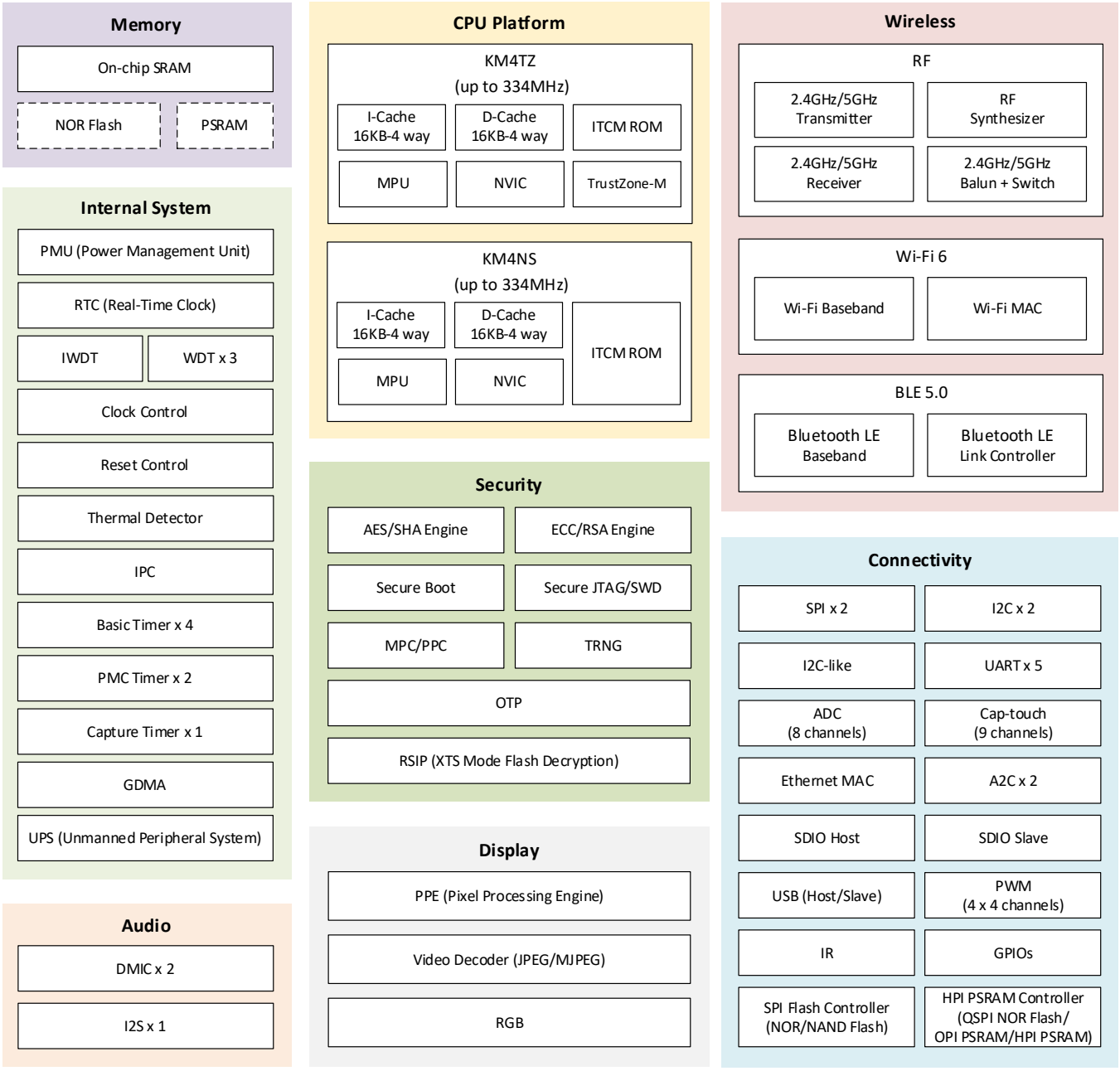


Figure 4-1 Block diagram

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

5 Pin Assignments

5.1 QFN48

5.1.1 RTL8721FAF

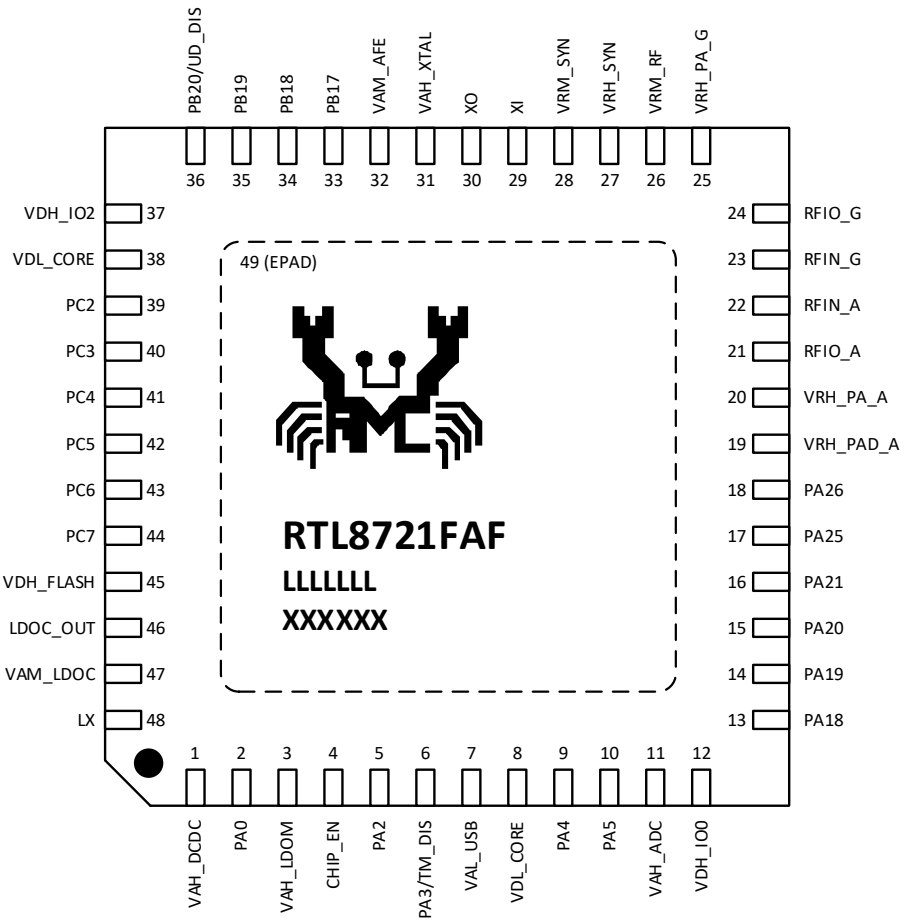


Figure 5-1 RTL8721FAF series pinout

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

5.1.2 RTL8721FAM

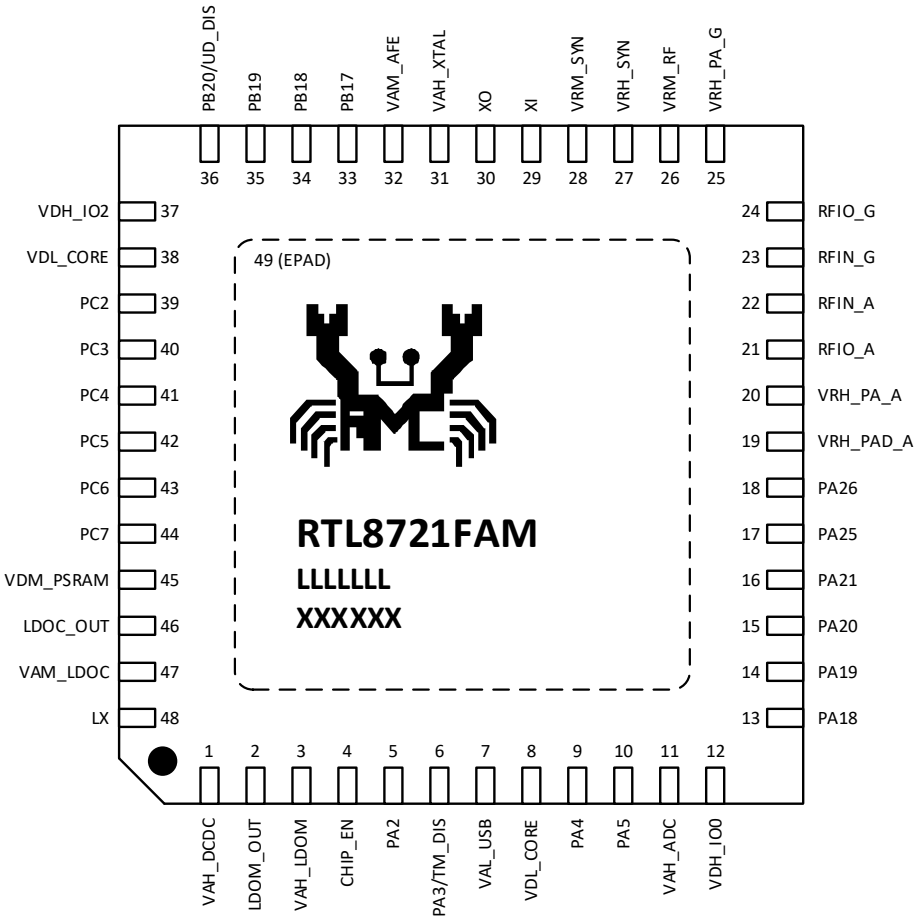


Figure 5-2 RTL8721FAM series pinout

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

5.2 QFN68

5.2.1 RTL8721FCM

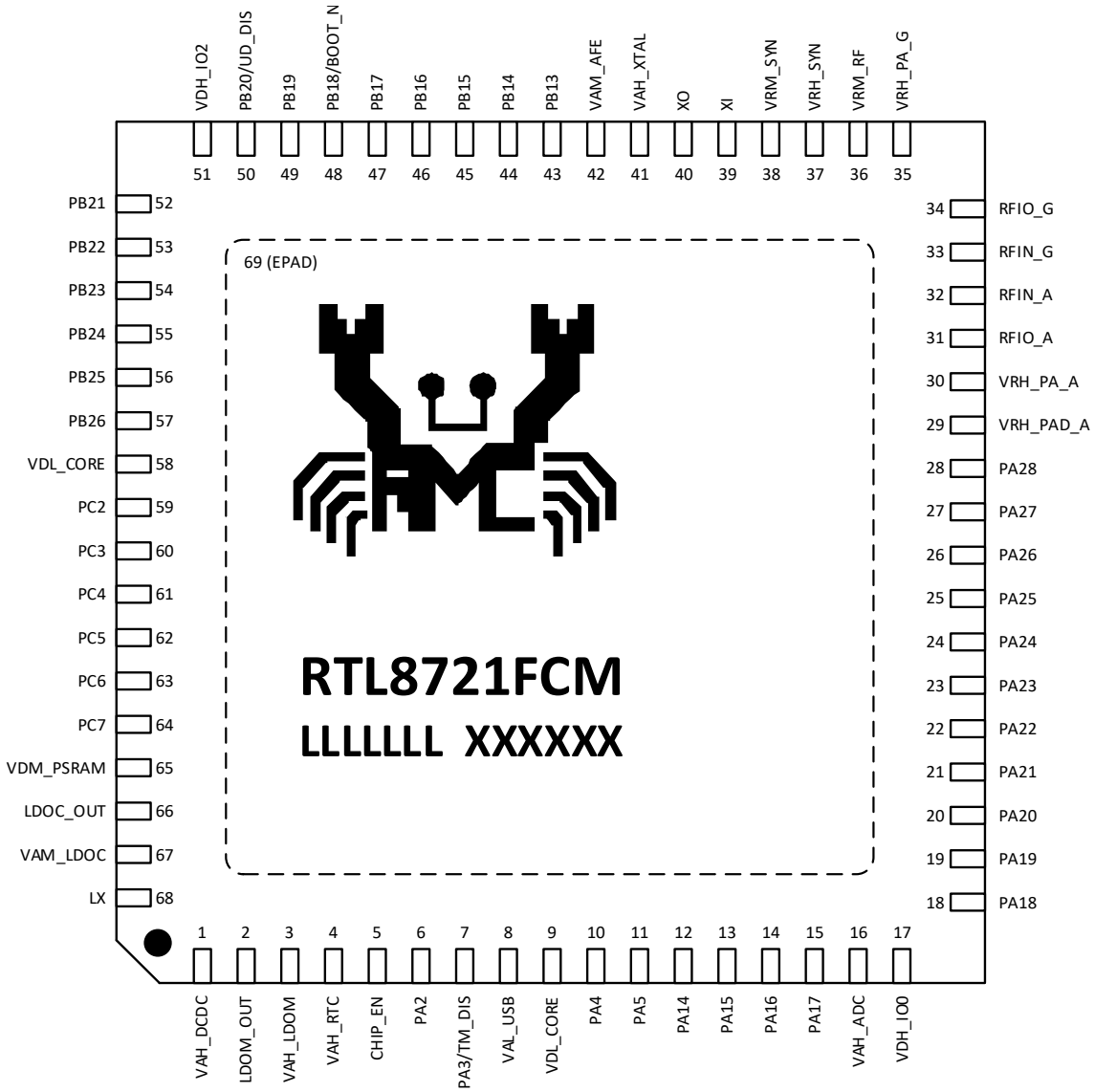


Figure 5-3 RTL8721FCM series pinout

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

5.3 QFN100

5.3.1 RTL8721FLM

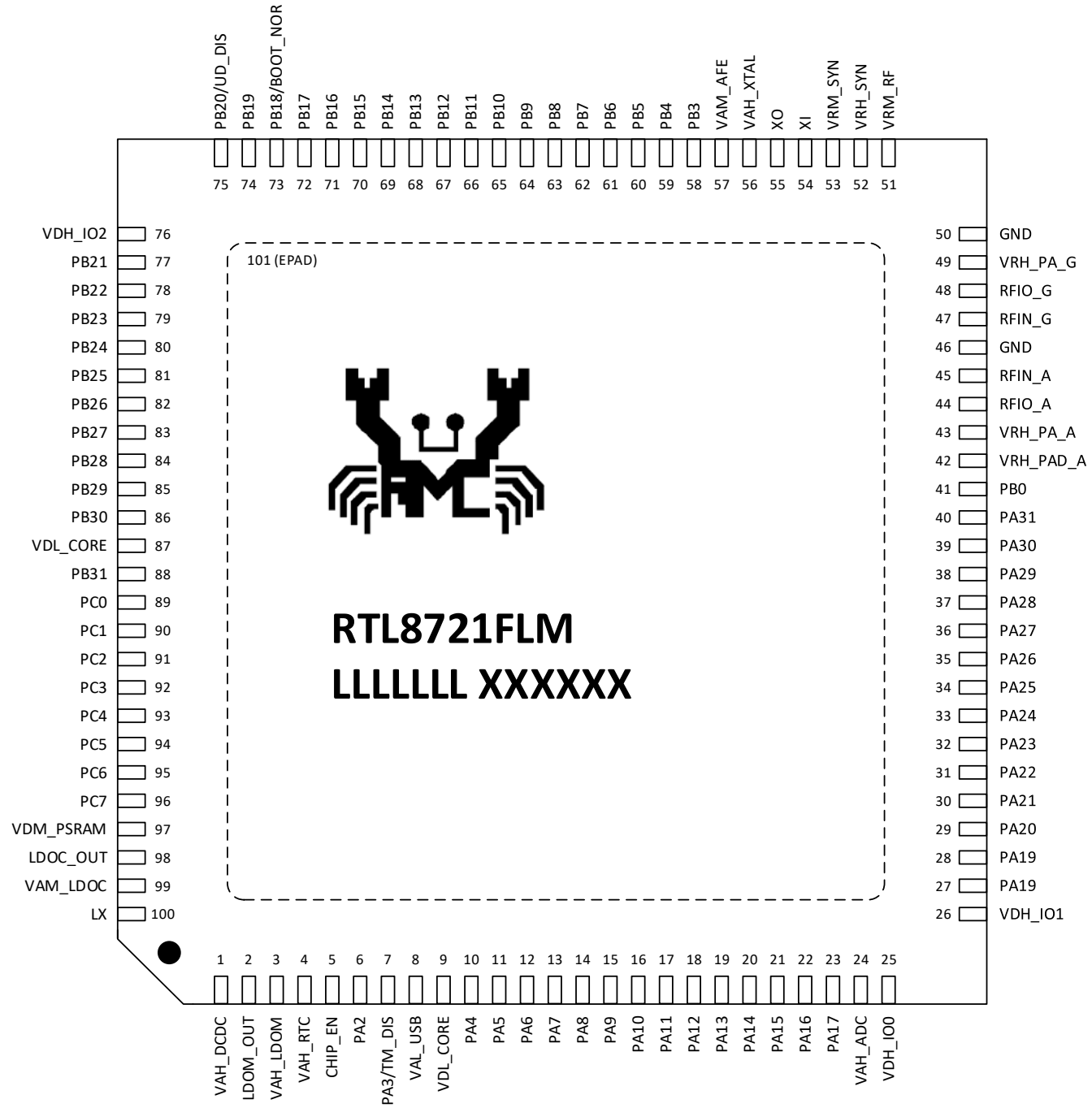


Figure 5-4 RTL8721FLM series pinout

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

6 Pin Description

6.1 Pin Definition

The definitions of pin type are listed below:

- I/O: Input/output pin
- A: Analog signal pin
- P: Power supply pin
- G: Ground pin
- RST: Reset pin

Pin No.				Pin name	Pin type	Default function	Description
RTL8721FAF	RTL8721FAM	RTL8721FCM	RTL8721FLM				
1	1	1	1	VAH_DCDC	P	-	Power input for DCDC
-	2	2	2	LDOM_OUT	P	-	Power output of LDOM
2	-	-	-	PA0	I/O	-	This is multi-function pin. The default function is general-purpose input/output, and it can be configured as other functions. This pin is also WAKE_PIN3, one of the wake up pins which can be a wakeup source to wake up the chip from deep-sleep mode. This function can be enabled via register after power on.
3	3	3	3	VAH_LDOM	P	-	Power input for LDOM
-	-	4	4	VAH_RTC	P	-	Power input for RTC
4	4	5	5	CHIP_EN	RST	-	Chip enable or shut-down selected pin. ● 1: Enable the chip ● 0: Shut down the chip
5	5	6	6	PA2	I/O	LOGUART Rx	This is multi-function pin. The default function is LOGUART Rx, and it can be configured as other functions. This pin is also WAKE_PIN1, one of the wake up pins which can be a wakeup source to wake up the chip from deep-sleep mode. This function can be enabled via register after power on.
6	6	7	7	PA3/TM_DIS	I/O	GPIO	This is multi-function pin. During power on, this pin is Test Mode Disable (TM_DIS) pin. The logical voltage level on this pin during power on determines the chip's operating mode: ● 1: Normal operating mode ● 0: Test mode for internal use. **DO NOT let the chip enter into this mode for normal usage**. After power on, this pin is PA3 I/O pin. The default function is general-purpose input/output. It can be configured as other functions by register setting. This pin is also WAKE_PIN0, one of the wake up pins which can be a wakeup source to wake up the chip from deep-sleep mode. This function can be enabled via register after power on.
7	7	8	8	VAL_USB	P	-	Power input for USB
8	8	9	9	VDL_CORE	P	-	Power input for the digital core domain
9	9	10	10	PA4	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
10	10	11	11	PA5	I/O	GPIO	
-	-	-	12	PA6	I/O	GPIO	
-	-	-	13	PA7	I/O	GPIO	
-	-	-	14	PA8	I/O	GPIO	
-	-	-	15	PA9	I/O	GPIO	
-	-	-	16	PA10	I/O	GPIO	
-	-	-	17	PA11	I/O	GPIO	
-	-	-	18	PA12	I/O	GPIO	
-	-	-	19	PA13	I/O	GPIO	
-	-	12	20	PA14	I/O	GPIO	
-	-	13	21	PA15	I/O	GPIO	
-	-	14	22	PA16	I/O	GPIO	

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

-	-	15	23	PA17	I/O	GPIO	
11	11	16	24	VAH_ADC	P	-	Power input for the ADC
12	12	17	25	VDH_IO0	P	-	Power input for the digital I/O
-	-	-	26	VDH_IO1	P	-	Power input for the digital I/O
13	13	18	27	PA18	I/O	SWD CLK	The default function is SWD signals, and it can be configured as other functions.
14	14	19	28	PA19	I/O	SWD DATA	
15	15	20	29	PA20	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
16	16	21	30	PA21	I/O	GPIO	
-	-	22	31	PA22	I/O	GPIO	
-	-	23	32	PA23	I/O	GPIO	
-	-	24	33	PA24	I/O	GPIO	
17	17	25	34	PA25	I/O	GPIO	
18	18	26	35	PA26	I/O	GPIO	
-	-	27	36	PA27	I/O	GPIO	
-	-	28	37	PA28	I/O	GPIO	
-	-	-	38	PA29	I/O	GPIO	
-	-	-	39	PA30	I/O	GPIO	
-	-	-	40	PA31	I/O	GPIO	
-	-	-	41	PB0	I/O	GPIO	
19	19	29	42	VRH_PAD_A	P	-	Power input for RF circuit
20	20	30	43	VRH_PA_A	P	-	Power input for RF circuit
21	21	31	44	RFIO_A	A	-	WLAN 5GHz radio transmitter output and receiver input
22	22	32	45	RFIN_A	A	-	WLAN 5GHz RF AUX input
-	-	-	46	GND	G	-	To be connected to ground
23	23	33	47	RFIN_G	A	-	WLAN 2.4GHz RF AUX input
24	24	34	48	RFIO_G	A	-	WLAN 2.4GHz & BT shared radio transmitter output and receiver input
25	25	35	49	VRH_PA_G	P	-	Power input for RF circuit
-	-	-	50	GND	G	-	To be connected to ground
26	26	36	51	VRM_RF	P	-	Power input for RF circuit
27	27	37	52	VRH_SYN	P	-	Power input for RF circuit
28	28	38	53	VRM_SYN	P	-	Power input for RF circuit
29	29	39	54	XI	A	-	Input of 40MHz crystal clock reference
30	30	40	55	XO	A	-	Output of 40MHz crystal clock reference
31	31	41	56	VAH_XTAL	P	-	Power input for XTAL
32	32	42	57	VAM_AFE	P	-	Power input for RF AFE
-	-	-	58	PB3	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	59	PB4	I/O	GPIO	
-	-	-	60	PB5	I/O	GPIO	
-	-	-	61	PB6	I/O	GPIO	
-	-	-	62	PB7	I/O	GPIO	
-	-	-	63	PB8	I/O	GPIO	
-	-	-	64	PB9	I/O	GPIO	
-	-	-	65	PB10	I/O	GPIO	
-	-	-	66	PB11	I/O	GPIO	
-	-	-	67	PB12	I/O	GPIO	
-	-	43	68	PB13	I/O	GPIO	
-	-	44	69	PB14	I/O	GPIO	
-	-	45	70	PB15	I/O	GPIO	
-	-	46	71	PB16	I/O	GPIO	
33	33	47	72	PB17	I/O	GPIO	
-	34	48	73	PB18/BOOT_NOR	I/O	GPIO	This is multi-function pin. During power on, this pin is BOOT from NOR (BOOT_NOR) pin. The logical voltage level on this pin during power on determines flash controller's configuration for different types of flash: ● 1: NOR Flash ● 0: NAND Flash After power on, this pin is PB18 I/O pin. The default function is general-purpose input/output, and it can be configured as other functions.
34	-	-	-	PB18	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
35	35	49	74	PB19	I/O	GPIO	
36	36	50	75	PB20/UD_DIS	I/O	LOGUART Tx	This is multi-function pin. During power on, this pin is UART Download Mode Disable (UD_DIS) pin. The logical voltage level on this pin during power on determines the chip's operating mode: ● 1: Normal boot mode ● 0: UART download mode After power on, this pin is PB20 I/O pin. The default function is

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

							LOGUART Tx. If it is configured as a GPIO function, the LOGUART function becomes invalid.
37	37	51	76	VDH_IO2	P	-	Power input for the digital I/O
-	-	52	77	PB21	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	53	78	PB22	I/O	GPIO	
-	-	54	79	PB23	I/O	GPIO	
-	-	55	80	PB24	I/O	GPIO	
-	-	56	81	PB25	I/O	GPIO	
-	-	57	82	PB26	I/O	GPIO	
-	-	-	83	PB27	I/O	GPIO	
-	-	-	84	PB28	I/O	GPIO	
-	-	-	85	PB29	I/O	GPIO	
-	-	-	86	PB30	I/O	GPIO	
38	38	58	87	VDL_CORE	P	-	Power input for the digital core domain
-	-	-	88	PB31	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	89	PC0	I/O	GPIO	
-	-	-	90	PC1	I/O	GPIO	
-	39	59	91	PC2	I/O	Flash_IO1	The default function is Flash signals, and it can't be configured as other functions.
-	40	60	92	PC3	I/O	Flash_CSN	
-	41	61	93	PC4	I/O	Flash_IO3	
-	42	62	94	PC5	I/O	FLASH_CLK	
-	43	63	95	PC6	I/O	FLASH_IO0	
-	44	64	96	PC7	I/O	FLASH_IO2	
39	-	-	-	PC2	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
40	-	-	-	PC3	I/O	GPIO	
41	-	-	-	PC4	I/O	GPIO	
42	-	-	-	PC5	I/O	GPIO	
43	-	-	-	PC6	I/O	GPIO	
44	-	-	-	PC7	I/O	GPIO	
	-	-	-	PC8	I/O	GPIO	
45	-	-	-	VDH_FLASH	P	-	Power input for Flash
-	45	65	97	VDM_PSRAM	P	-	Power input for PSRAM
46	46	66	98	LDOC_OUT	P	-	Power output of LDOC
47	47	67	99	VAM_LDOC	P	-	Power input for LDOC
48	48	68	100	LX	P	-	DCDC output
49	49	69	101	EPAD	G		Whole system Ground, to be connected to ground

6.2 Power Supply for I/O Pins

Several I/O pins belong to a specific power supply group and have corresponding power supply pin.

Refer to *Realtek_RTL8721F_pin_mux.xlsx* for I/O group information and allowed supply voltage range.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7 Functional Description

7.1 Power Management

7.1.1 Power Structure

Single external power supply is required for the RTL8721F. All the other required voltages can be converted and outputted by two embedded low-dropout regulators (LDO) and one embedded DC-DC switching regulator (DCDC).

- Active mode:
  - The DCDC outputs typical 1.25V or 1.35V for RF circuits and LDO core (LDOC) input.
  - The LDOC outputs typical 0.9V or 1.0V for digital core circuits.0.9V or 1.0V is based on CPU frequency setting.
  - The LDO memory (LDOM) outputs typical 1.8V for optional embedded PSRAM based on different part numbers.
- Sleep mode:
  - The DCDC outputs typical 0.7V or 0.8V for RF circuits and LDO core (LDOC) input.
  - The LDOC outputs typical 0.7V or 0.8V for digital core circuits.
  - The LDOM can output typical 1.8V or be shutdown based on configuration for different usage scenarios.
- Deep-sleep mode:
  - The DCDC, LDOC, and LDOM are all shut down.

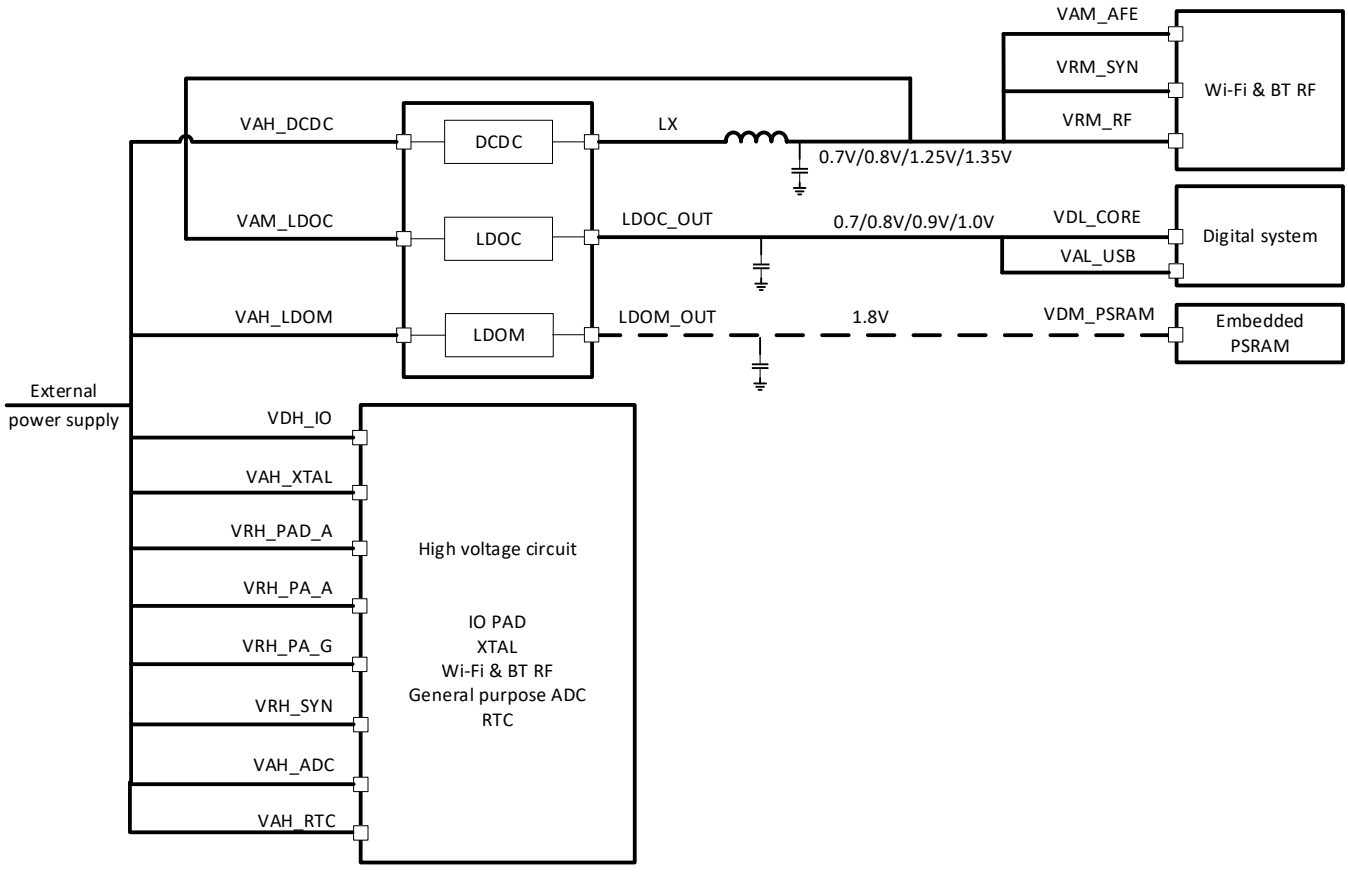


Figure 7-1 Power block diagram

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.1.2 Power Supply Supervisor

The RTL8721F has integrated a power-on reset (POR) circuit and a brownout detect (BOD) circuit.

7.1.2.1 Power-on Reset (POR)

The POR supervisor monitors VAH_LDOM power supply input during power on and power off.

- When VAH_LDOM is higher than V_{POR_H}, the chip releases the internal reset.
- When VAH_LDOM is lower than V_{POR_L}, the chip remains in reset mode.

Refer to *Power Sequence* for more details.

7.1.2.2 Brownout Detect (BOD)

The BOD supervisor monitors VAH_LDOM power supply input. The BOD function can work in reset mode or interrupt mode, and has independent falling threshold V_{BOD_L} and rising threshold V_{BOD_H}. The BOD function is enabled in reset mode by default and can be disabled or switched to interrupt after power on.

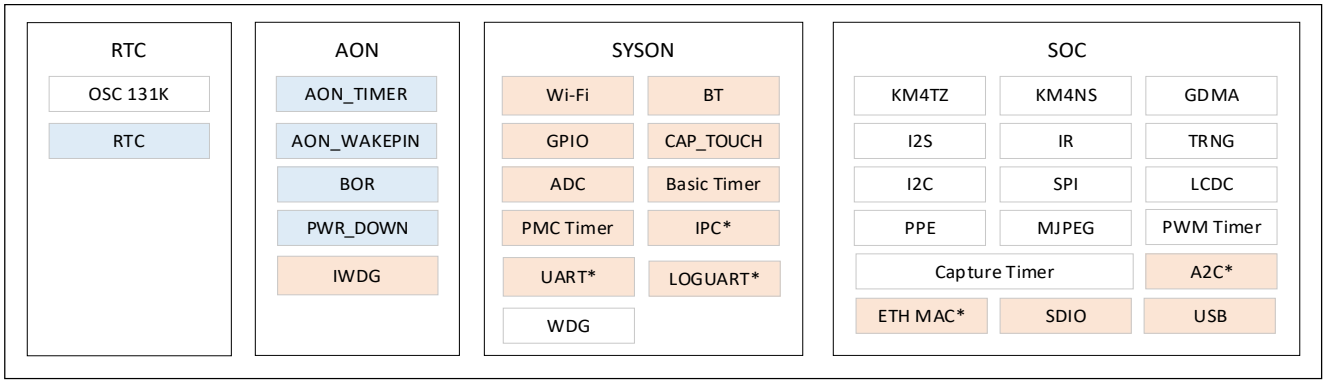
- When VAH_LDOM drops below V_{BOD_L}, the BOD circuit will trigger an interrupt or a reset depending on the register configuration.
- When VAH_LDOM rises above V_{BOD_H}, the BOD circuit will release the internal reset. V_{BOD_L} and V_{BOD_H} can be chosen by setting the register, but V_{BOD_H} must be set higher than V_{BOD_L}.

Refer to *Power Sequence* for more details.

7.1.3 Power Domain

There are different power domains in the RTL8721F, and RTC, AON, SYSON, SOC are four main power domains in the digital system. Users can flexibly power up different power domains to achieve the best balance between the performance and power consumption. Functions in different power domains will be turned off differently in different power-saving modes. More information about power domains and wakeup sources are depicted in *Figure 7-2*.

Some peripherals (such as UART, LOGUART, …) can only wake up the system under some special conditions, refer to *Table 7-2* for more details.



The peripheral on AON/RTC domain can be a wakeup source from deep-sleep and sleep mode.
The peripheral on AON/SYSON/SOC domain can be a wakeup source from sleep mode.
* The peripheral can only wake up the system under some special conditions.

Figure 7-2 Power domains and wakeup sources

7.1.4 Power Mode

By controlling the power and clock of individual functions, the RTL8721F can support both active mode and power saving mode.

The two special power-saving modes, sleep mode and deep-sleep mode, are to achieve low power consumption with different peripherals running.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

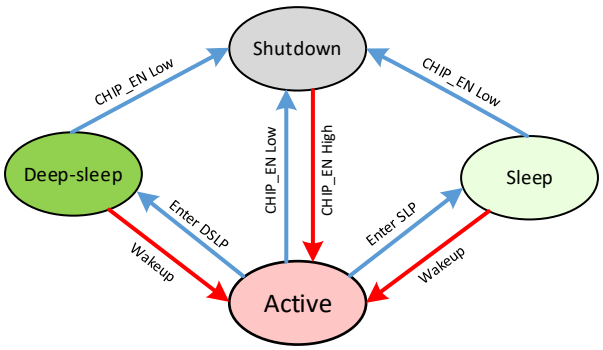


Figure 7-3 Switch among different power modes

7.1.4.1 Active Mode

In active mode, all the digital modules are powered on. Each of them can be configured as active or clock-gated, depending on the application requirement. In addition, there are individual power-down controls for some of the analog peripherals.

7.1.4.2 Sleep Mode

In sleep mode, the system exhibits the following behaviors:

- Most functions and the SoC domain are power-gated or clock-gated to conserve power.
- The contents of the memory are retained, enabling the system to remember its previous state and resume operation from where it left off before entering sleep mode once it wakes up.
- Certain peripherals can be used as wakeup sources, and interrupts can trigger these peripherals to wake up the system. The selection of different sleep states mainly depends on the required wakeup sources. If a peripheral of the SoC domain is used as a wakeup source, clock-gated mode should be selected.

7.1.4.3 Deep-sleep Mode

In deep-sleep mode, all functional blocks are powered down except for the Always-On (AON) domain and the Real-Time Clock (RTC) domain. The system's main memory (e.g., SRAM or PSRAM) is also powered off to achieve ultra-lower power consumption.

The system can only be awakened by an interrupt or event generated from the AON or RTC domains. When exiting from the deep-sleep mode, the system follows the normal boot flow.

7.1.4.4 Wakeup Source

Table 7-1 summarizes typical power modes supported by RTL8721F, which is a non-exhaustive list.

Table 7-1 Power modes

Function	Power mode				
	Shutdown	Deep-sleep	Sleep		Active
			Power gating	Clock gating	
WLAN	OFF	OFF	Software configurable	Software configurable	Software configurable
Bluetooth	OFF	OFF	Software configurable	Software configurable	Software configurable
Processors + Cache	OFF	OFF	OFF	Clock gating	ON
SRAM	OFF	OFF	Retention	Retention	ON
RTC	OFF	Software configurable	Software configurable	Software configurable	Software configurable
AON peripherals	OFF	Software configurable	Software configurable	Software configurable	Software configurable
SYSON peripherals	OFF	OFF	Software configurable	Software configurable	Software configurable
SOC peripherals	OFF	OFF	OFF	Software configurable	Software configurable

Table 7-2 lists the wakeup sources of power-saving mode.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Table 7-2 Wakeup sources of power-saving mode

Power-saving mode	Wakeup source	Restriction
Sleep mode	WLAN	
	BT	
	IPC	Only KM4NS can use the IPC to wake up KM4TZ
	Basic Timer	Timer 0 ~ 3 can be wake sources in sleep mode.
	PMC Timer	
	UART	● When using UART as a wakeup source, the Rx clock source can only be OSC2M, and do not turn off OSC4M during sleep. ● When the baudrate is larger than 115200, it is not recommended to use UART as a wakeup source. ● The portion of the command used to wake up that exceeds the FIFO depth (64B) will be lost.
	LOGUART	● When using LOGUART as a wakeup source: ■ If the Rx clock source is XTAL40M, do not turn off XTAL or OSC4M during sleep. ■ If the Rx clock source is OSC2M, do not turn off OSC4M during sleep. ● The portion of the command used to wake up that exceeds the FIFO depth (32B) will be lost.
	GPIO	
	Ethernet MAC	● The voltage needs to be maintained at 0.9V or higher. ● The PLL for Ethernet MAC should be turned on.
	CAP_TOUCH	
	A2C	● The voltage needs to be maintained at 0.8V. ● OSC4M needs to be turned on.
	IWDG	
	ADC	
	SDIO	Only clock gating is supported.
	USB	Only clock gating is supported.
Deep-sleep mode	AON_TIMER	
	AON_WAKEPIN	
	RTC	
	BOR	
	CHIP_EN	To use CHIP_EN wake up the system, the Interrupt Mode must be explicitly enabled.

7.2 Reset and Clock Control (RCC)

The RCC module manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides high flexibility in the choice of clock sources and allows the application of clock ratios to improve power consumption.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.2.1 Reset Control

7.2.1.1 Reset Diagram

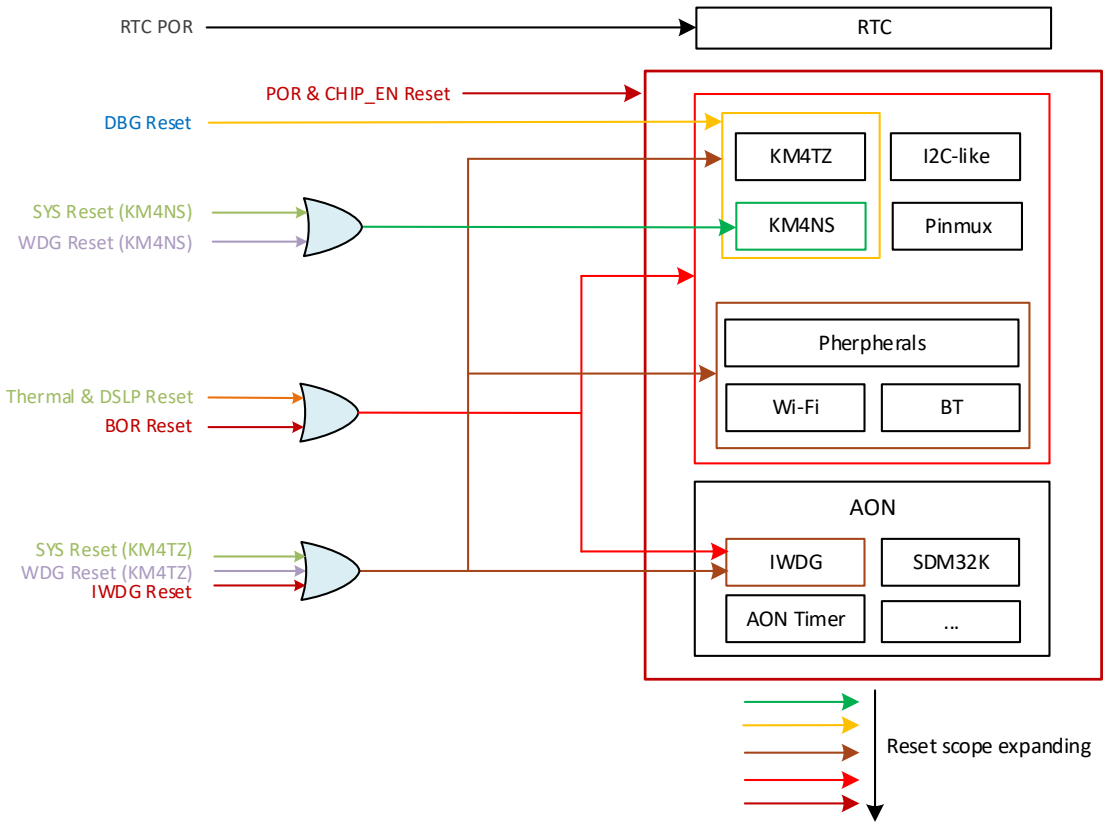


Figure 7-4 Reset diagram

7.2.1.2 Reset Type

The following reset sources or events are able to generate a reset.

Table 7-3 Reset types

Reset type	Description
POR	A power-on reset is generated when power on
CHIP_EN	Generated by external CHIP_EN pin
BOR	A brownout reset is generated when BOR reset detected
Thermal	Generated by internal temperature protection
DSLP	A DSLP reset is generated when waking from deep-sleep
WDG	A watchdog reset is generated when watchdog timeout
SYS	A system reset is triggered by software
DBG	A debug reset is triggered by SWD debug

7.2.1.3 Reset Domain

Different reset types reset different domains:

- The RTC has its own power-on reset, and has a separate reset scope itself.
- The power-on reset (POR) and external CHIP_EN reset can reset the whole chip.
- The BOR reset, Thermal reset, and DSLP reset can reset the system peripherals and IWDG.
- The IWDG reset, SYS reset, WDG reset and can reset IWDG and all peripherals except I2C-like and Pinmux.
- The KM4NS SYS Rest and WDG reset Default reset scope is same with IWDG, they can be configured to reset KM4NS CPU itself only
- A debug reset is triggered by SWD debug, which will reset the CPU core definitely, and has the flexibility to reset the other CPU core and peripherals.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.2.2 Clock Control

The clock sources of RTL8721F are listed below. Different clock sources can drive different functions.

- 40MHz clock based on external oscillator:
  - XTAL40M: used for peripherals directly or after frequency division.
- Internal oscillators:
  - OSC4M: provides clock for peripherals after frequency division.
  - OSC131K: used for input of SDM and clock for Cap-Touch.
  - OSC100K: resides in the AON domain and used for driving the IWDG.
- Separate PLLs:
  - SYS_PLL: 200MHz ~ 500MHz. The PLL supports fractional-N frequency division, which is ideal for applications requiring precise frequency tuning, such as high-quality audio systems.
  - USB_PLL: 480MHz ~ 1000MHz. The PLL can only generate output frequencies that are integer multiples of the crystal (XTAL) reference frequency.
  - Except for peripherals with specific clock requirements (e.g., USB, Ethernet MAC, and audio systems), other high-speed peripherals and the CPU can select their clock sources from any of the available PLLs via the clock selection mechanism.

7.3 CPU Architecture

7.3.1 Dual-Core Subsystem

There are two KM4 processors in RTL8721F for different purposes.

- KM4TZ: KM4 with TrustZone-M security technology, usually works as Application Processor (AP)
- KM4NS: KM4 without TrustZone-M security technology, usually works as Network Processor (NP)

The boot sequence always starts with KM4TZ. After KM4TZ boots, it will decide whether to bring up KM4NS for execution.

7.3.2 KM4 Processor

The KM4 is a 3-staged pipelined 32-bit high-performance processor that bases on Armv8.1-M architecture supporting Arm Cortex-M55 instruction set compatible, and offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration for high-performance, deeply embedded applications. The TrustZone-M security technology provides hardware-enforced isolation between the Trusted and Non-Trusted resources on the devices, while maintaining the efficient exception handling and determinism. The KM4 achieves an optimal blend between real-time determinism, energy efficiency, software productivity, and system security that opens the door for many new applications and opportunities across diverse markets.

The KM4 processor has the following features:

- Armv8.1-M mainline architecture
- 3-stage pipeline to support the clock frequency of up to 334MHz
- Thumb/Thumb-2 technology
- TrustZone-M technology for Armv8-M, with Security Attribution Unit (SAU) of up to 8 regions
- 16K bytes I-Cache, 16K bytes D-Cache
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Memory Protection Unit (MPU) with up to 8 regions with non-secure state and 4 regions with secure state
- Waking up the processor from state retention power gating or when all clocks are stopped
- Non-maskable Interrupt (NMI) and physical interrupts with 8 priority levels
- Integrated wait for event (WFE) and wait for interrupt (WFI) instructions
- JTAG and Serial Wire Debug ports, up to 4 instruction breakpoints and 1 data watchpoint

The KM4 is designed to run up to 267MHz at 0.9V and 334MHz at 1.0V.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.4 Memory Mapping

The RTL8721F incorporates several distinct memory regions. Program memory, data memory, registers, and I/O ports are organized within the same linear 4G bytes address space. The bytes are coded in memory in Little-Endian format.

The addressable space is divided into multiple main blocks. All the memory areas that are not allocated to on-chip memories and peripherals are considered “RSVD” (reserved).

Base address	End address	Size (bytes)	Function		TrustZone*
0x0000_0000	0x000F_FFFF	1M	KM4 internal ROM or TCM	ROM Flash	-
0x0010_0000	0x001F_FFFF	1M	Common ROM		
0x0020_0000	0x0FFF_FFFF	254M	SPI NOR Flash		
0x1000_0000	0x101F_FFFF	2M	ROM	ROM Flash	Secure
0x1020_0000	0x1FFF_FFFF	254M	SPI NOR Flash		
0x2000_0000	0x200F_FFFF	1M	SRAM	SRAM	-
0x2010_0000	0x2FFF_FFFF	255M	RSVD		
0x3000_0000	0x300FFFFF	1M	SRAM	SRAM	Secure
0x3010_0000	0x3FFF_FFFF	255M	RSVD		
0x4000_0000	0x407F_FFFF	8M	High-Speed peripherals group	Peripherals	-
0x4080_0000	0x417F_FFFF	16M	Low-Speed peripherals group		
0x4180_0000	0x4FFF_FFFF	232M	RSVD		
0x5000_0000	0x507F_FFFF	8M	High-Speed peripherals group	Peripherals	Secure
0x5080_0000	0x517F_FFFF	16M	Low-Speed peripherals group		
0x5180_0000	0x5FFF_FFFF	232M	RSVD		
0x6000_0000	0x6FFF_FFFF	256M	External PSRAM	DRAM	-
0x7000_0000	0x7FFF_FFFF	256M	External PSRAM	DRAM	Secure

NOTE

- *The function of TrustZone is only applicable to KM4TZ, so the secure address spaces can only be accessed from the secure world of KM4TZ and other security-capable masters.*
- *The security attribution of address space is determined by the bit[28] of this address.*
- *The memory space in the table represents logical address mapping, but not the actual physical memory size. For example:*
  - *The system SRAM is logically mapped as 1MB in the memory map, but the actual physical size is only 512KB.*
  - *When the BT function is disabled, the physical memory inside the BT module can be mapped to the address space above 512KB and shared with the system for general use.*

7.5 Memory Subsystem

The RTL8721F incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash controller provides a flexible and efficient way to access Flash (e.g., byte and block access). A multilayer AXI interconnect supports internal and external memory access.

The memory of RTL8721F consists of the following types:

- ROM
- TCM
- SRAM
- Flash
- PSRAM

7.5.1 ROM

The ROM address space is mapped from 0x0000_0000 to 0x000E_FFFF. It consists of two main components: the KM4TZ ROM and the Common ROM.

- KM4TZ ROM: contains the core boot code responsible for initializing the system during power-on or reset.
- Common ROM: provides shared firmware functions and system-level utilities accessible by both processors.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.5.2 TCM

The KM4 core is equipped with 16KB of instruction cache (I-Cache) and 16KB of data cache (D-Cache). When the caches are disabled, the underlying memory can be used as Tightly Coupled Memory (TCM), providing deterministic access for time-critical applications. The TCM address space is mapped from 0x000F_0000 to 0x000F_FFFF.

7.5.3 On-chip SRAM

The on-chip SRAM starts from 0x2000_0000 and consists of two blocks:

- A general purposed 512KB of contiguous SRAM for system heap and application
- A dedicated 152KB of connectivity SRAM shared with Bluetooth (lower protocol stack)

All the SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits) by processors, DMA engine and other AXI masters.

The entire SRAM can be disabled or enabled in the Power Management Unit (PMU) to save power, and can also enter retention mode for quickly resuming from sleep mode when the system enters sleep mode.

7.5.4 Flash

The Flash memory consists of a SPI Flash controller and a Flash memory array module. The SPI Flash controller acts as an interface between the system bus and the Flash memory device. It implements the erase and program Flash memory operations, and the read/write protection mechanisms, and accelerates code execution with a system of instruction prefetch and cache lines.

The SPI Flash controller of RTL8721F supports SPI NOR/NAND Flash with Single/Dual/Quad I/O pins.. It can run up to 104MHz Single Data Rate (SDR) speed.

7.5.5 PSRAM

The PSRAM controller of RTL8721F supports high-speed hyperbus PSRAM with Double Data Rate (DDR).

- Clock rate: up to 200MHz
- 8-/16-bit I/O
- Supports half sleep-mode and deep power-down mode

7.6 RF Subsystem

7.6.1 RF Block Diagram

The Radio Frequency (RF) block diagram of RTL8721F, including WLAN and BT modem, is given in *Figure 7-5*.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

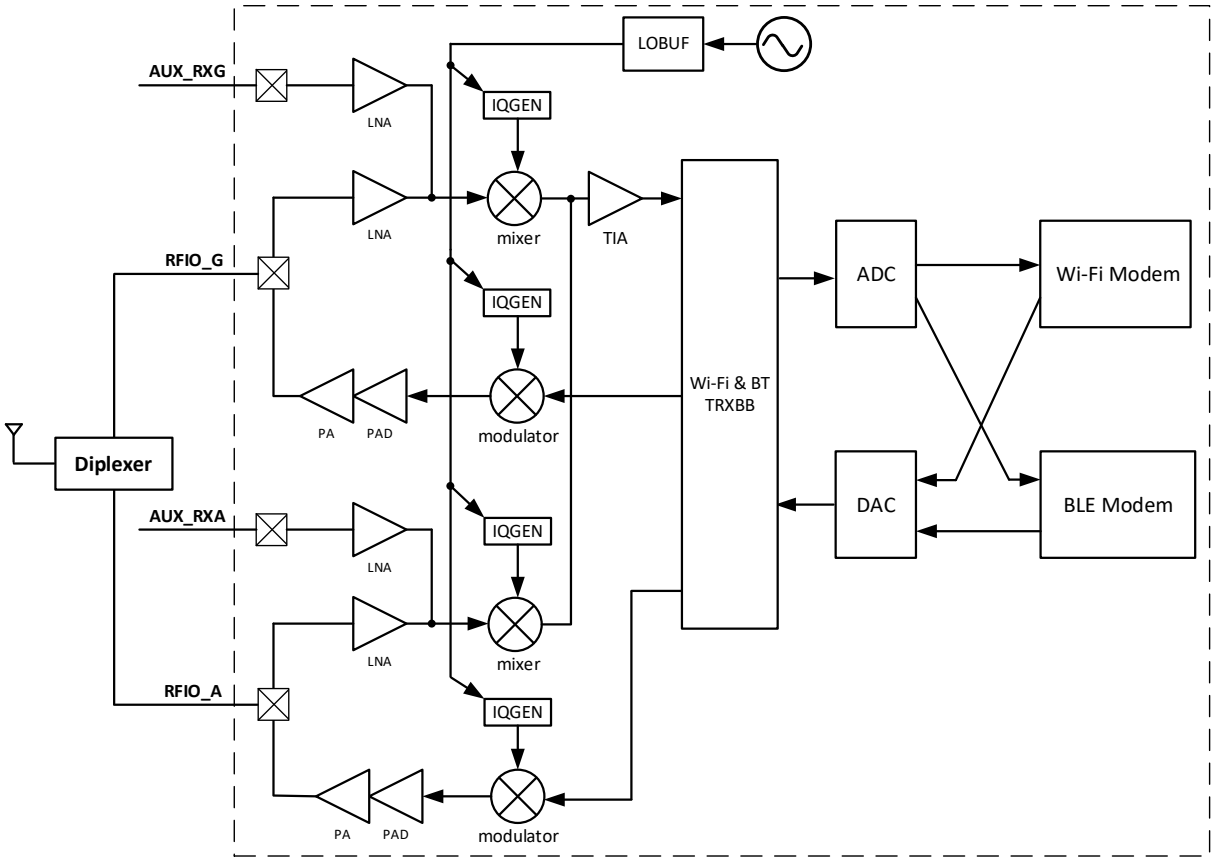


Figure 7-5 RF block diagram

7.6.2 WLAN

The RTL8721F includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4GHz and 5GHz Wireless LAN systems. It is designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4GHz unlicensed ISM or 5GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing and gain control functions. The integrated on-chip baluns convert the fully differential transmit and receive paths to single-ended signal pins.

The WLAN radio subsystem of RTL8721F consists of the following modules:

- Receiver
- Transmitter
- Real-time calibration

7.6.2.1 WLAN Receiver

The RTL8721F has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the 5GHz U-NII band. At port RFIO_G, an on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN 2.4G receivers, while the 5GHz at port RFIO_A receiver path has a dedicated on-chip LNA. Because the NF of receiver path is lower enough, external LNA is not necessary, which can increase the receive sensitivity no more than 1dB.

7.6.2.2 WLAN Transmitter

The baseband data is modulated and up-converted to the 2.4 GHz ISM band or 5GHz U-NII band respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11 a/b/g/n specifications without the need for external PAs. But if you do want high Tx power, external PA can be added. When using the internal PAs, closed-loop output power control is completely integrated.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.6.2.3 Real-time Calibration

The RTL8721F adopts real-time and automatic on-chip calibration mechanisms to ensure that normal radio system can operate perfectly, and users do not need to do extra operations to enhance Tx/Rx performance. These calibration mechanisms that are merged into software or hardware continually compensate for temperature and process variations across components. Examples of some of these algorithms are digital correction, such as:

- I-Q compensation calibration
- Digital pre-distortion calibration for good EVM performance of the transmitter
- LO calibration for carrier leakage reduction

7.6.3 Bluetooth

7.6.3.1 Bluetooth Transceiver

The fully integrated radio transceiver is compliant with Bluetooth SIG test specifications, and designed for low power consumption, excellent transmit and receive performance in the ISM band.

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy (BLE)

7.6.3.2 Bluetooth Transmitter

The modulator translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

7.6.3.3 Bluetooth Receiver

The LNA amplifies a low-energy RF signal to the desired level without significantly increasing the noise power. When input power is high, the design limits non-linearity. The Receive mixer is a device whose input is an RF signal, and the output is an IF signal. The IF signal is then passed along the IF path to the demodulator.

7.7 WLAN Subsystem

7.7.1 WLAN Baseband

The WLAN baseband of RTL8721F supports the following features:

- 802.11 a/b/g/n/ac/ax
- 802.11ax MCS0-9, 20MHz bandwidth, up to 114.7Mbps of data rate
- Integrated 2.4GHz&5GHz PA and LNA, and T/R switch
- Integrated 2.4GHz&5GHz balun
- Support both internal and external PA
- Adjustable transmitting power
- Supports Channel State Info (CSI)
- Supports Tx Low-Density Parity Check (LDPC), Tx Binary Convolutional Code (BCC), and Rx BCC
- Supports Rx STBC 2x1
- Supports SU/MU Beamformee
- Supports Rx DL-OFDMA, Tx UL-OFDMA
- Supports 802.11ax Dual Carrier Modulation (DCM)/ER Tx/Rx
- Supports Spatial Reuse to maximize parallel transmissions
- Short guard interval
- Supports digital pre-distortion to enhance PA performance
- Smoothing for channel estimation
- Antenna diversity

The RTL8721F supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and select the best antenna to minimize the effects of channel fading.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.7.2 WLAN MAC

The WLAN MAC of RTL8721F applies low-level protocol functions automatically. It supports the following features:

- Frame aggregation for increased MAC efficiency (A-MPDU])
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Supports Target Wake Time (TWT) function for power saving
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- Supports Enhanced Distribution Channel Access (EDCA) and MU EDCA
- Supports for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Supports 2 Network Allocation Vector (NAV)
- Supports Basic Service Set (BSS) color
- Supports Time Synchronization Function (TSF) auto-sync
- IEEE 802.11i (WPA, WPA2, WPA3), open, shared key, and pair-wise key authentication services
- Rx trigger frame (except GCR MU-BAR and NFRP)
- Supports AP/STA/Concurrent mode (802.11ax AP not supported)
- Supports Multi Channel Concurrent (MCC) mode by software TDMA
- Supports Wi-Fi Tunnel (WTN)
- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmitting beamforming as beamformee
- Support group key update

7.8 Bluetooth Subsystem

The RTL8721F integrates a hardware link layer controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

7.8.1 Bluetooth Baseband

The Bluetooth baseband of RTL8721F supports the following features:

- Compliant with Bluetooth Core Specification including LE-1M/LE-2M/LE-Coded (Long Range)
- Fast AGC control to improve receiving dynamic range
- Supports serial Flash for firmware storage and parameter upgrade
- Supports channel map update to dynamically detect channel quality to improve transmission quality

7.8.2 Bluetooth Link Controller

- Bluetooth 5.0 specification compliant, single mode:
  - Bluetooth Low Energy (BLE)
- Integrated MCU to execute Bluetooth protocol stack
- LE advertising extensions
- Supports piconets in a scatter-net
- Enhanced Bluetooth/WLAN Co-existence Control to improve transmission quality in different profiles
- Supports multiple Low Energy states

7.9 Security

The RTL8721F is designed to safely hold security-related data such as cryptographic keys and general-purpose security information with the following security techniques.

- Secure boot
- Arm TrustZone-M
- True Random Number Generator (TRNG)
- Hardware crypto engine
- Public key engine
- Whole or partial Flash decryption
- Read Protection (RDP)

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- Secure JTAG/SWD
- 2K bytes OTP

7.9.1 Secure Boot

Secure boot aims at firmware protection, which prevents attackers from modifying or replacing firmware maliciously. When the chip is powered on, the secure boot ROM executes to check the validity of the image signature.

The RTL8721F supports the following algorithms of secure boot:

- Signing/Authentication algorithm:
  - Ed25519
  - ECDSA: SECP192R1, SECP224R1, SECP192R1, BP256R1, SECP192K1, SECP224K1, SECP192K1
- Hash algorithm:
  - SHA2: 224, 256, 384, 512
  - HMAC_SHA2: 224, 256, 384, 512

7.9.2 Hardware Crypto Engine

The RTL8721F integrates SHA engine and AES engine, which can accelerate applications that need cryptographic functions, such as authentication, encryption and decryption. Hardware crypto engines executing these functions cannot only reduce software overhead but also save CPU and memory resources, and the processing is more secure and faster than software.

The crypto engine provides basic cryptographic features:

- Authentication algorithms
  - General cryptographic hash function
    - SHA2-224
    - SHA2-256
    - SHA2-384
    - SHA2-512
  - HMAC (Hash-based message authentication code)
    - HMAC_SHA2-224
    - HMAC_SHA2-256
    - HMAC_SHA2-384
    - HMAC_SHA2-512
- Cipher (Encryption/Decryption) algorithms
  - AES-128/192/256
    - ECB (Electronic Codebook) mode (weak, not recommended)
    - CBC (Cipher Block Chaining) mode
    - OFB (Output Feedback) mode
    - CFB (Cipher Feedback) mode
    - CTR (Counter) mode (weak, not recommended)
    - GCM (Galois/Counter Mode) mode
    - CMAC mode
    - XTS mode
- AES key management:
  - Six secure OTP keys: two keys for crypto engine only, and other four keys shared with RSIP
  - Two secure software keys
  - Two non-secure software keys
- HMAC key management:
  - Four secure OTP keys
  - Two secure software keys

Applies masking algorithms during AES encryption and decryption processes to randomize internal computational states, effectively mitigating risks from side-channel attacks.

7.9.3 Public Key Engine (PKE)

The Public Key Engine (PKE) provides hardware acceleration for public key algorithms and integrates active countermeasures against cryptographic attacks. In particular, the PKE supports both ECC and RSA cryptographic operations, offering enhanced performance and security for embedded and wireless applications.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Supported operations:

- RSA:
  - RSA private key operations (decryption & signature generation)
  - RSA public key operations (encryption & signature verification)
  - On-chip RSA key generation
  - Supports up to RSA-4096 bits
- ECC:
  - Standard ECC (Elliptic Curve Cryptography)
  - ECDH (Elliptic Curve Diffie-Hellman)
  - ECDSA (Elliptic Curve Digital Signature Algorithm)
  - EdDSA (Edwards-curve Digital Signature Algorithm)
  - Curve Size Support: Supports elliptic curves up to 512 bits

Security and attack countermeasures:

- DPA Defense: Equipped with Differential Power Analysis (DPA) protections, safeguarding private key operations against side-channel analysis
- Timing Attack Defense: Mitigate risks from timing-based side-channel attacks, securing cryptographic transactions against sophisticated threats

7.9.4 Secure Image Protection (RSIP)

Generally, both firmware and some data are stored in Flash memory. The SPI Flash controller is used to transmit/receive data from/to SPI Flash memory. In order to protect the firmware, the code and data in Flash can be encrypted with Advanced Encryption Standard (AES) algorithm. The RSIP is mainly used for MMU and image decryption.

The RSIP consists of two parts:

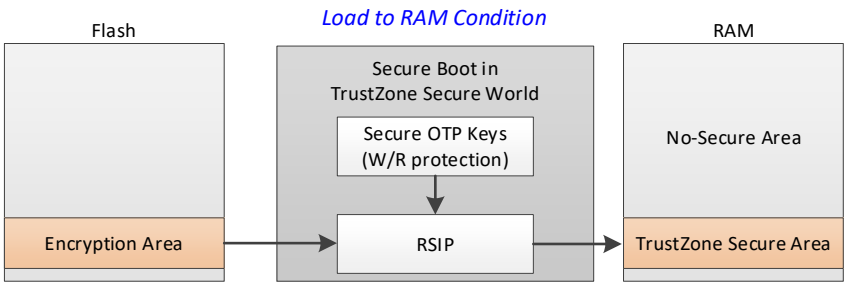
- RSIP-AES: performs Flash decryption on the fly.
- RSIP-MMU: used for virtual-to-physical memory address translation.

The RSIP-AES has the following features:

- The whole or part of Flash can be decrypted.
- Encrypted Flash data is decrypted by the hardware engine on the fly.
- Optional crypto algorithm: AES-256 CTR mode, XTS mode and GCM mode (GCM support different tag length).
- Key length is 256 bits, which should be programmed into OTP, and can be set to Read Protection and Write Protection.
- IV length is 128 bits, the higher 64 bits can be defined by users, and the lower 64 bits are decided by the address.
- Support four OTP keys. Keys are auto-loaded to the hardware engine; software cannot access them after read protection is enabled.
- Keeps eight IVs in the engine, and each of the eight entries can choose a different IV and mode independently to enable decryption for specific areas.

7.9.5 Read Protection (RDP)

Read Protection (RDP) is used to protect security-critical code, which is implemented with Arm TrustZone technology. The security-critical code is stored in the Flash with encrypted form. It would be decrypted by RSIP in secure bootloader and loaded into secure SRAM or XiP, protected by TrustZone. The RSIP has two different sets of OTP keys. Secure and non-secure images can use different OTP keys to ensure the security of the TrustZone image.



7.9.6 True Random Number Generator (TRNG)

The True Random Number Generator (TRNG) can generate full-entropy 32-bit random data for application use. Its core components include a dynamic entropy source and an internal conditioning module. Adopting a physical entropy source design, fundamentally immune to side channel attacks. This module can pass NIST sts-2.1.2 randomness tests.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

It has the following features:

- Delivers 32-bit true random numbers, produced by a digital entropy source
- Embeds with a health test unit and an error management unit
- Includes a control bit to enable/disable access from the non-secure world.
- FIFO Resource Prioritization
  - FIFO_S: 256-bit capacity, high-priority filling (immediately refills when data < 128 bits to ensure secure world access even under malicious attacks).
  - FIFO_NS: 128-bit capacity, filling depends on remaining secure world data (enabled only when FIFO_S ≥ 128 bits).
- Throughput of the TRNG up to about 2Mbps.

7.10 Timers and Watchdogs

The RTL8721F includes four basic timers, one capture timer, four PWM timer, also two PMC timer groups, a RTC timer, a debug timer and four watchdog timers.

Table 7-4 Timer feature comparison

Type	Number	Counter resolution	Counter mode	Prescaler	INT generation	Sleep mode	Secure mode
Basic timer	4	32-bit	Up	×/6-bit	✓	✓	✓
Capture timer	1	16-bit	Up	16-bit	✓	×	×
PWM timer	4	16-bit	Up	16-bit	✓	×	×

7.10.1 Basic Timer (TIM0 ~ TIM3)

The RTL8721F has four basic timers: TIM0, TIM1, TIM2, TIM3. The clock source is SDM32kHz by default, and can be changed to XTAL1M.

The basic timers also can be used as generic timers for time-based generation.

All the basic timers support:

- Resolution: 32-bit
- Counter mode: up
- Interrupt generation
- Secure mode
- Wakeup from sleep mode

7.10.2 PWM Timer (TIM4 ~ TIM7)

The RTL8721F has four pulse width modulation (PWM) timer (TIM4 ~ TIM7), which is a special timer to generate PWM output waveform and synchronize the multiple PWM output. Pulse lengths and waveform periods can be modulated from a few microseconds to several seconds using the timer prescaler.

The PWM timer supports:

- Channel: 4
- Clock source: XTAL40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- One pulse mode with configurable default level and trigger edge
- PWM mode with polarity selection
- Interrupt generation
- Duty cycle: 0% ~ 100%
- Phase shift
- Secure mode

7.10.3 Capture Timer (TIM8)

The RTL8721F has one capture timer (TIM8), which can be used for a variety of purposes, including measuring the input signal pulse width or number of input signals.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

The capture timer supports:
- Clock source: XTAL40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- Statistic pulse width
- Statistic pulse number
- Secure mode

7.10.4 PMC Timer

The RTL8721F has two PMC timer groups. One PMC timer group contains 4 timers inside, all for internal usage. They are used for different purposes in power saving flow internally, such as used for maintaining system active time or setting system sleep time.

The PMC timer has the following features:
- Clock source: SDM32kHz
- Counter mode: down
- Resolution: 32-bit
- Interrupt generation
- Wake up from sleep mode

7.10.5 Real-time Clock (RTC) Timer

The RTC timer is an independent binary coded decimal (BCD) timer/counter. One 32-bit register contains the seconds, minutes, hours (12- or 24-hour format) expressed in BCD format. One 32-bit register contains the days expressed in binary format. One 8-bit register contains the years expressed in binary format. It usually updates the calendar at 1Hz.

The RTC timer provides a set of continuously running counters in the RTC domain to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or watchdog reset, or when the device wakes up from sleep or deep-sleep mode.

The RTC supports:
- Prescaler: 9-bit asynchronous prescaler and 9-bit synchronous prescaler
- Time with seconds, minutes, hours (12- or 24-hour format) days and years
- Daylight saving compensation programmable by software
- One programmable alarm with interrupt function. The alarm can be triggered by any combination of the time fields.
- Maskable interrupt/event:
  - Alarm
  - Day threshold
  - Wakeup timer
- Digital calibration circuit
- Register write protection
- Periodic auto-wakeup
- A digital calibration to compensate for some deviation
- Keeps running as long as the supply voltage remains in the operating range

The RTC timer of RTL8721F is powered by the VAH_RTC pin, which is only available on some packages (refer to *Pin Assignments* for detailed information). While on other packages, the VAH_RTC pin is internally bonded with other power pins within the chip.
- For packages with VAH_RTC pin, VAH_RTC pin can be independently connected to the external power supply. Therefore, when all other power pins of the system are powered off but VAH_RTC pin remains powered, the RTC timer can still work normally.
- For other packages, the RTC function can only be used when all power supplies of the system are normal.

When the system boots up, the clock source of RTC timer is from SDM32K. After calibrating the internal XTAL, the RTC module's deviation is less than 2s per 24 hours (typical value).

7.10.6 Debug Timer

Debug timer is a common timestamp for all debug messages originating from all on-die processors and processor execution domains (application, kernel and firmware). It also includes a lock-free increment counter. It features:
- A simple 64-bit wrap timer

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

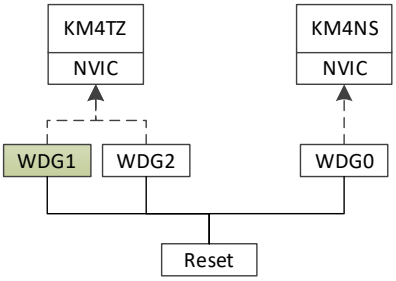
- A lock-free counter

The counter is enabled by default. The counter wraps around to zero and continues to count once it reaches 32'hFFFFFFFF. A write to the timestamp will set the current value of it, however, it must continue to increment at the base of the new setting value if the writing happens when the counter is active.

The debug timer has two types of clock sources: XTAL and internal 32K. The XTAL clock may be gated in sleep mode. If users select XTAL as the clock source in sleep mode, the debug timer will stop counting, and all the registers will be maintained. The counter will resume the increment immediately after XTAL resumes. Users can select 32K as the clock source in sleep mode; however, the counter itself needs 220us to switch the clock before continuing counting. In this period, writing to this IP is not allowed. All the registers will be reset to the initial values after wakeup from deep-sleep mode.

7.10.7 Watchdog Timer

The RTL8721F includes three system watchdog timers (WDG).
- WDG0: a watchdog timer for KM4NS
- WDG1: a secure watchdog timer for KM4TZ
- WDG2: a non-secure watchdog timer for KM4TZ



All the watchdog timers can trigger the reset of the corresponding CPU or the whole system.

The power and clock of the system watchdog timer are protected by itself. Once the watchdog timer is enabled, the processor cannot shut off the watchdog timer's power and clock again. It features:
- An optional early interrupt can be generated at a programmable time prior to watchdog timeout
- Watchdog gates automatically when the processor is in debug mode
- Gates and maintains settings in sleep mode
- Window protection function and timeout cannot be changed anymore once WDG is enabled.
- A separate boot reason for each watchdog timer

7.11 Direct Memory Access Controller (DMAC)

The RTL8721F has a DMAC, which allows peripheral-to-memory, peripheral-to-peripheral, memory-to-peripheral, and memory-to-memory transactions without the participation of CPU. Each DMA stream provides unidirectional DMA transfers for a single source and destination. It features:
- Up to eight independent channels, with programmable priority
- FIFO per channel for source and destination
- Programmable flow control at block transfer level (source, destination or DMAC)
- Programmable source and destination for each channel
- Transaction: supports single and burst transaction mode
- DMA transfer: supports single-block and multi-block transfer
- Secure mode supports secure transfer mode
- Power save: support DMAC low power mode (internal clock gating)
- Supports for disabling channels without data loss
- Supports for suspension of DMA operation
- Support gather and scatter functions

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.12 Audio

The audio module is divided into two parts: DMIC interface and I2S. The functions and features are described below.

7.12.1 Digital Microphone (DMIC) Interface

The audio module integrates two DMIC interfaces.

- 8kHz/11.025kHz/12kHz/16kHz/22.5kHz/24kHz/32kHz/44.1kHz/48kHz/88.2kHz/96kHz for DMIC interface
- Configurable 0-5 band EQ
- Adjustable digital volume control
- For digital volume control, supports zero-crossing detection to minimize audible artifacts
- DC remove function

7.12.2 Inter-IC Sound (I2S)

The SPORT 0 include the following features:
- Supports up to 8-channel I2S transmitter by TDM or PCM mode
- Up to 4 serial data outputs/inputs are transmitted within a sample period (multi io)
- Audio data word length: 16/20/24/32 bits
- Channel length: 16/20/24/32 bits
- Works in master and slave mode
- In 2 channels mode, channel length=32 bits ,fs supports up to 192kHz
- LRCLK start and stop detection

7.13 Inter-Processor Communication (IPC)

The inter-processor communication (IPC) hardware is designed to make any two CPUs communicate with each other. The IPC provides a set of registers for each processor that facilitates inter-processor communication via interrupts. Interrupts may be independently masked by each processor to allow polled-mode operation.

The IPC communication data must be located in common memory. It features:
- Status signaling for the 32 channels (16 channels for Tx and 16 channels for Rx)
  - Channel empty/full flag, also used as a lock
- Four sets interrupt lines per processor
  - Two sets for Rx channel full (communication data posted by sending processors)
  - Two sets for Tx channel empty (communication data retrieved by receiving processors)
- Interrupt masking per channel
  - Channel Tx empty mask
  - Channel Rx full mask
- 64 hardware semaphores for the atomic operation of shared resources

7.14 Universal Serial Bus (USB) Interface

The RTL8721F integrates USB 2.0 controller with flexible host and device capabilities, delivers a high-speed, multi-functional and plug-and-play universal serial interface.

The USB interface supports the following features:
- Compatible with USB 2.0 specification:
  - Host / device mode
  - High-speed (480Mbps) / full-speed (12Mbps) / low-speed (1.5Mbps) mode
- Up to 8 endpoints with 12 addresses in device mode:
  - EP0 IN/OUT, for control transfer only
  - EP1 IN
  - EP2 IN/OUT
  - EP3 IN/OUT
  - EP4 IN
  - EP5 OUT

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- EP6 IN/OUT
- EP7 OUT

- Up to 12 channels in host mode
- Data FIFO depth 1024 with 35 bits width (32 data bits plus 3 control bits):
  - Data FIFO configurations in device mode:
    - Single shared Rx FIFO for all device OUT transfers, max. depth 1024
    - 6 dedicated Tx FIFO for device IN transfers, max. depth of each Tx FIFO:
      - Tx FIFO0: 32
      - Tx FIFO1: 16
      - Tx FIFO2: 256
      - Tx FIFO3: 32
      - Tx FIFO4: 256
      - Tx FIFO5: 128
  - Data FIFO configurations in host mode:
    - Single shared Rx FIFO for all host IN transfers, max. depth 1024
    - Single Non-periodic Tx FIFO for non-periodic host OUT transfers, max. depth 1024
    - Single Periodic Tx FIFO for periodic host OUT transfers, max. depth 1024
- DMA / slave mode
- Integrated UTMI+ PHY
- External hub connection support in host mode
- Automatic ping in host mode

7.15 Secure Digital Input and Output Salve (SDIO)

The SDIO device supports the following features:

- Full compliance with SDIO card specification version 2.0:
  - 1-bit and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
- Partial CCCR registers are configurable
- SDIO multi-function support:
  - Function 0: SDIO Wi-Fi function
  - Function 1: BT function
- Internal DMA supported
- Interrupt control
- 3.3V/1.8V operating voltage

7.16 Secure Digital Input and Output Host (SDH)

Three secure digital input/output Multi-Media Card interfaces (SDMMC) provide an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDH supports the following features:

- Full compliance with SD host controller specification version 2.0:
  - 1-bit mode and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
  - Multi-block read/write
- Internal DMA supported
- Interrupt control
- Operation mode:
  - Polling mode
  - Interrupt mode
  - DMA mode
- 3.3V/1.8V operating voltage

7.17 General-Purpose Input/Output (GPIO)

The GPIO supports the following features:

- Separate data register and data direction register for each signal
- Read back the data on external pads using memory-mapped registers.
- Independently controllable signal by bits

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- Interrupt mode for each pin
  - Level sensitive: active-high level or active-low level interrupt
  - Edge trigger: rising edge, falling edge or both edges
- Option to generate single or multiple interrupts
- Configurable de-bounce time up to 8ms to de-bounce interrupts
- Level interrupt synchronization

Each of the GPIO pins can be dynamically configured by software as output or input. GPIO pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Most of the GPIO pins are shared with digital or analog alternate functions.

7.18 LCD Controller (LCDC)

The RTL8721F integrates LCD Display Controller (LCDC) that delivers high configurability, supporting both standard RGB parallel interfaces and 8080 interface. The LCDC offers flexible, programmable display parameters and includes a built-in pixel format converter, allowing easy adaptation to a wide range of display panels and resolutions.

The LCDC supports the following features:

- Interface Support
  - RGB Parallel Interface supports multiple pixel output formats:
  - 6-bit RGB (RGB565); 8-bit RGB (RGB888); 16-bit RGB (RGB565); 24-bit RGB (RGB888)
  - 8080 Interface supports flexible pixel output format:
  - 8-bit RGB (RGB565); 8-bit RGB (RGB888); 16-bit RGB (RGB565); 24-bit RGB (RGB888)
- Comprehensive Timing Control for Panel Compatibility
- Programmable timing parameters for both RGB and 8080 interfaces:
  - RGB Interface
    - Timings: HSYNC width, VSYNC width, VBP, HBP, VFP, HFP
    - Polarity: HSYNC, VSYNC, Data Enable, Pixel clock
  - 8080 Interface
    - Timings: RD width, WR width, VSYNC period, TE delay
    - Polarity: RD, WR, RS, CS, TE, and VSYNC signal
- Integrated Pixel Format Converter
- Native conversion between multiple color formats, adapting various display module requirements seamlessly
- Panel Resolution
- Supports a wide range of panel resolutions

7.19 Pixel Processing Engine (PPE)

The Pixel Processing Engine (PPE) is designed to accelerate specific operations on rasterized image data through dedicated hardware. These operations mainly include pixel format conversion, image geometric transformation, multi-layer image blending, and color keying.

The PPE supports the following features:

- Configurable number of input layers (max. 3) and 1 result layer
- Suspend, resume, and abort
- XOR function
- Multi-frame mode
  - Auto-reload
  - Link list
- Interrupt mask/unmask, status, and clear
- Each input layer:
  - Supports configurable input image size
  - Supports different input sources:
    - From DMA
    - From constant pixel
  - Supports bilinear interpolation (2 x 2)
  - Supports Pixel Format Converter
  - Supports color key filter:
    - Inside mode
    - Outside mode
  - Supports configurable input image line length
  - Supports window output
  - Supports rotation with 90, 180, 270 degree

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- Result layer:
  - Supports configurable result image size
  - Supports configurable result image line length
  - Supports multiple pixel formats and format converter
  - Supports background blend

7.20 Motion Joint Photographic Experts Group (MJPEG)

The Motion Joint Photographic Experts Group (MJPEG) is composed of a JPEG decoder and a post-processing unit, the JPEG decoder and post-processing can operate independently (standalone mode) or collaboratively (combined mode). In standalone mode, the JPEG decoder decodes JPEG images into YCbCr format data, and the post-processing unit can process YCbCr format data and output it in YCbCr or RGB format. In combined mode, the data decoded by the JPEG decoder is directly sent to the post-processing unit for further processing.

The JPEG Decoder supports the following features:
- Baseline interleaved JPEG
- Input data format: YCbCr400, YCbCr420, YCbCr422, YCbCr440, YCbCr411, YCbCr444 sampling formats
- Output data format: YCbCr400, YCbCr420, YCbCr422, YCbCr440, YCbCr411, YCbCr444 in semi-planar raster-scan format
- Image size: 48 x 48 to 8176 x 8176
- Slice mode in standalone mode
- Input buffering mode

The Post-Processing supports the following features:
- Input data sources:
  - JPEG decoder (combined mode)
  - External memory (standalone mode)
- Rotation:
  - 90, 180, 270 degree rotation in standalone mode
  - Horizontal and vertical flip
- Input data formats:
  - Any format generated by the JPEG decoder
  - In standalone mode:
    - YCbCr 4:2:0 semi-planar raster-scan
    - YCbCr 4:2:0 semi-planar tiled (16x16)
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2, YCrYCb 4:2:2
    - CbYCrY 4:2:2, CrYCbY 4:2:2
- Output data formats:
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2 raster-scan or 4x4 tiled
  - YCrYCb 4:2:2 raster-scan or 4x4 tiled
  - CbYCrY 4:2:2 raster-scan or 4x4 tiled
  - CrYCbY 4:2:2 raster-scan or 4x4 tiled
  - Fully configurable ARGB channel lengths and positions within 32-bit output or 16-bit output, e.g., ARGB 32-bit (8-8-8-8), RGB 16-bit (5-6-5), ARGB 16-bit (4-4-4-4). Alpha channel is programmable
- Input image size:
  - 48x48 to 8176x8176
  - Step size: 16 pixels
- Output image size:
  - 16x16 to 4096x4096
  - Horizontal step size: 8 pixels
  - Vertical step size: 2 pixels
- Scaling in the same direction:
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Maximum upscaling ratio 3 and unlimited downscaling ratio
- YCbCr to RGB color conversion:
  - BT.601-5 compliant
  - BT.709 compliant
  - User-definable conversion coefficients
- 2 x 2 ordered spatial dithering for 4-, 5-, and 6-bit RGB channel precision
- Alpha blending:
  - Output image can be alpha blend with 2 rectangular
  - Supported overlay input formats:

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

  - alpha value + YCbCr 4:4:4, 8 bits each
  - 8-bit alpha value + 24-bit RGB
- RGB image contrast/brightness/saturation adjustment
- Image cropping
- Picture-in-picture
- Output image masking: Output image writing can be prevented on two rectangular areas in the image.

7.21 A2C

The RTL8721F has two independent A2C modules. Each A2C includes a part of memory logic for flexible message transmission and reception, which can ease the CPU loading and be more efficiency.

Each A2C has the following features:
- Compatible with ISO11898-1 (CAN specification 2.0)
- Configurable 3 sample points for better robustness
- Configurable auto re-transmission
- Time-stamp recorded in Tx/Rx
- Event generation (or Time-trigger message) in Tx
- Auto reply for remote message in Tx/Rx
- Configurable DMA function in Rx
- Up to 16 buffers to store message for easing CPU loading
- Configurable space size and direction (Tx or Rx) for each buffer
- Configurable FIFO mode for the upper 4 buffers
- Low power wakeup function with digital filter
- Loop back mode and Silence mode for debug
- Multiple interrupts for error detection
- Warning function when error counter larger than threshold (default 96)

7.22 Ethernet MAC

The Ethernet MAC (ETH MAC) module supports interface interaction with the physical layer (PHY), controls the transmission and reception of data frames, and complies with the standard Ethernet protocol rules (IEEE 802.3). It can communicate with external Ethernet PHY through RMII interface.

The Ethernet MAC supports the following features:
- Supports RMII as the MAC-side interface
- Supports half-duplex/full-duplex modes at 10Mbps/100Mbps
- Supports the CSMA/CD (Carrier Sense Multiple Access with Collision Detection) protocol for half-duplex mode
- Supports IEEE 802.3x flow control for full-duplex mode
- Supports both PHY mode and MAC mode
- Supports two operating modes for MDIO: master mode and slave mode
- Supports EEE (Energy Efficient Ethernet) functionality
- Supports outputting a clock source (25MHz/50MHz) to the PHY, which can save XTAL for PHY
- Supports the configuration and management of PHY devices using the MDC/MDIO interface
- Automatically obtain and synchronize the speed and duplex of PHY after Auto-negotiation through MDC/MDIO

7.23 Inter-integrated Circuit Interface (I2C)

The RTL8721F embeds two I2C interfaces (I2C0, I2C1), which handle communications between the RTL8721F and the serial I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing. The design of RTL8721F I2C aims at sensor-hub applications in low-power or battery-powered productions. Essential features of the I2C bus protocol should be provided for acquiring or controlling external sensor data.

The I2C interface supports:
- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three-speed modes
  - Standard Speed, up to 100Kbps
  - Fast Speed, up to 400Kbps
  - High Speed, up to 3.4Mbps
- Master or Slave I2C operation

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- Transmitter or Receiver
- Transmit and receive FIFOs with a depth of 16 and a width of 12-bit
- DMA interface for DMA transfer
- Multi-master ability including bus arbitration scheme
- Clock stretch in master/slave mode
- 7-bit or 10-bit addressing mode, 7-bit or 10-bit combined format transfer
- Manual START/RESTART/STOP bit control
- Supports General Call, NULL DATA, START BYTE transfer protocol
- Component parameters for configurable software driver support (programmable SDA hold time, slave address, SCL duty cycle, etc.)
- Filter to eliminate the glitches on signals of SDA and SCL, programmable digital noise filter
- Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)
- Slave Mode Dual Own Address
  - Slave 1 supports 7-bit or 10-bit address mode
  - Slave 2 only supports 7-bit address mode
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

7.24 Inter-integrated Circuit like (I2C-like) Interface

This simplified I2C variant is designed specifically for unidirectional (transmit-only) communication with special I2C device. It operates exclusively in master mode and omits slave acknowledgment (ACK/NACK) and slave address confirmation mechanisms.

Key features:
- Interface: standard two-wire (SDA, SCL)
- Supported speeds: 100kbps, 400kbps, 1Mbps
- Maximum payload: 127 bytes per transmission
- Power domain: resides in the AON (Always-On) domain within the SYSON (System-On) domain, and retains state during software, watchdog, or system reset

7.25 Universal Asynchronous Receiver/Transmitter (UART, LOGUART)

The UART offers a flexible means of full-duplex data exchange with external equipment, requiring an industry-standard NRZ asynchronous serial data format. It provides a very wide range of baud rates using a fractional baud rate generator. Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

7.25.1 UART0 ~ UART3

Except the LOGUART, the RTL8721F has embedded four general UART interfaces:
- UART0: 4-wire
- UART1: 2-wire
- UART2: 2-wire
- UART3: 4-wire, reserved to control BT HCI UART. If BT function is not enabled, UART3 can be used as normal UART.

These UARTs have the following features:
- Various UART formats: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Fractional baud rate:
  - Up to 8Mbps within high-speed mode (XTAL 40MHz)
  - Up to 115.2kbps within low-power mode (OSC 2MHz)
- Separated clocks for Tx path and Rx path
  - Tx path: XTAL 40MHz
  - Rx path: XTAL 40MHz, OSC 2MHz
- 11-bit * 16 asynchronous Transmit FIFO
- 11-bit * 64 asynchronous Receive FIFO
- Configurable auto-flow control
- Interrupt control and error detection
- IrDA (SIR mode) encoder and decoder module
- Loop-back mode for test
- Low power mode for Rx path

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

- Monitor and elimination of Rx baud rate error and own frequency drift automatically for Rx path
- UART Rx timeout mechanism
- DMA interface for DMA transfer
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

7.25.2 LOGUART

The RTL8721F has one LOGUART, which is responsible for printing logs. It can print logs from four sources at the same time without disordered logs, also it can receive commands for CPU to process.

The LOGUART features:
- Clock source: XTAL40M, OSC2M
- Follows UART protocol
- Various UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Up to 3Mbps baud rate for fast log printing
- Fractional baud rate
- Monitor function to eliminate Rx baud rate error and own frequency drift automatically for Rx path
- DMA interface for DMA TRx transfer
- Four Tx ports for multi-core or multi-function to print log, which are KM4TZ CPU, KM4NS CPU, Bluetooth, and Bluetooth firmware
- Supports UART relay function, Bluetooth firmware log of UART protocol from other SoC can be relayed by this IP to print out through one Tx port
- Hardware arbitration for Tx ports so that all Tx ports can print log concurrently without disordered log
- Independent open and close for four Tx ports
- Tx AGG supported, hardware adds AGG header automatically so that console can separate logs from different Tx ports
- Wakes up the system when the clock source is open during sleep mode

7.26 Serial Peripheral Interface (SPI)

The RTL8721F features up to two SPIs (SPI0, SPI1) that allow communication at up to 50Mbps in master and slave modes, in half-duplex, full-duplex and simplex modes. All SPI interfaces support 64 x 16-bit embedded Rx and Tx FIFOs with DMA capability.

The SPI has the following features:
- Supports Motorola SPI Serial interface operation
- Master and slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps
  - Dedicated zone:
    - SPI master: supports up to 50MHz
    - SPI slave: supports up to 25MHz (If the master supports sample delay, the SPI slave can theoretically reach up to 50MHz.)
  - Full-matrix zone:
    - SPI master: supports up to 25MHz
    - SPI slave: supports up to 12.5MHz (If the master supports sample delay, the SPI slave can theoretically reach up to 25MHz.)
- DMA interface for DMA transfer
- Independent masking of interrupts
- The Transmit and Receive FIFO buffers are 64 words in depth. The FIFO width is fixed at 16 bits.
- Hardware/Software slave-select
  - Dedicated hardware slave-select lines
  - Software control to select target serial-slave device
- Programmable features:
  - Clock bit-rate – Dynamic control of the serial bit rate of the data transfer, only when configured in Master Mode.
  - Data frame size (4 to 16 bits) – Frame size of each data transfer under the control of the programmer.
  - Configurable clock polarity and phase
  - Programmable delay sample time of the received serial data bit (rxd), when configured in Master Mode
- Transfer mode:
  - Transmit and receive
  - Transmit only
  - Receive only
- Operation mode:
  - Polling mode

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

  - Interrupt mode
  - DMA mode
- CS force control:
  - CS remains low during the whole data transfer, regardless of Tx FIFO underrun
  - SPI transmission pauses (SCLK halts) if Tx FIFO is empty before all data is sent, but CS stays low
  - Transmission resumes when new data is written to the Tx FIFO
  - CS is automatically released only after all calculated data bits are transmitted

7.27 Infrared Radiation (IR)

The RTL8721F embeds one infrared radiation (IR).

The IR is mainly designed to process IR signals with carrier frequency under 250kHz. The hardware IP supports hardware modulation which can be used on the IR Tx transmission. It also can detect the period of a continuous high/low level signal, and record in Rx FIFO, and then the software can recognize a received IR signal serial and process it. IR module works in Half-duplex mode.

It supports the following features:
- Half-duplex mode
  - Tx mode: carrier frequency range is from 25kHz to 250KHz
  - Rx mode: maximum sample frequency is 40MHz
- 32*4 bytes FIFO depth
  - Tx FIFO: Tx carrier symbol count and Tx data state
  - Rx FIFO: Rx data Level and Rx data count
- Customizable carrier duty by users
- Tx Compensation Mechanism
- Optional to modulate space symbol to carrier symbol
- IR receiver front can be IR receiver module or IR diode
- IR Rx glitch filter from 25ns to 225ns
- Operation mode:
  - Interrupt mode
  - Polling mode

7.28 General Purpose Analog-to-Digital Converter (ADC)

The RTL8721F integrates a 12-bit successive-approximation register (SAR) ADC, which provides a solution for collecting analog sensor and system power-consumption data with a low-power requirement. Various operation modes, for instance, auto mode, timer-trigger mode, and software-trigger mode, are adopted according to different using strategies.

It has the following features:
- Resolution: 12-bit SAR
- Single-ended input
- Available channel number
  - 8 external channels
  - 4 internal channels
- Built-in calibration
- Wide input voltage range: 0 ~3.3V
- Configurable ADC clock source
- Configurable channel switch order and channel number
- Individual channel compare mode
- Multi-sampling trigger sources
  - Software
  - Timer
- Manual and auto mode conversion
  - Manual mode for software-controllable conversion
  - Auto mode for hardware continuous conversion
- Hardware oversample for higher SNR

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

7.29 Cap-Touch Controller (CTC)

Self-capacitance touch controller measures the capacitance between the capacitive sensor pin and ground. The capacitive touch controller detects the presence of a finger through capacitance changes.

It has the following features:

- 9 capacitive sensor channels:
  - Detection of finger touch
  - Programmable enable/disable for each channel
  - Adjustable sensitivity for each channel
  - Adjustable touch threshold for each channel
- Automatic channel scan: hardware scans each enabled channel automatically in sequence
- Programmable scan period: sample number and scan interval
- Configurable sample clock
- Active noise immunity:
  - Supports SNR information monitor
  - Adjustable environmental noise threshold for each channel
  - Enhanced noise filter for higher SNR
- Automatic environment tracking and calibration (ETC)
  - Automatic hardware baseline initialization
  - Automatic baseline and threshold update for different noise environments
  - Programmable ETC update step and factor
- Programmable button debounce function
- Interrupt control:
  - Programmable interrupt enabled for each interrupt source
  - Software readable interrupt status and raw status register

7.30 Thermal Sensor

The RTL8721F device embeds a thermal sensor to monitor the temperature inside the chip. This thermal sensor has a good linearity and is calibration-free. It provides low-temperature warning, high-temperature warning and over-temperature protection.

- When the temperature exceeds the limit high-temperature threshold, an interrupt will be sent to the CPU.
- When the temperature exceeds the limit low-temperature threshold, an interrupt will be sent to the CPU.
- When the temperature exceeds the limit over-temperature protection threshold, hardware will automatically trigger a thermal reset for over-temperature protection. After a thermal reset, the chip will stay in reset mode for about 500 ms, then it checks the temperature. If the temperature is below the default over-temperature threshold (125°C), the system boots normally. Otherwise, it waits another 500ms and checks again.

It has the following features:

- Measurement range: -45°C ~ 125°C
- Variation: ±1.5°C (typical), ±5°C (worst)
- Independent configuration for temperature warning and over-temperature protection functions including enable control and detection temperature

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

8 Power Sequence

The recommended power-on and power-off sequences are depicted in the following sections. The VDH_x/VAH_x/VRH_x and CHIP_EN are powered and controlled by external power sources. Other used voltages are recommended to be powered by the embedded regulator or LDO.

NOTE

The VDH_x/VAH_x/VRH_x refers to typical 3.3V power supply including VAH_DCDC, VAH_LDOM, VAH_ADC, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, and VDH_IO2. The VDH_IO0 and VDH_IO1 can be powered by typical 3.3V or 1.8V, and should be stable before the corresponding I/Os normal operation.

The parameter specification of power sequence is listed in *Table 8-1*.

Table 8-1 Power sequence specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{NORMAL}	VDH_x/VAH_x/VRH_x normal operation voltage	2.97	3.3	3.63	V
V_{POR_H}	Power on reset high level	1.9	2.1	2.7	V
V_{POR_L}	Power on reset low level	0.5	1.6	1.9	V
V_{IL}	CHIP_EN input low voltage			0.35*V_{NORMAL}	V
V_{IH}	CHIP_EN input high voltage	0.65*V_{NORMAL}			V
T_R	VDH_x/VAH_x/VRH_x rising time	0.1			ms
T_{READY}	VDH_x/VAH_x/VRH_x ready time after POR			3.2	ms
T_F	VDH_x/VAH_x/VRH_x falling time	0.1			ms
T_{CORE}	Core power on time		4.8[1]		ms
T_{TM}	Test mode trap time	0		4	ms
T_{UD}	UART download mode trap time	0		5	ms
T_{BOOT_NOR}	Boot from NOR flash trap time	0		5	ms
T_{PD_LOW}	VDH_x/VAH_x/VRH_x power down low voltage last time	0.3			ms
T_{DBC_CHIPEN}	CHIP_EN default debounce time	0.06	0.1	0.2	ms
T_{RST_CHIPEN}	CHIP_EN low voltage last time	0.1			ms

NOTE

[1] T_{CORE} is characterized under 3.3V power supply and 25°C.

8.1 Power-on Sequence

During power-on, VDH_x/VAH_x/VRH_x must rise monotonously. When VDH_x/VAH_x/VRH_x exceeds V_{POR_H} and CHIP_EN is high, the chip releases its internal reset and starts to boot. VDH_x/VAH_x/VRH_x must rise up to V_{NORMAL} within T_{READY}. There is no restriction that CHIP_EN is pulled up earlier than, later than, or simultaneously with VDH_x/VAH_x/VRH_x.

- T_{CORE}: after internal reset release, embedded DCDC/LDOC will start to output core power for VDL_CORE.
- T_{TM}: after internal reset release, the IC will get the state of PA3/TM_DIS.
  - When PA3/TM_DIS is high, the IC will enter normal mode.
  - When PA3/TM_DIS is low, the IC will enter test mode (only for internal test, user access prohibited).
- T_{UD}: during the period immediately following the core power ready, the chip samples the voltage level on the PB20/UD_DIS pin. Please keep the pin on a proper voltage level stably before the end of the T_{UD} period.
  - When PB20/UD_DIS is high, the IC will enter normal boot mode.
  - When PB20/UD_DIS is low, the IC will enter UART download mode.
- T_{BOOT_NOR}: after LDOC core power output, the IC will get the state of PB18/BOOT_NOR.
  - When PB18/BOOT_NOR is high, it indicates that the external Flash is NOR Flash.
  - When PB18/BOOT_NOR is low, it indicates that the external Flash is NAND Flash.
  - T_{BOOT_NOR} is only valid for part numbers with embedded PSRAM. For other part numbers, the IC will ignore the state of PB18/BOOT_NOR during power on, and always treat the internal or external Flash as NOR flash.

All these trap pins are latched only once during the first power-on sequence, including POR and CHIP_EN reset.

During normal power-on sequence, the pull-up resistors of these trap pins will be enabled first, and then the input level status of these pins will be latched. When these trap pins are left floating without external driving, all of them will be trapped as high level, and the chip will enter normal mode and treat the Flash as NOR Flash.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

If the chip has external drivers for these trap pins, the safe approach is to ensure that the level status of them is correctly driven within the specified time to avoid entering an unexpected mode.

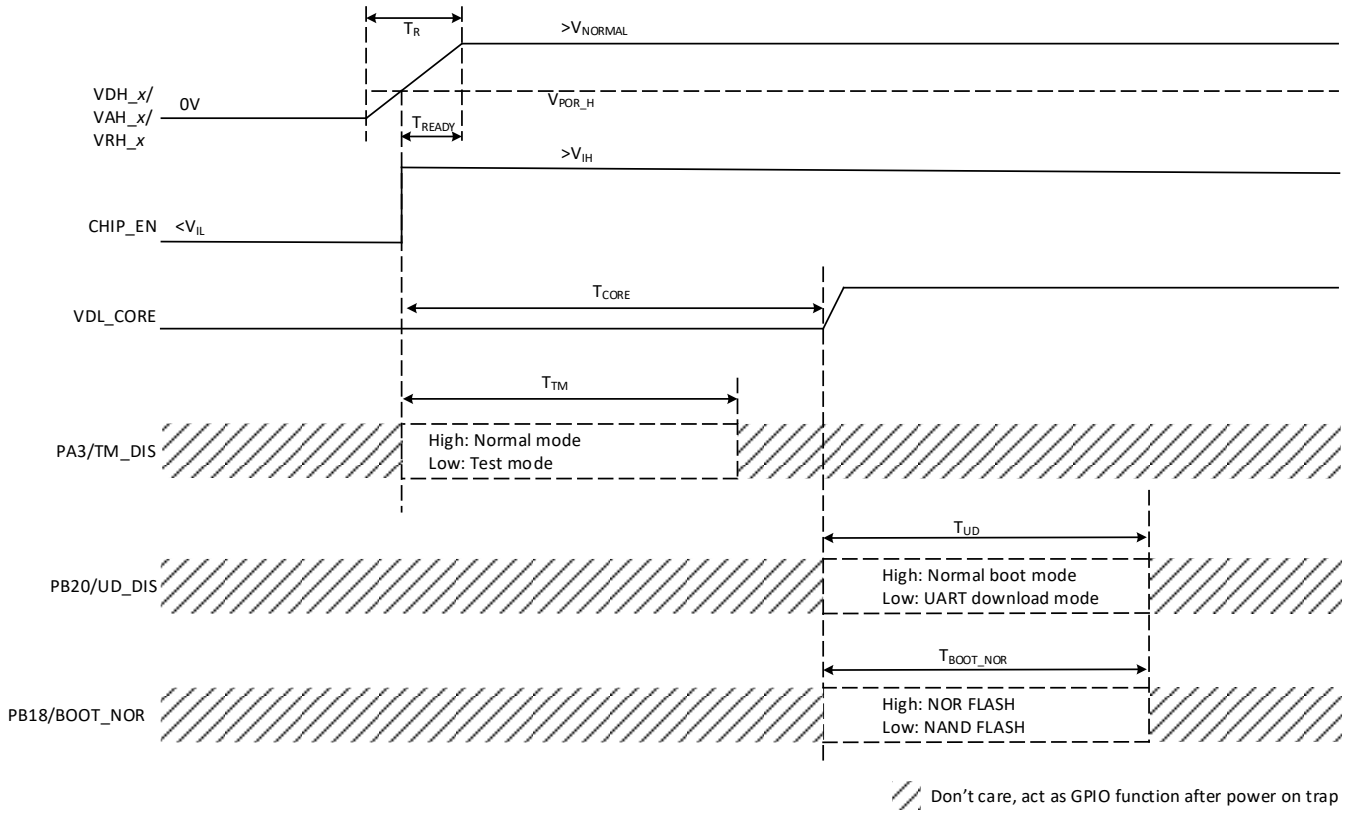


Figure 8-1 Power-on sequence

8.2 Power-off Sequence

In the process of power-off, VDH_x/VAH_x/VRH_x must drop down below V_{POR_L} and lasts for at least T_{PD_LOW} before it can be boosted and the IC can be powered on again. Any voltage between V_{NORMAL} and V_{POR_L} may not trigger a reset, and it may cause the IC to work abnormally.

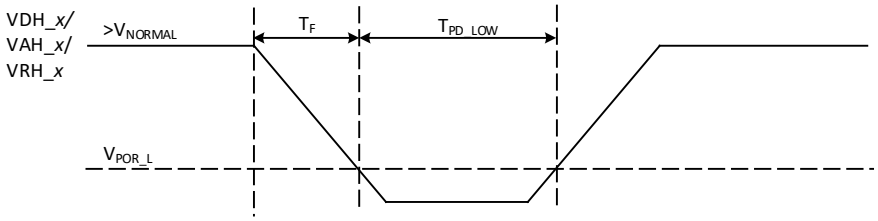


Figure 8-2 Power-off sequence

During power off, between V_{NORMAL} and V_{POR_L}, the normal operation of the IC cannot be fully guaranteed. During this period, abnormal operation may cause peripheral errors, such as unexpected destruction of the flash storage content. Therefore, it is recommended to speed up power-off time. It is also recommended to enable BOD reset function, which can turn off all IO outputs at a higher threshold voltage to avoid abnormal peripheral operations outside of the normal operating voltage range.

8.3 CHIP_EN Reset Sequence

When using the CHIP_EN as normal reset function, the expected debounce time can be set, ranging from 0us to 16ms. This time may vary from 66% to 200% under different conditions, such as different voltage, temperature, etc. When reset, the pull-down time must be T_{RST_CHIPEN} more than debounce time, and the variation of debounce time needs to be taken into consideration.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

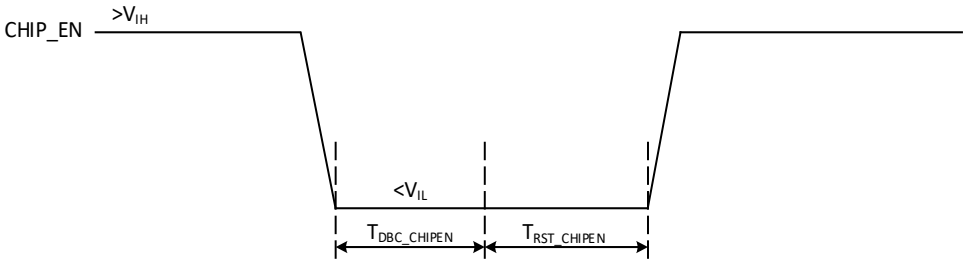


Figure 8-3 CHIP_EN reset sequence

8.4 BOD Reset Sequence

The BOD function is enabled in reset mode by default and can be disabled or switch to interrupt after power on.

When BOD is enabled in reset mode, it will monitor VAH_LDOM power supply input. When VAH_LDOM drops below V_{BOR_L}, it will trigger a BOR reset. All I/O outputs will also be turn off. When VAH_LDOM voltage rises again above V_{BOR_H}, BOR reset will be released.

NOTE

The trap pins including PA3/TM_DIS, PB20/UD and PB18/BOOT_NOR will not be latched again during the BOD reset process.

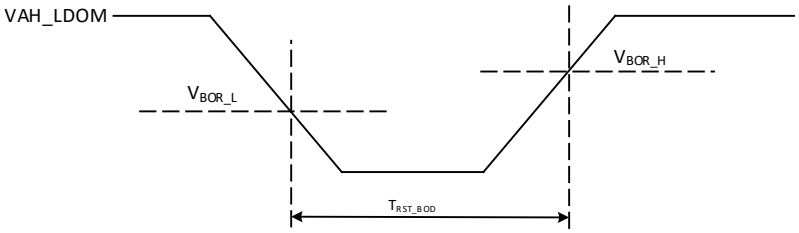


Figure 8-4 BOD reset sequence

When VAH_LDOM drop below max. of V_{POR_L}, it may trigger a POR reset, the subsequent sequence needs to refer to power-on and power-off sequence.

V_{BOR_L} and V_{BOR_H} can be adjusted separately. The parameters given in *Table 8-2* are derived from the test under ambient operating temperature.

Table 8-2 Embedded BOD threshold characteristics

Symbol	Parameter	Configuration	Min.	Typ.	Max.	Unit
T_{RST_BOD}	BOD reset voltage low last time		1			ms
V_{BOD_L} & V_{BOD_H}	Brownout detection threshold	BOD_THRESHOLD1		2.84		V
		BOD_THRESHOLD2		2.80		V
		BOD_THRESHOLD3		2.77		V
		BOD_THRESHOLD4		2.73		V
		BOD_THRESHOLD5 (default rising setting)		2.69		V
		BOD_THRESHOLD6		2.63		V
		BOD_THRESHOLD7		2.59		V
		BOD_THRESHOLD8 (default falling setting)		2.55		V
		BOD_THRESHOLD9		2.51		V
		BOD_THRESHOLD10		2.47		V

NOTE

- *V_{BOD_H} needs to be set higher than V_{BOD_L}.*
- *It is recommended to reserve about 100mV or higher hysteresis window between V_{BOD_H} and V_{BOD_L}.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9 Electrical Characteristics

9.1 Parameters Definitions

9.1.1 Maximum and Minimum Values

Unless otherwise specified, all data are guaranteed by design, simulation and samples test to be applicable to all declared temperature, voltage ranges and processes, and are not tested in production.

9.1.2 Typical Values

Unless otherwise specified, the typical values are reference results when the IC is at a junction temperature of 25 degrees Celsius and an operating voltage of 3.3V. This value is for reference design only and not actually tested.

9.1.3 Pin Status

9.1.3.1 Loading Capacitor

Unless otherwise specified, the load refers to the equivalent capacitance mounted on the chip pin. Schematic diagrams used for loading capacitor measurements is illustrated in *Figure 9-1*.

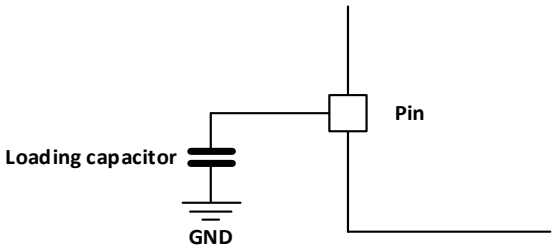


Figure 9-1 Loading capacitor diagram of pin

9.1.3.2 Input Voltage

Unless otherwise specified, the input voltage of the chip pin refers to the voltage difference between the pin and ground. The schematic diagram is illustrated in *Figure 9-2*.

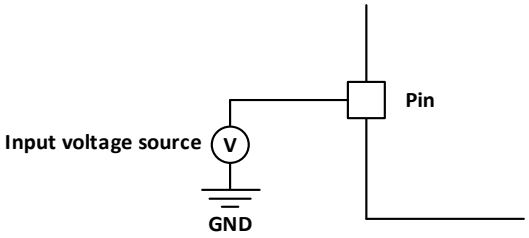


Figure 9-2 Input voltage diagram of pin

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9.2 Absolute Maximum Ratings

Stresses beyond absolute maximum ratings may cause permanent damage to the device. These are emphasized ratings only and do not address functional operation of the device.

Table 9-1 Absolute maximum ratings

Symbol	Description	Condition	Min.	Max.	Unit
VAH_DCDC, VAH_LDOM, VAH_RTC, VAH_ADC, VDH_IO0, VDH_IO1, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VDH_IO2, VDH_FLASH	External supply voltage	Input DC voltage at power pin	-0.3	3.63	V
V_{IN}	Input voltage on PA*x*/PB*x*/PC*x* pins	Input DC voltage at digital I/O pin, VDH_IO*x*≤3.63V	-0.3	VDH_IO*x*+0.3	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin			dBm
T_{STORE}	Storage temperature range		-65	150	°C
MSL	Moisture Sensitivity Level				
HBM	ESD Human Body Model	T_A=25°C, conforming to JESD22-A114F			
CDM	ESD Charged Device Model	T_A=25°C, conforming to JESD22-C101F			

9.3 Operation Conditions

Table 9-2 Recommended operation conditions

Symbol	Condition		Min.	Typ.	Max.	Unit
VAH_DCDC, VAH_LDOM, VAH_ADC, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VDH_IO2, VDH_FLASH[1]	Normal operation voltage		2.97	3.3	3.63	V
	Voltage ripple				+/-100	mV
VDH_IO0, VDH_IO1[2]			1.62	1.8/3.3	3.63	V
VAH_RTC			1.3[3]	3.3	3.63	V
LDOM_OUT			1.7	1.8	1.95	V
VRM_RF, VRM_SYN, VAM_XTAL, VAM_LDOC, VDM_PSRAM	Active mode		1.2	1.25/1.35	1.45	V
	Sleep mode		0.65	0.7/0.8	0.9	V
VAL_USB, VDL_CORE, LDOC_OUT	Active mode		0.85	0.9/1.0	1.05	V
	Sleep mode		0.65	0.7/0.8	0.9	V
T_A	Ambient operating temperature	Standard temperature IC	-20		+85	°C
		Wide-range temperature IC	-40		105	
$T_J$max.	Maximum Junction temperature[4][5]		-	-	+125	°C

CAUTION

[1] All these power pins must be powered by the same voltage. For IC's stable performance, the voltage ripple on these pins is suggested to be under +/-100mV.

[2] The voltage for VDH_IO1 and VDH_IO2 needs to be not higher than the voltage for VAH_LDOM.

[3] The VAH_RTC voltage needs to be higher than 2.97V during first power-on. After initialization is completed, the RTC can work normally before the VAH_RTC voltage drops to 1.3V.

[4] The junction temperature must not exceed $T_J$max in all T_A ranges. When T_A is high and the power consumption of device is also high, a well-designed thermal management should be implemented to the board system to guarantee proper T_J. Please refer to Thermal Characteristics to estimate T_J.

[5] The IC must not operate at junction temperature of 125°C for extended periods of time.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9.4 Embedded Regulators Characteristics

The characteristics of embedded regulators including LDOC, DCDC, and LDOM are guaranteed by design.

Table 9-3 Embedded regulators characteristics

Regulators	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LDOC	V_{IN}	Input voltage range	LDO mode	1.2	1.25/1.35	1.45	V
			Bypass mode	0.65	0.7/0.8	0.9	
	V_{OUT}	Output voltage range	LDO mode	0.85	0.9/1.0	1.05	V
DCDC	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		0.6	1.25/1.35	1.45	V
	F	Switching frequency	PWM mode		2		MHz
LDOM	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		1.7	1.8	1.95	V
	I_{LOAD}[1]	Extra load beside embedded PSRAM	System in active mode			10	mA

NOTE

[1] Beyond powering embedded PSRAM, LDOM can also supply supplementary current for other circuits, such as 1.8V-powered I/O circuits. Note that the supplementary current can only be guaranteed when the system is in active mode.

9.5 Crystal Characteristics

The RTL8721F has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.

Table 9-4 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

9.6 I/O Pin Characteristics (TBD)

This section applies when GPIO is used as a digital function, but not used as an analog function.

Table 9-5 Output/input voltage level of I/O ports

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	V_{IO}[1]=1.8V±10%				V
		V_{IO}=3.3V±10%				
V_{IH}	I/O input high level voltage	V_{IO}=1.8V±10%				
		V_{IO}=3.3V±10%				
V_{OL}[2]	I/O output low level voltage	V_{IO}=1.8V±10%, I_{OL} max.[2]				
		V_{IO}=3.3V±10%, I_{OL} max.				
V_{OH}[2]	I/O output high level voltage	V_{IO}=1.8V±10%, I_{OL} max.		-	-	
		V_{IO}=3.3V±10%, I_{OL} max.		-	-	
I_{IN}	I/O input leakage current					nA

NOTE

[1] V_{IO} is the power supply for I/O pin.
[2] Refer to Table 9-6 for driving strength.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

All I/Os are listed in *Table 9-6*.

Table 9-6 I/O types

Pin name	I/O power pin	Driving (mA)[1]		Internal pull resistor (kΩ)[2]			Resistor available in deep-sleep mode[3]?
		1.8V (±10%)	3.3V (±10%)	Min.	Typ.	Max.	

9.7 RF Characteristics

9.7.1 WLAN Radio Specifications

This section describes the RF characteristics of WLAN 2.4GHz and 5GHz radios. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

NOTE

The WLAN radio performance values were measured in Lab environment using a Realtek EVB with the following conditions:

- *Room temperature: 25°C*
- *Typical voltage: 3.3V*
- *50ohm impedance load*

9.7.1.1 WLAN 2.4GHz Band Receiver Performance

Table 9-7 WLAN 2.4GHz band receiver performance

Parameter	Condition	Performance (3.3V)			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Rx Sensitivity 802.11b	1Mbps CCK		-99		dBm
	2Mbps CCK		-96		dBm
	5.5Mbps CCK		-93		dBm
	11Mbps CCK		-90		dBm
Rx Sensitivity 802.11g	BPSK rate 1/2, 6Mbps OFDM		-95		dBm
	BPSK rate 3/4, 9Mbps OFDM		-93		dBm
	QPSK rate 1/2, 12Mbps OFDM		-92		dBm
	QPSK rate 3/4, 18Mbps OFDM		-89.5		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-86		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-83		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-79		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-77.5		dBm
Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-94.5		dBm
	MCS 1, QPSK rate 1/2		-91.5		dBm
	MCS 2, QPSK rate 3/4		-89		dBm
	MCS 3, 16-QAM rate 1/2		-86		dBm
	MCS 4, 16-QAM rate 3/4		-82.5		dBm
	MCS 5, 64-QAM rate 2/3		-78.5		dBm
	MCS 6, 64-QAM rate 3/4		-77		dBm
	MCS 7, 64-QAM rate 5/6		-75.5		dBm
Rx Sensitivity 802.11ax BW = 20MHz	MCS 0, BPSK rate 1/2		-94.5		dBm
	MCS 1, QPSK rate 1/2		-91		dBm
	MCS 2, QPSK rate 3/4		-88.5		dBm
	MCS 3, 16-QAM rate 1/2		-85.5		dBm
	MCS 4, 16-QAM rate 3/4		-82.5		dBm
	MCS 5, 64-QAM rate 2/3		-78		dBm
	MCS 6, 64-QAM rate 3/4		-77		dBm
	MCS 7, 64-QAM rate 5/6		-75.5		dBm
	MCS 8, 256-QAM rate 3/4		-71.5		dBm
	MCS 9, 256-QAM rate 5/6		-69.5		dBm

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Max. Receive Level	6Mbps OFDM		0		dBm
	54Mbps OFDM		0		dBm
	11n, MCS 0, HT20		0		dBm
	11n, MCS 7, HT20		0		dBm
	11ax MCS 0 HE20		0		dBm
	11ax MCS 9 HE20		0		dBm
Adjacent Channel Rejection	11Mbps CCK		TBD		dB
	BPSK rate 1/2, 6Mbps OFDM		TBD		dB
	64-QAM rate 3/4, 54Mbps OFDM		TBD		dB
	HT20, MCS 0, BPSK rate 1/2		TBD		dB
	HT20, MCS 7, 64-QAM rate 5/6		TBD		dB
	HE20, MCS 0, BPSK rate 1/2		TBD		dB
	HE20, MCS 8, 256-QAM rate 3/4		TBD		dB
	HE20, MCS 9, 256-QAM rate 5/6		TBD		dB

9.7.1.2 WLAN 2.4GHz Band Transmitter Performance

Table 9-8 WLAN 2.4GHz band transmitter performance

Parameter	**Condition**	**Performance (3.3V)**			**Unit**
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK		20		dBm
	11Mbps CCK		20		dBm
	BPSK rate 1/2, 6Mbps OFDM		19		dBm
	64-QAM rate 3/4, 54Mbps OFDM		19		dBm
	HT20, MCS 0, BPSK rate 1/2		19		dBm
	HT20, MCS 7, 64-QAM rate 5/6		19		dBm
	HE20, MCS 8, 256-QAM rate 3/4		18		dBm
	HE20, MCS 9, 256-QAM rate 5/6		17		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM			-5	dB
	64-QAM rate 3/4, 54Mbps OFDM			-25	dB
	HT20, MCS 0, BPSK rate 1/2			-5	dB
	HT20, MCS 7, 64QAM rate 5/6			-27	dB
	HE20, MCS 8, 256-QAM rate 3/4			-30	dB
	HE20, MCS 9, 256-QAM rate 5/6			-32	dB
Output power variation	TSSI on across operating temperature range, all channels and VSWR≤1.5:1 at RFIO port	-1.5		1.5	dB
Carrier suppression				-32	dBc
Harmonic output power[2]	2nd harmonic		-19		dBm/MHz
	3rd harmonic		-21		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable. The output power is measured at RF connector on the Realtek EVB with an approximate 2.4GHz trace loss of 0.8dB. The actual Tx power may differ from the suggested power level due to PCB losses and national regulatory restrictions. Note that the mass production (MP) power may be lower than the values mentioned above. For further details, refer to the MP flow documentation.

[2] Harmonic output power is tested at IC port.

[3] Harmonic output power is measured at RF connector with diplexer and appropriate matching.

All information provided in this document is subject to legal disclaimers.

© REALTEK 2025. All rights reserved.

9.7.1.3 WLAN 5GHz Band Receiver Performance

Table 9-9 WLAN 5GHz band receiver performance

Parameter	Condition	Performance (3.3V)			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5885	MHz
Rx Sensitivity 802.11a	BPSK rate 1/2, 6Mbps OFDM		-94.5		dBm
	BPSK rate 3/4, 9Mbps OFDM		-92.5		dBm
	QPSK rate 1/2, 12Mbps OFDM		-91.5		dBm
	QPSK rate 3/4, 18Mbps OFDM		-89		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-86		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-82.5		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-78.5		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-77		dBm
Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-94		dBm
	MCS 1, QPSK rate 1/2		-91		dBm
	MCS 2, QPSK rate 3/4		-88.5		dBm
	MCS 3, 16-QAM rate 1/2		-86		dBm
	MCS 4, 16-QAM rate 3/4		-82		dBm
	MCS 5, 64-QAM rate 2/3		-78		dBm
	MCS 6, 64-QAM rate 3/4		-76.5		dBm
	MCS 7, 64-QAM rate 5/6		-75		dBm
Rx Sensitivity 802.11ac BW = 20MHz	MCS 0, BPSK rate 1/2		-94		dBm
	MCS 1, QPSK rate 1/2		-91		dBm
	MCS 2, QPSK rate 3/4		-88.5		dBm
	MCS 3, 16-QAM rate 1/2		-85.5		dBm
	MCS 4, 16-QAM rate 3/4		-82		dBm
	MCS 5, 64-QAM rate 2/3		-78		dBm
	MCS 6, 64-QAM rate 3/4		-76.5		dBm
	MCS 7, 64-QAM rate 5/6		-75		dBm
	MCS 8, 256-QAM rate 3/4		-71		dBm
Rx Sensitivity 802.11ax BW = 20MHz	MCS 0, BPSK rate 1/2		-94		dBm
	MCS 1, QPSK rate 1/2		-90.5		dBm
	MCS 2, QPSK rate 3/4		-88		dBm
	MCS 3, 16-QAM rate 1/2		-85		dBm
	MCS 4, 16-QAM rate 3/4		-82		dBm
	MCS 5, 64-QAM rate 2/3		-78		dBm
	MCS 6, 64-QAM rate 3/4		-76.5		dBm
	MCS 7, 64-QAM rate 5/6		-75		dBm
	MCS 8, 256-QAM rate 3/4		-71		dBm
	MCS 9, 256-QAM rate 5/6		-69		dBm
Max. Receive Level	6Mbps OFDM		0		dBm
	54Mbps OFDM		0		dBm
	11n, MCS 0, HT20		0		dBm
	11n, MCS 7, HT20		0		dBm
	11ac, MCS 0, VHT20		0		dBm
	11ac, MCS 8, VHT20		0		dBm
	11ax MCS 0 HE20		0		dBm
	11ax MCS 9 HE20		0		dBm
Adjacent Channel Rejection	BPSK rate 1/2, 6Mbps OFDM		TBD		dB
	64-QAM rate 3/4, 54Mbps OFDM		TBD		dB
	HT20, MCS 0, BPSK rate 1/2		TBD		dB
	HT20, MCS 7, 64-QAM rate 5/6		TBD		dB
	HE20, MCS 8, 256-QAM rate 3/4		TBD		dB
	HE20, MCS 9, 256-QAM rate 5/6		TBD		dB

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9.7.1.4 WLAN 5GHz Band Transmitter Performance

Table 9-10 WLAN 5GHz band transmitter performance

Parameter	Condition	Performance (3.3V)			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5885	MHz
Output power with spectral mask and EVM compliance[1]	BPSK rate 1/2, 6Mbps OFDM		18		dBm
	64-QAM rate 3/4, 54Mbps OFDM		18		dBm
	HT20, MCS 0, BPSK rate 1/2		18		dBm
	HT20, MCS 7, 64-QAM rate 5/6		18		dBm
	VHT20, MCS 8, 256-QAM rate 3/4		17		dBm
	HE20, MCS 9, 256-QAM rate 5/6		16		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM			-5	dB
	64-QAM rate 3/4, 54Mbps OFDM			-25	dB
	HT20, MCS 0, BPSK rate 1/2			-5	dB
	HT20, MCS 7, 64QAM rate 5/6			-27	dB
	VHT20, MCS 8, 256-QAM rate 3/4			-30	dB
	HE20, MCS 9, 256-QAM rate 5/6			-32	dB
Output power variation	TSSI on across operating temperature range, all channels and VSWR≤1.5:1 at RFIO port	-1.5		1.5	dB
Carrier suppression				-32	dBc
Harmonic output power[2]	2nd harmonic		-35		dBm/MHz
	3rd harmonic		-35		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50	dBm/MHz
	3nd harmonic			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable. The output power is measured at RF connector on the Realtek EVB with an approximate 5GHz trace loss of 1.5dB. The actual Tx power may differ from the suggested power level due to PCB losses and national regulatory restrictions. Note that the mass production (MP) power may be lower than the values mentioned above. For further details, refer to the MP flow documentation.

[2] Harmonic output power is tested at IC port.

[3] Harmonic output power is measured at RF connector with diplexer and appropriate matching.

9.7.2 Bluetooth Radio Specifications

This section describes the RF characteristics of Bluetooth 2.4GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

9.7.2.1 Bluetooth Low Energy (BLE) Receiver Performance

Table 9-11 BLE receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	-	2480	MHz
Bluetooth LE 1Mbps					
Receiver Sensitivity	PER<30.8%		-98[1]		dBm
Max. Usable Signal	PER<30.8%		0		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		6		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-5		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-48		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-52		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-27		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-26		dB
Inter-modulation			-29		dBm
Out-of-band blocking[2]	30MHz to 2000MHz	-30			dBm
	2003MHz to 2399MHz	-35			dBm
	2484MHz to 2997MHz	-35			dBm

All information provided in this document is subject to legal disclaimers.

© REALTEK 2025. All rights reserved.

	3000MHz to 12.75GHz	-30			dBm
Bluetooth LE 2Mbps					
Receiver Sensitivity	PER<30.8%		-94[1]		dBm
Max. Usable Signal	PER<30.8%		0		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		6		dB
C/I 2MHz (PER<30.8%)	Adjacent channel selectivity		-2		dB
C/I 4MHz (PER<30.8%)	2nd adjacent channel selectivity		-41		dB
C/I >= 6MHz (PER<30.8%)	3rd adjacent channel selectivity		-45		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-27		dB
C/I Image 2MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-24		dB
Inter-modulation			-29		dBm
Out-of-band blocking[2]	30MHz to 2000MHz	-30			dBm
	2003MHz to 2399MHz	-35			dBm
	2484MHz to 2997MHz	-35			dBm
	3000MHz to 12.75GHz	-30			dBm
Bluetooth LE 125kbps					
Receiver Sensitivity	PER<30.8%		-105[1]		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		3		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-15		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-53		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-56		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-35		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-35		dB
Bluetooth LE 500kbps					
Receiver Sensitivity	PER<30.8%		-100[1]		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		4		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-9		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-50		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-54		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-33		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-32		dB

NOTE

[1] The receiver sensitivity is measured at the chip out, and channels 2440MHz & 2480MHz may have extra degradation due to spurs interference.

[2] Frequencies where the requirements are not met are called "spurious response frequencies". The number of spurs must not exceed 10 if blocking signal power level is as specified above, and must not exceed 3 if it is reduced to -50dBm.

9.7.2.2 Bluetooth Low Energy (BLE) Transmitter Performance

Table 9-12 BLE transmitter performance

Parameter	Condition	Performance (PA 3.3V)			Performance (PA 1.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Output Power	At max. power output level		20			8		dBm
Bluetooth LE 1Mbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±10			±10		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		250			250		kHz
	Δf2 max.	185			185			kHz
	Δf1 avg./Δf2 avg.		0.92			0.92		
In-Band Spurious Emission	±2MHz offset		-37			-48		dBm
	>±3MHz offset		-41			-51		dBm
Bluetooth LE 2Mbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±30			±30		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		500			500		kHz

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

	Δf2 max.	370			370			kHz
	Δf1 avg./Δf2 avg.		0.93			0.93		
In-Band Spurious Emission	±4MHz offset		-40			-50		dBm
	±5MHz offset		-41			-51		dBm
	>±6MHz offset		-41			-51		dBm
Bluetooth LE 125kbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±15			±15		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		250			250		kHz
	Δf1 max.	185			185			kHz

NOTE

[1] Initial carrier frequency offset should be calibrated in MP process in customer side.

9.8 USB Interface Characteristics

The USB comply with the Universal Serial Bus (USB) V2.0 standard. All AC parameters related to these buffers can be found within the USB 2.0 electrical specifications. The following sections gives a brief overview of the electrical requirements on a USB interface. For extensive information, please refer to the USB specification.

The USB supports High-speed, Full-speed and Low-speed data rates, this document gives most attention to these items.

9.8.1 Signaling Level

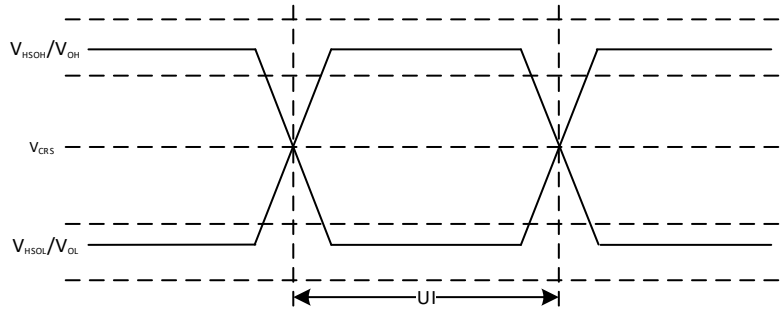


Figure 9-3 USB signal waveform

Table 9-13 USB signal waveform parameters

Speed mode	Parameter	Symbol	Min.	Max.	Unit
Low speed & full speed	Output Low	V_{OL}			V
	Output High	V_{OH}			V
	Output Signal Crossover Voltage	V_{CRS}			V
	Bit period	UI			ns
High speed	High-speed data signaling high	V_{HSOI}			mV
	High-speed data signaling low	V_{HSOH}			mV
	Bit period	UI			ns

9.8.2 Signal Rising and Fall Times

The rise and fall times are measured from 10-90% of the signal low and high levels.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

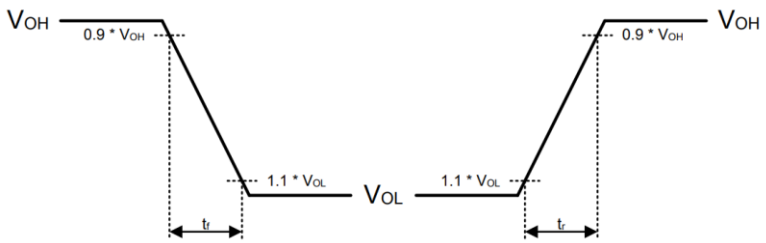


Figure 9-4 Data signal rising and falling time

Table 9-14 Data signal rising and falling time parameters

Speed mode	Parameter	Symbol	Min.	Max.	Unit
Full speed	Rise/fall time (10-90%)	t_r			ns
Low speed	Rise/fall time (10-90%)	t_r			ns
High speed	Rise/fall time (10-90%)	t_r			ps

9.9 General purpose ADC Characteristics

Table 9-15 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
fs	ADC sample frequency	-	-	166.7	400	kHz
V_{in}[1]	Conversion input voltage range	External channel (CH0 ~ CH7)	0	-	3.3	V
R_{in}	Input impedance (to GND)	External channel (CH0 ~ CH7)	-	500	-	kohm
t_{STAB}	ADC total power-up time	Including internal LDO/ADC power-up time	-	150	-	us
I_{DDA}	ADC power consumption (pin VAH_ADC)	T_A = 25°C, fs = 125kHz	-	135	-	uA
		T_A = 25°C, fs = 166.67kHz	-	145	-	
		T_A = 25°C, fs = 400kHz	-	155	-	
Resolution	-	-	-	-	12	bits
EO[2]	Offset error	fs = 166.67kHz VAH_ADC = 3.3V T_A = 25°C	TBD	-	TBD	LSB
EG[2]	Gain error		TBD	-	TBD	
INL	Integral nonlinearity		-2	-	4	
DNL	Differential nonlinearity		-1	-	2	
SFDR	Spurious free dynamic range		-	74	-	dB
THD	Total harmonic distortion		-	-68	-	
SNDR	Signal-to-noise and distortion ratio		-	62	-	
ENOB	Effective number of bits		-	10	-	bits

NOTE

[1] Conversion input voltage range: 0 ~ 3.3V (if VAH_ADC >= 3.3V) or 0 ~ VAH_ADC (if VAH_ADC < 3.3V).
[2] Need to use IC built-in calibration parameters.

9.10 QSPI Flash Memory Controller Characteristics

This section describes the timing characteristics of the Quad Serial Peripheral Interface (QSPI) for Flash memory controller.

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

All timing is shown with respect to 30% V_{IO} and 70% V_{IO} thresholds. Refer to Section 9.6 for the definitions of V_{IO}.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Table 9-16 Timing data

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SCL}	Clock period	Master			ns
t_{LOW}	Clock Low Time	Master			ns
t_{HIGH}	Clock High Time	Master			ns
t_r	Data/Clock raise time	Master			ns
t_f	Data/Clock fall time	Master			ns
$t_{SU;DAT(I)}$	Data input setup time	Master			ns
$t_{HD;DAT(I)}$	Data input hold time	Master			ns
$t_{SU;DAT(O)}$	Data output setup time	Master			ns
$t_{HD;DAT(O)}$	Data output hold time	Master			ns
$t_{VD;DAT(O)}$	Data output valid time	Master			ns
$t_{SU;CS(A)}$	CS active setup time relative to CLK	Master			ns
$t_{HD;CS(A)}$	CS active hold time relative to CLK	Master			ns

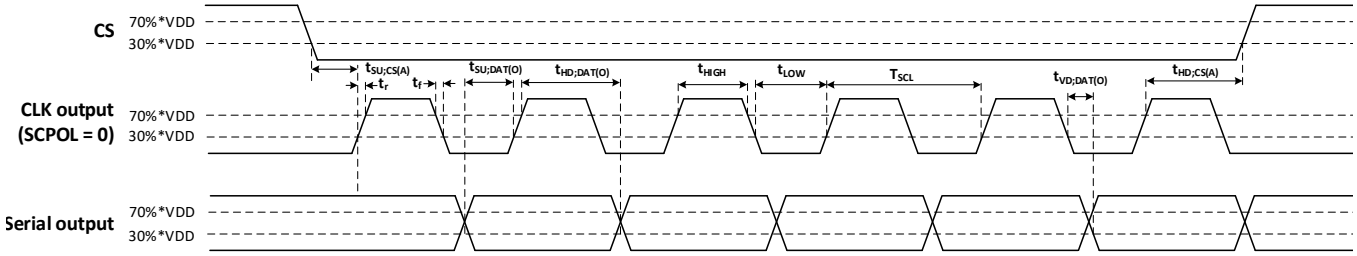


Figure 9-5 Output timing diagram (SCPH = 0)

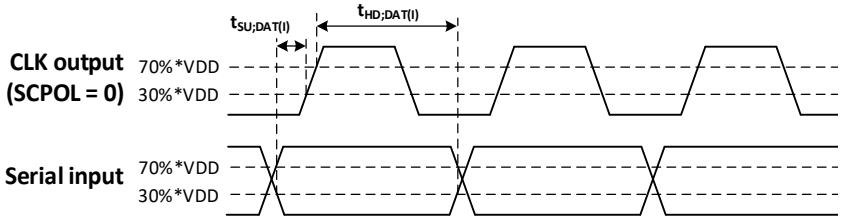


Figure 9-6 Input timing diagram (SCPH = 0)

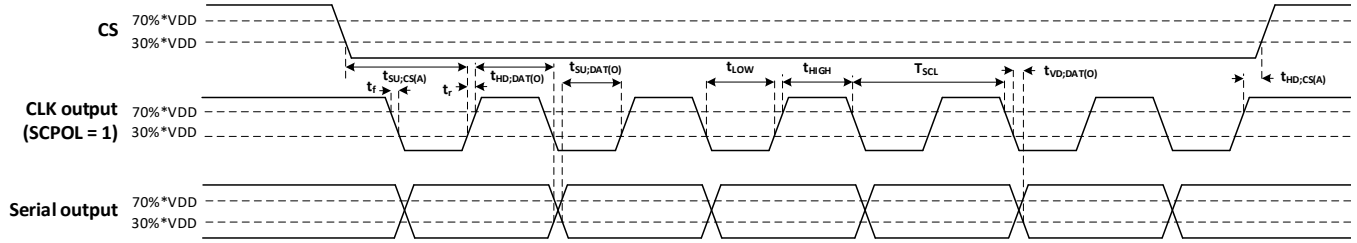


Figure 9-7 Output timing diagram (SCPH = 1)

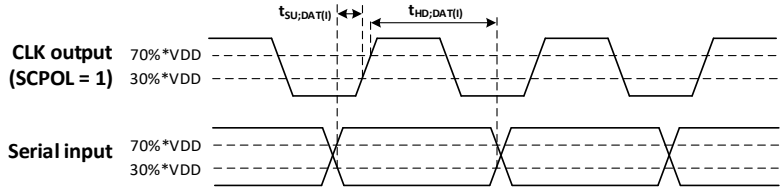


Figure 9-8 Input timing diagram (SCPH = 1)

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9.11 UART Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process covers all corners.

NOTE

Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.

Table 9-17 Timing data of UART

Item	Conditions	Min.	Typ.	Max.	Unit
Transfer rate	TXD Clock Source: 40MHz XTAL				bps
	RXD Clock Source: 40MHz XTAL				bps
	RXD Clock Source: 2MHz OSC				bps

NOTE

Total baud rate error shall be less than 3% in order to communicate correctly, which includes three parts: the error of real baud rate of Tx device and expected communication baud rate, the frequency drift of Rx IP clock, and the calculation baud error of Rx device. Users can enable the function of monitoring baud rate of Rx data to decrease the baud rate error.

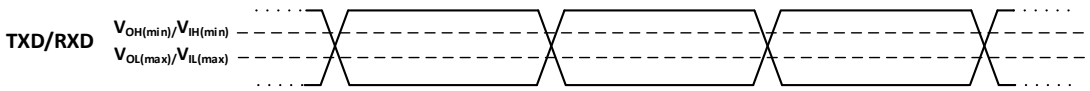


Figure 9-9 Timing diagram of UART

9.12 SPI Characteristics

The SPI function of RTL8721F is divided into dedicated SPI and full-matrix SPI.

The SPI in dedicated zone has the following features:

- Limited choices with fixed group usage, only the specified pins configured as function ID9 or ID10 can be used in combination.
  - SPI0:
    - Group1: PA4, PA5, PA18, PA19
    - Group2: PA7 ~ PA10
    - Group3: PA14 ~ PA17
    - Group4: PA23, PA24, PA27, PA28
    - Group5: PA30, PA31, PB0, PB1
  - SPI1:
    - Group1: PB7 ~ PB10
    - Group2: PB13 ~ PB16
    - Group3: PB23 ~ PB26
    - Group4: PB29 ~ PC0
    - Group5: PC2 ~ PC5
- Better timing performance

The SPI in full-matrix zone has the following features:

- More combinations and each pin signal can be flexibly configured, more pins that can be freely configured as individual signals of SPI function ID (ID29 (SPI1_CLK), ID30 (SPI1_MISO), ID31 (SPI1_MOSI), ID32 (SPI1_CS)), and can be used in any combination.
- Limited timing performance.

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process covers all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Table 9-18 Timing data of SPI in dedicated zone

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master					ns
		Slave					ns
Duty cycle	SPI duty cycle	Master					%
		Slave					%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master					ns
		Slave					ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master					ns
		Slave					ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master					ns
		Slave					ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master					ns
		Slave					ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master					ns
		Slave					ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master					ns
		Slave					ns

NOTE

- *The maximum value of $t_{VD;DAT(SO)}$ is already greater than half of a 50MHz clock cycle, so when used as a slave, the maximum speed supported by SPI is 25MHz. But if the connected master supports sampling delay function, it could support up to 50MHz.*
- *The timing data of $t_{SU;DAT(MI)}$ is only applicable to speeds of 25MHz or below. When the RTL8721Dx is used as a master running at 50MHz, due to the sample delay function of IC, the accepted minimum value of $t_{SU;DAT(MI)}$ can be -7ns for 3.3V I/O and -1ns for 1.8V I/O.*

Table 9-19 Timing data of SPI in full-matrix zone

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master					ns
		Slave					ns
Duty cycle	SPI duty cycle	Master					%
		Slave					%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master					ns
		Slave					ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master					ns
		Slave					ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master					ns
		Slave					ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master					ns
		Slave					ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master					ns
		Slave					ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master					ns
		Slave					ns

NOTE

If the connected master supports sampling with a delay, the SPI slave could support a higher speed.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

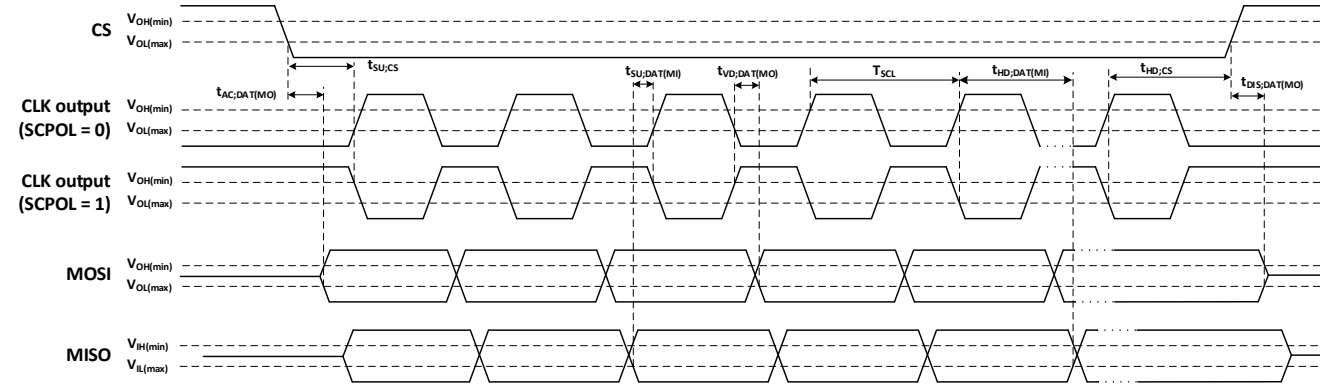


Figure 9-10 Timing diagram for master (SCPH = 0)

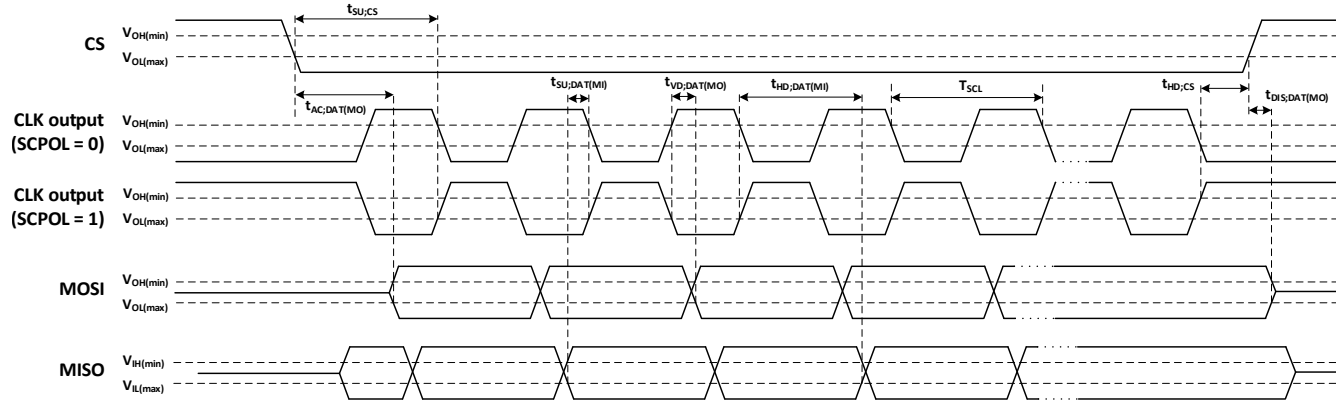


Figure 9-11 Timing diagram for master (SCPH = 1)

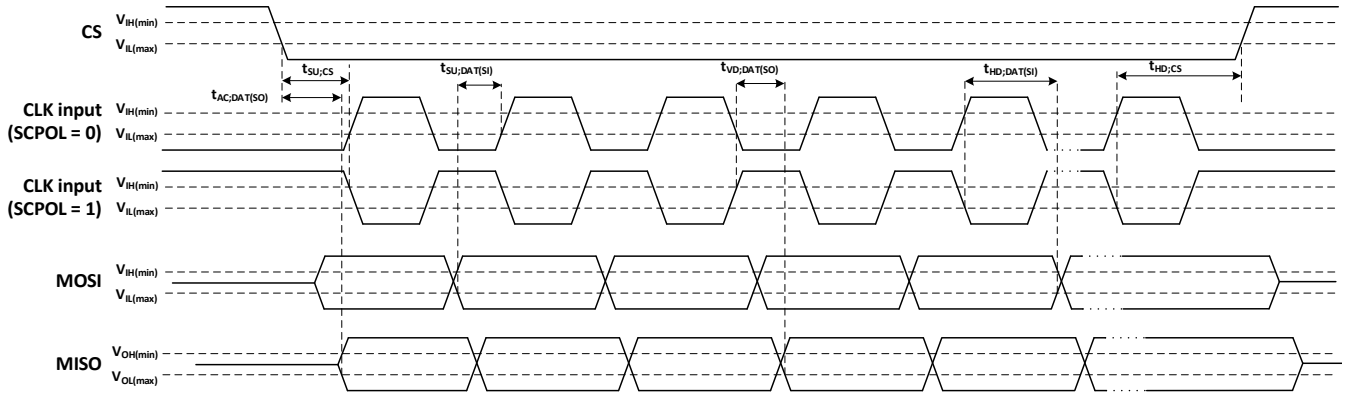


Figure 9-12 Timing diagram for slave (SCPH = 0)

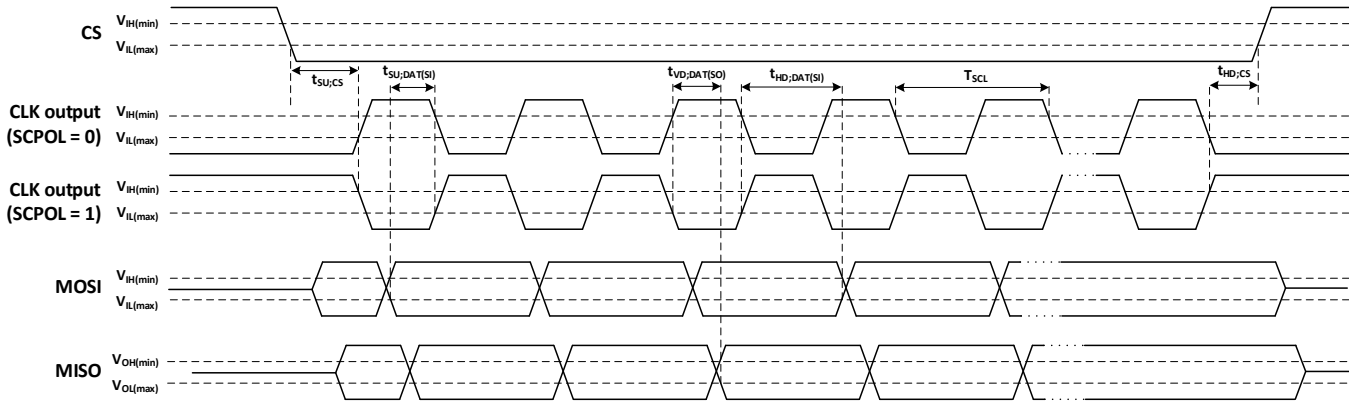


Figure 9-13 Timing diagram for slave (SCPH = 1)

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

9.13 I2C Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 400pF (SS mode, 1.7M FS mode), 100pF (3.4M HS mode).
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process covers all corners.

NOTE

All timing is shown with respect to 30% V_{IO} and 70% V_{IO} thresholds. Refer to Section 9.6 for the definitions of V_{IO}.

Table 9-20 Timing data of I2C (FS/SS mode)

Symbol	Parameter	Standard mode (Cb=400pF max.)		Fast mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency					kHz
$t_{HD;STA}$	Hold time START condition					µs
t_{LOW}	Low period of the SCL clock					µs
t_{High}	High period of the SCL clock					µs
t_r	Raise time of both SDA and SCL signals					ns
t_f	Fall time of both SDA and SCL signals					ns
$t_{SU;STA}$	Set-up time for a repeated START condition					µs
$t_{HD;DAT}$	Data hold time					us
$t_{SU;DAT}$	Data set-up time					µs
$t_{SU;STO}$	Set-up time for STOP condition					µs
$t_{VD;DAT}$	Data valid time					µs
$t_{VD;ACK}$	Data valid acknowledge time					µs
t_{BUF}	Bus free time between a STOP and START condition					µs

NOTE

Cb is the capacitive load for each bus line.

Table 9-21 Timing data of I2C (HS mode)

Symbol	Parameter	High-Speed mode (Cb=100pF max.)		High-Speed mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency					MHz
$t_{HD;STA}$	Hold time START condition					ns
$t_{SU;STA}$	Set-up time for a repeated START condition					ns
$t_{HD;DAT}$	Data hold time					ns
$t_{SU;DAT}$	Data set-up time					ns
$t_{SU;STO}$	Set-up time for STOP condition					ns
t_{high}	High period of the SCL clock					ns
t_{low}	Low period of the SCL clock					ns
t_{rCL}	Rise time of SCLH signal					ns
t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit					ns
t_{rDA}	Rise time of SDAH signal					ns
t_{fCL}	Fall time of SCLH signal					ns
t_{fDA}	Fall time of SDAH signal					ns

NOTE

Cb is the capacitive load for each bus line.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

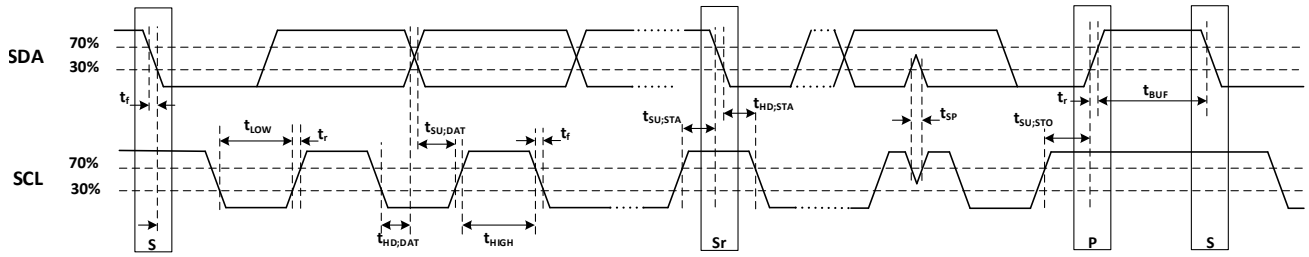


Figure 9-14 Timing diagram of I2C (FS/SS mode)

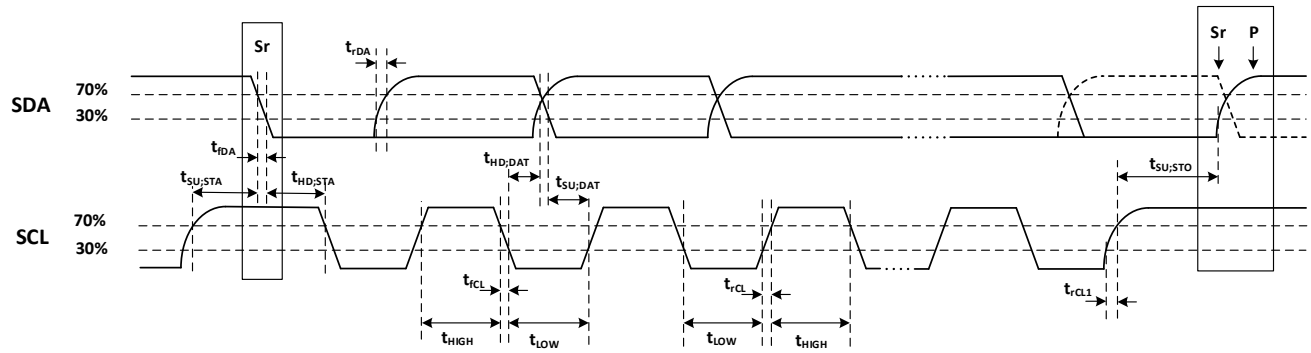


Figure 9-15 Timing diagram of I2C (HS mode)

NOTE

In HS mode, the first rising edge of SCLH signal after a repeated start condition is push-pull output instead of open-drain output.

9.14 I2C-like Characteristics

The I2C-like only supports master mode.

All data are guaranteed under the following conditions:

- The maximum loading is 400pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-22 Timing data of I2C-like

Symbol	Parameter	100k		400k		1M		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency							KHz
$t_{HD;STA}$	Hold time START condition							µs
t_{LOW}	LOW period of the SCL clock							µs
t_{High}	HIGH period of the SCL clock							µs
t_r	Raise time of both SDA and SCL signals							ns
t_f	Fall time of both SDA and SCL signals							ns
$t_{SU;STA}$	Set-up time for a repeated START condition							µs
$t_{HD;DAT}$	Data hold time							us
$t_{SU;DAT}$	Data set-up time							µs
$t_{SU;STO}$	Set-up time for STOP condition							µs
t_{BUF}	Bus free time between a STOP and START condition							µs

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

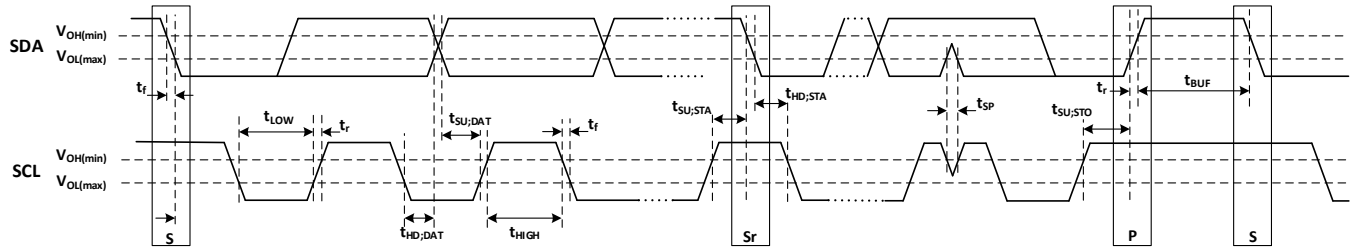


Figure 9-16 Timing diagram for I2C-like

9.15 I2S Characteristics

The Inter-IC Sound (I2S) supports both master and slave operations.

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-23 Timing data of dedicated I2S

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	I2S clock	Master					ns
		Slave					ns
Duty	Clock duty	Master					%
		Slave					%
$t_{SU;DAT(I)}$	Input data setup time	Master					ns
$t_{SU;DAT(I)}/t_{SU;WS}$	Input data/WS setup time	Slave					ns
$t_{HD;DAT(I)}$	Input data hold time	Master					ns
		Slave					ns
$t_{VD;DAT(O)}$	Output data valid time	Master					ns
$t_{VD;WS}$	Output WS valid time	Master					ns
$t_{VD;DAT(O)}$	Output data valid time	Slave					ns

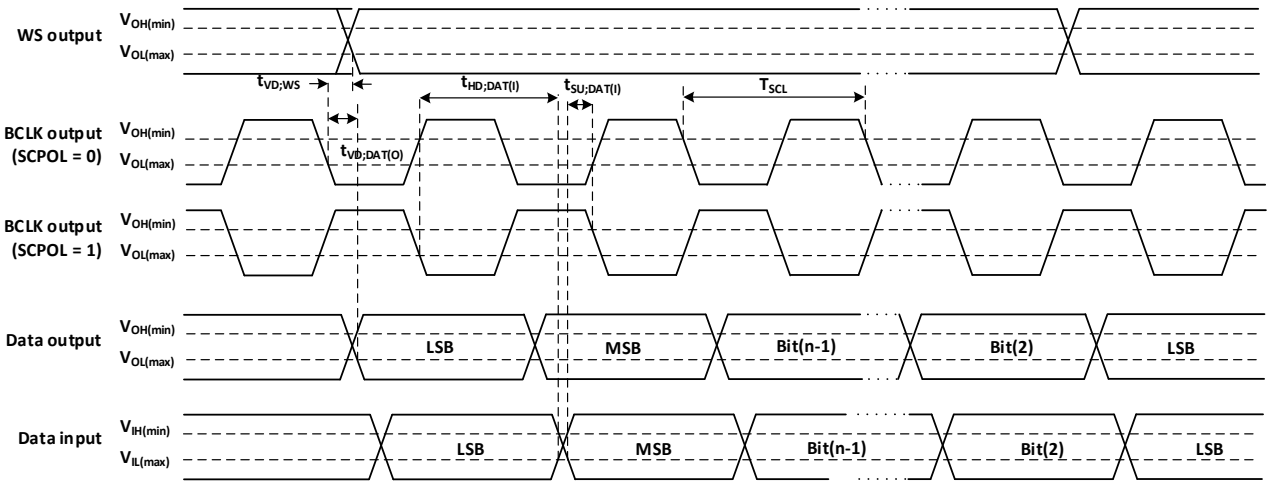


Figure 9-17 Timing diagram for I2S master

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

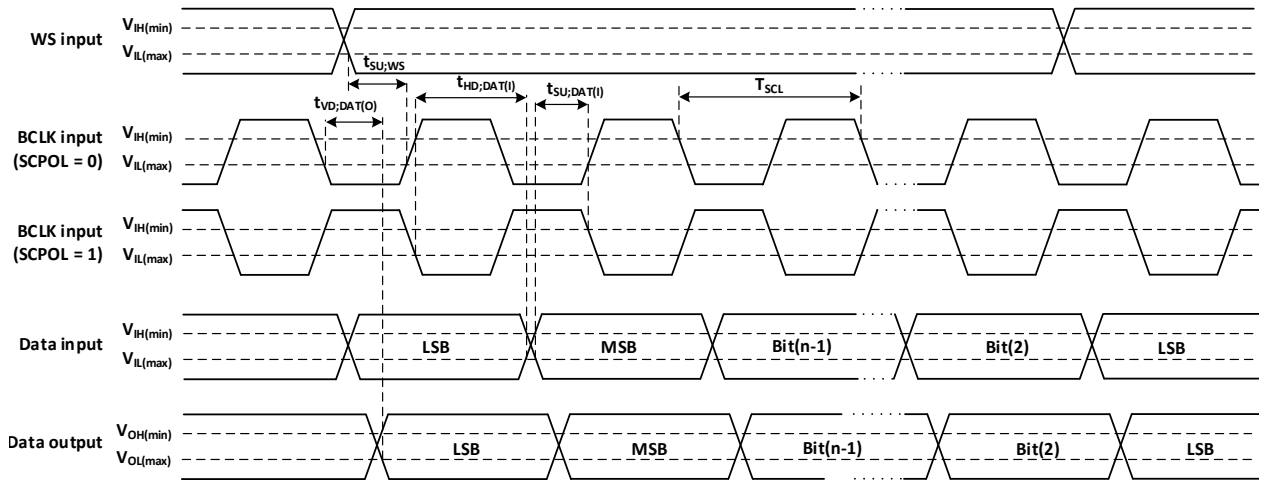


Figure 9-18 Timing diagram for I2S slave

9.16 DMIC Characteristics

The Digital Microphone (DMIC) supports only master operations.

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-24 Timing data of DMIC

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	DMIC clock period	Master					ns
Duty cycle	DMIC clock duty cycle	Master					%
$t_{SU;DAT(R)}$/$t_{SU;DAT(F)}$	Input data Rising/Falling edge setup time	Master					ns
$t_{HD;DAT(R)}$/$t_{HD;CS(F)}$	Input data Rising/Falling edge hold time	Master					ns

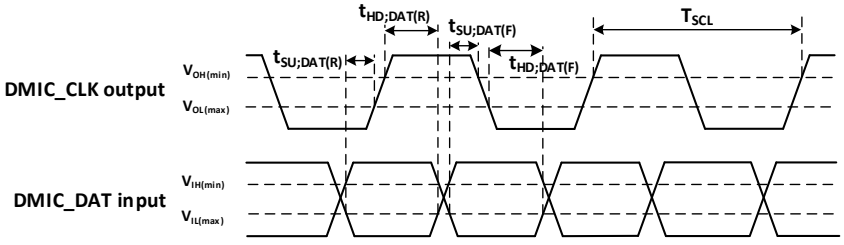


Figure 9-19 Timing diagram of DMIC

9.17 SWD Interface Characteristics

The debug interface of RTL8721F is Arm standard bi-directional Serial Wire Debug (SWD).

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-25 Timing data of SWD

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SWCLK clock period	Slave					ns
Duty cycle	Input clock duty cycle	Slave					%
$t_{VD;DAT(O)}$	Output data valid time	Slave					ns
$t_{VD;DAT(I)}$	Input data setup time	Slave					ns
$t_{HD;DAT(I)}$	Input data hold time	Slave					ns

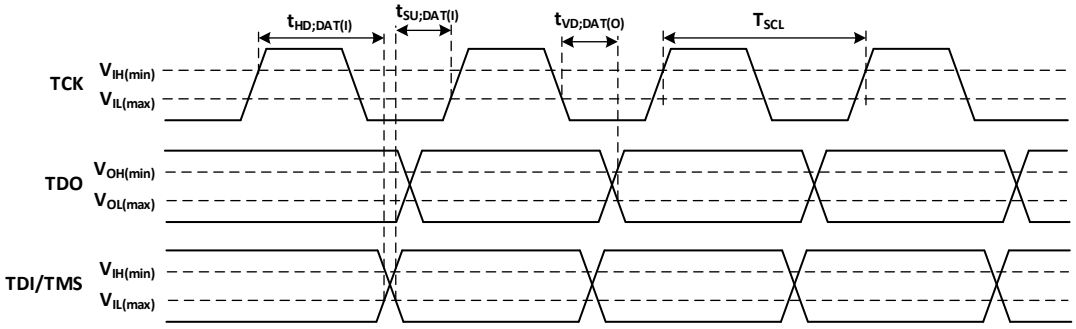


Figure 9-20 Timing diagram of SWD

9.18 SD/eMMC/SDIO Host Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-26 Timing data of SDIO host (default speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SDIO clock period	Master					ns
Duty cycle	SDIO duty cycle	Master					%
$t_{VD;DAT(O)}$/$t_{VD;CMD(O)}$	Data output valid time	Master					ns
$t_{SU;DAT(I)}$/$t_{SU;CMD(I)}$	Data input setup time	Master					ns
$t_{HD;DAT(I)}$/$t_{HD;CMD(I)}$	Data input hold time	Master					ns

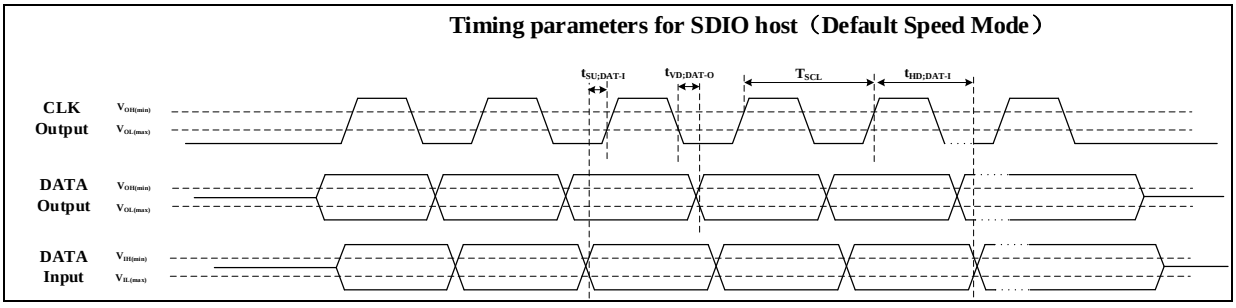


Figure 9-21 Timing diagram of SDIO host (default speed mode)

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Table 9-27 Timing data of SDIO host (high speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SDIO clock period	Master					ns
Duty cycle	SDIO duty cycle	Master					%
$t_{VD;DAT(O)}/t_{VD;CMD(O)}$	Data output valid time	Master					ns
$t_{SU;DAT(I)}/t_{SU;CMD(I)}$	Data input setup time	Master					ns
$t_{HD;DAT(I)}/t_{HD;CMD(I)}$	Data input hold time	Master					ns

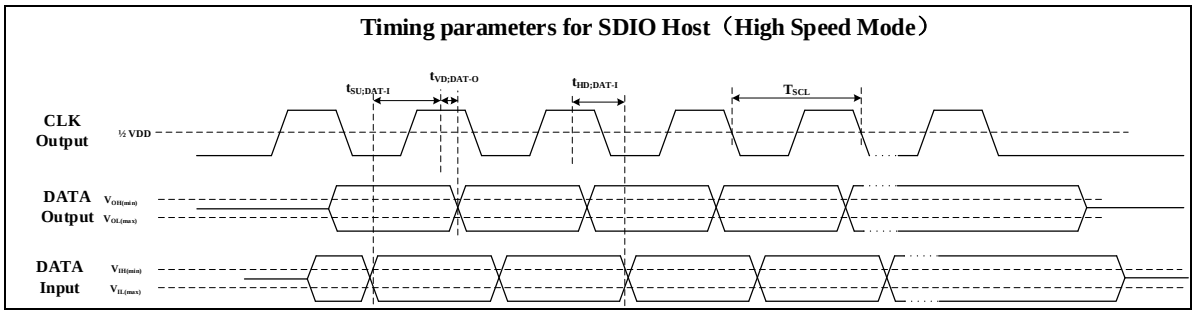


Figure 9-22 Timing diagram of SDIO host (high speed mode)

9.19 SDIO Device Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-28 Timing data of SDIO device (default speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
f_{pp}	SDIO clock frequency	Slave	0	25	0	25	MHz
t_{WL}	Clock low time	Slave	10	-	10	-	ns
t_{WH}	Clock high time	Slave	10	-	10	-	ns
t_{TLH}	Clock rise time	Slave	-	10	-	10	ns
t_{THL}	Clock fall time	Slave	-	10	-	10	ns
t_{ODLY}	Data/CMD output valid time	Slave	0	14	0	14	ns
t_{ISU}	Data/CMD input setup time	Slave	5	-	5	-	ns
t_{ISH}	Data/CMD input hold time	Slave	5	-	5	-	ns

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

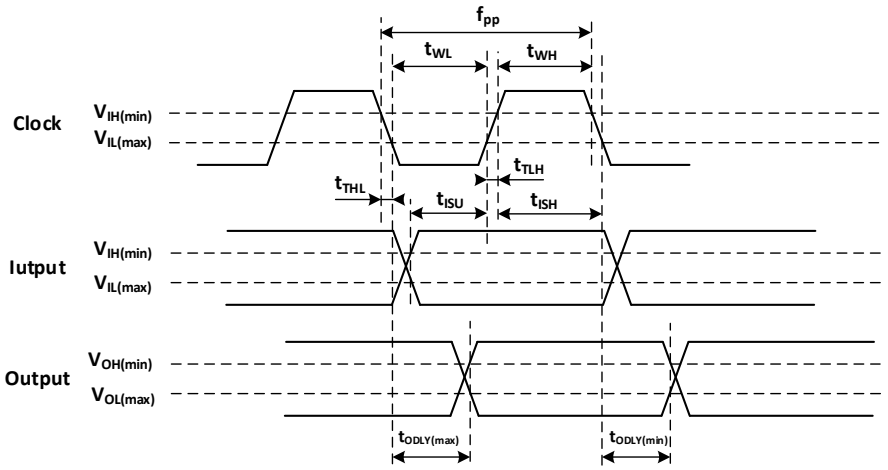


Figure 9-23 Timing parameters for SDIO device (default speed mode)

Table 9-29 Timing data of SDIO device (high speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
f_{pp}	SDIO clock frequency	Slave	0	50	0	50	MHz
t_{WL}	Clock low time	Slave	7	-	7	-	ns
t_{WH}	Clock high time	Slave	7	-	7	-	ns
t_{TLH}	Clock rise time	Slave	-	3	-	3	ns
t_{THL}	Clock fall time	Slave	-	3	-	3	ns
t_{ODLY}	Data/CMD output valid time	Slave	0	14	0	14	ns
t_{OH}	Data/CMD output hold time	Slave	2.5	-	2.5	-	ns
t_{ISU}	Data/CMD input setup time	Slave	6	-	6	-	ns
t_{ISH}	Data/CMD input hold time	Slave	2	-	2	-	ns

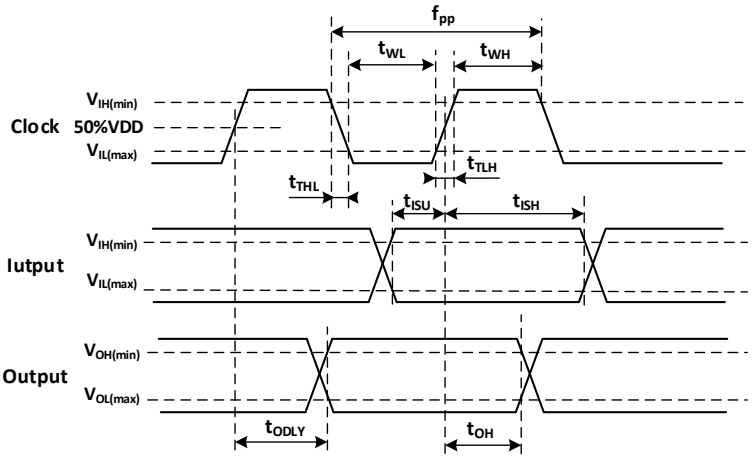


Figure 9-24 Timing parameters for SDIO device (high speed mode)

9.20 RMII Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Table 1-3 Timing data of RMII in MAC mode

Symbol	Parameter	Conditions	3.3V I/O		Unit
			Min.	Max.	
T_{REF_CLK}	REF_CLK cycle time	MAC			ns
Duty REF_CLK	Clock duty of REF_CLK	MAC			ns
$t_{SU;DAT(I)}$	Input data setup time	MAC			ns
$t_{HD;DAT(I)}$	Input data hold time	MAC			ns
$t_{SU;CRS(I)}$	Input carrier sense setup time	MAC			ns
$t_{HD;CRS(I)}$	Input carrier sense hold time	MAC			ns
$t_{SU;ER(I)}$	Input Rx error setup time	MAC			ns
$t_{HD;ER(I)}$	Input Rx error hold time	MAC			ns
$t_{VD;EN(O)}$	Output enable valid time	MAC			ns
$t_{VD;DAT(O)}$	Output data valid time	MAC			ns

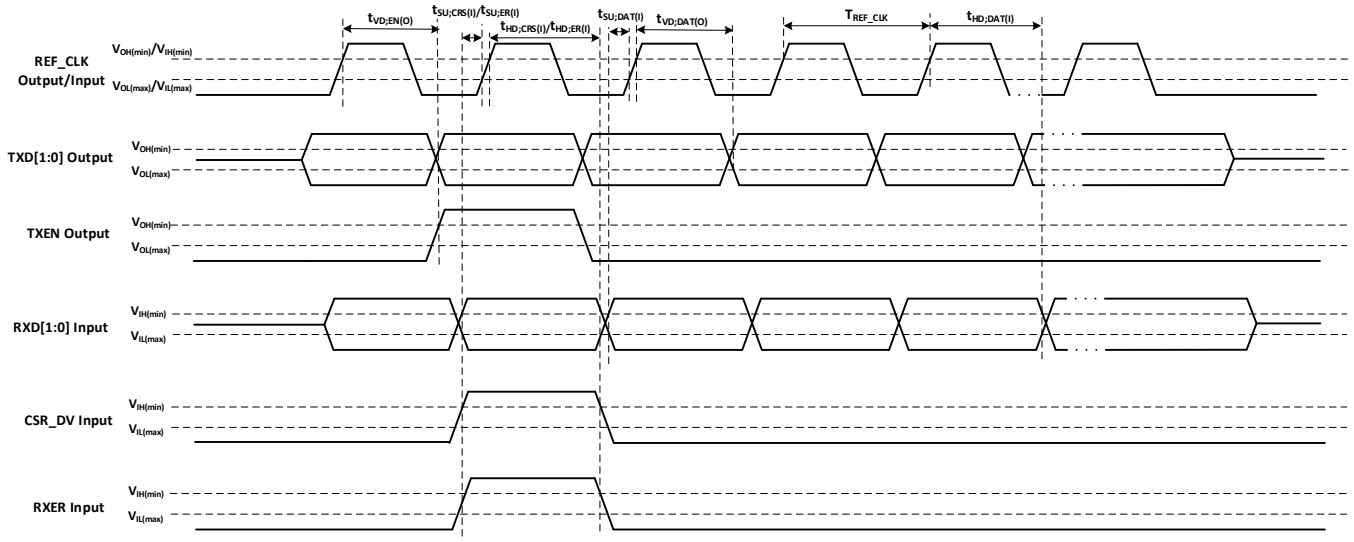


Figure 9-25 Timing parameters for RMII in MAC mode

9.21 MDC/MDIO Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-30 Timing data of MDC/MDIO

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	MDC period	Master/Slave					ns
Duty cycle	MDC duty cycle	Master/Slave					%
$t_{VD;DAT(MO)}$	Output data valid time	Master					ns
$t_{VD;DAT(SO)}$	Output data valid time	Slave					ns
$T_{SU;DAT(I)}$	Input data setup time	Master/Slave					ns
$t_{HD;DAT(I)}$	Input data hold time	Master/Slave					ns

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

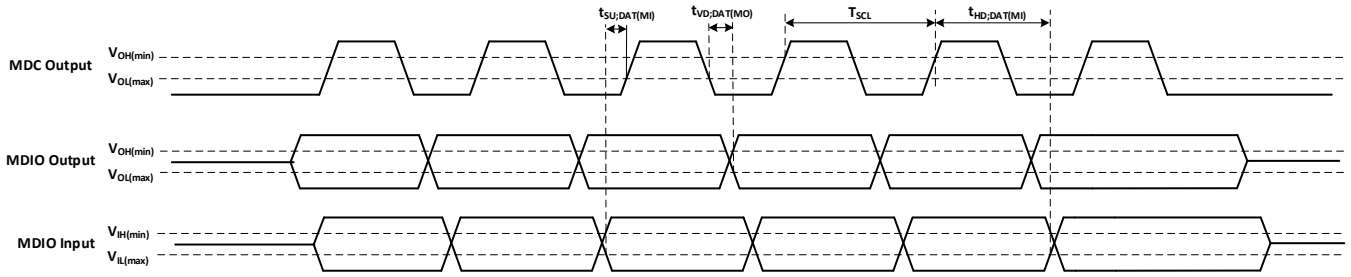


Figure 9-26 Timing parameters for MDC/MDIO in master mode

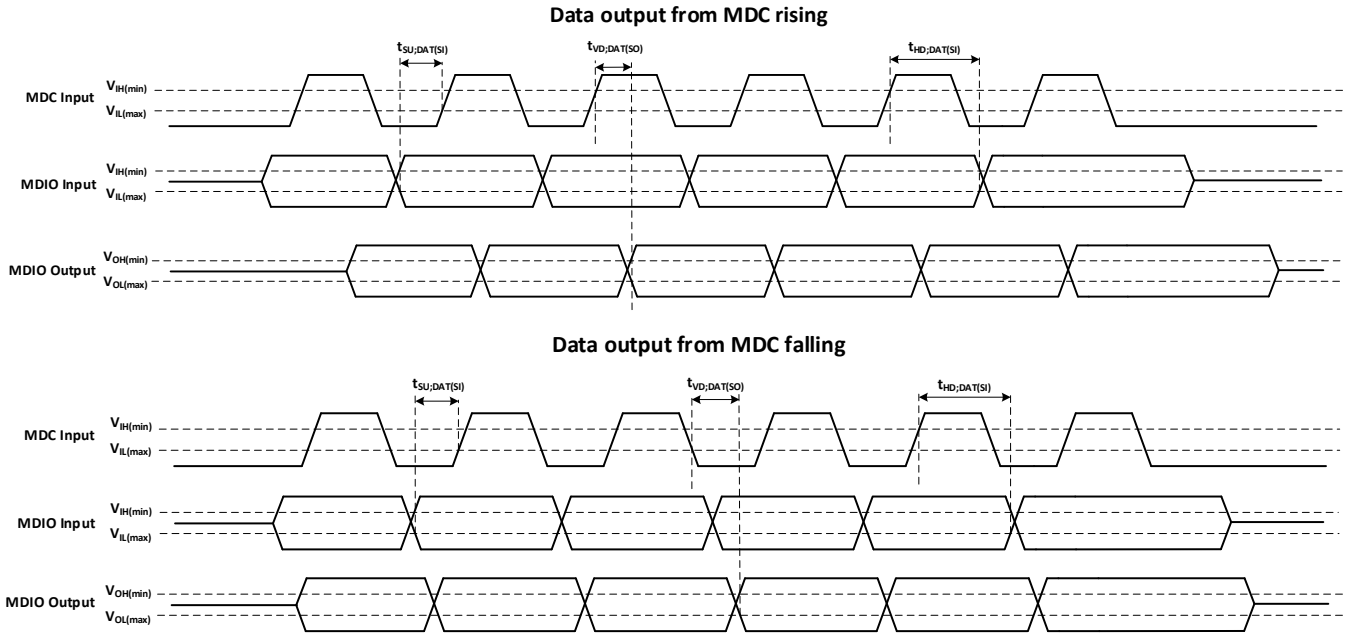


Figure 9-27 Timing parameters for MDC/MDIO in slave mode

9.22 LCDC Characteristics

All data are guaranteed under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

- *Refer to Section 9.6 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.*
- *The operating voltage of 3.3V I/O ranges from 2.97V to 3.63V, and the operating voltage of 1.8V I/O ranges from 1.71V to 1.98V.*

Table 9-31 Timing data of RGB Mode

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	DCLK period	Master					MHz
Duty cycle	CLK pulse duty	Master					ns
$t_{VD;DAT(O)}$	Data output valid time	Master					ns
$t_{VD;VSYNC(O)}$	VSYNC output valid time	Master					ns
$t_{VD;HSYNC(O)}$	HSYNC output valid time	Master					ns
$t_{VD;EN(O)}$	Enable output valid time	Master					ns

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

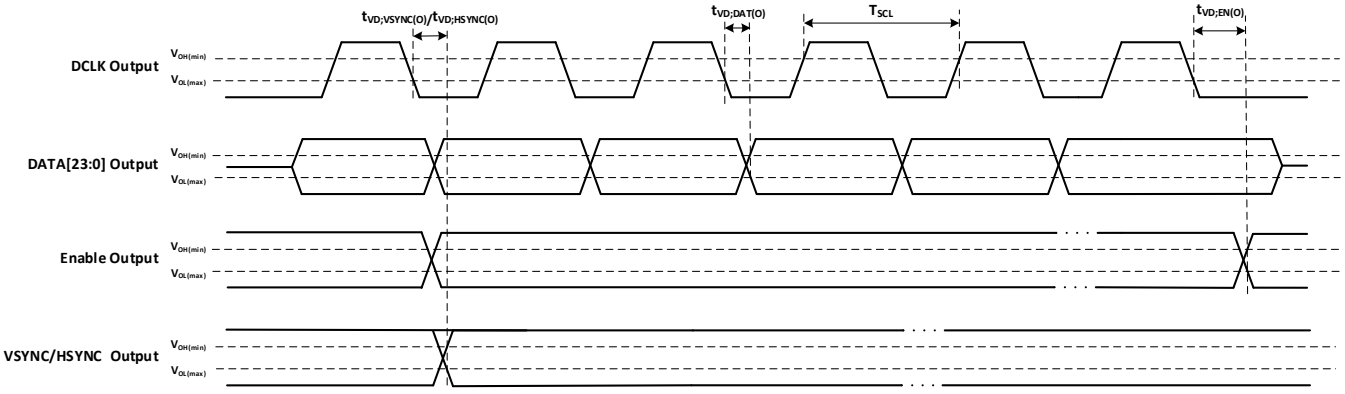


Figure 9-28 Timing parameters for parallel RGB

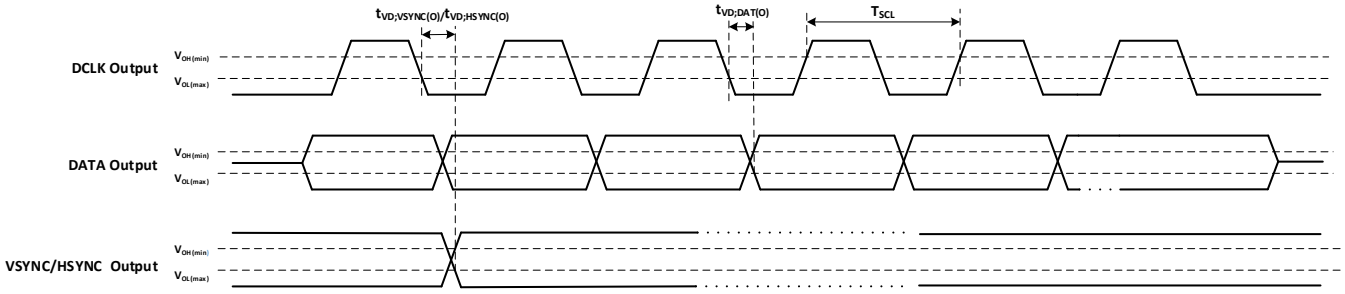


Figure 9-29 Timing parameters for serial RGB

Table 9-32 Timing data of MCU Mode

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{WR}	Write cycle period	Master					ns
T_{RD}	Read cycle period	Master					ns
$t_{VD;DAT(O)}$	Data output valid time	Master					ns
$t_{SU;DAT(I)}$	Input data setup time	Master					ns
$t_{HD;DAT(1)}$	Input data hold time	Master					ns
$t_{SU;CS}$	CS setup time	Master					ns
$t_{HD;CS}$	CS hold time	Master					ns
$t_{SU;AD}$	Address setup time	Master					ns
$t_{HD;AD}$	Address hold time	Master					ns

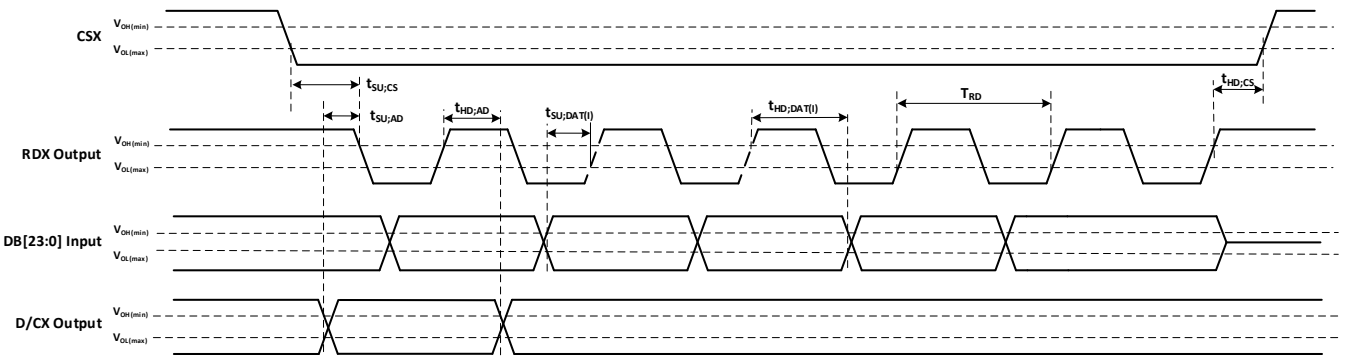


Figure 9-30 Read timing parameters for LCDC in MCU mode

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

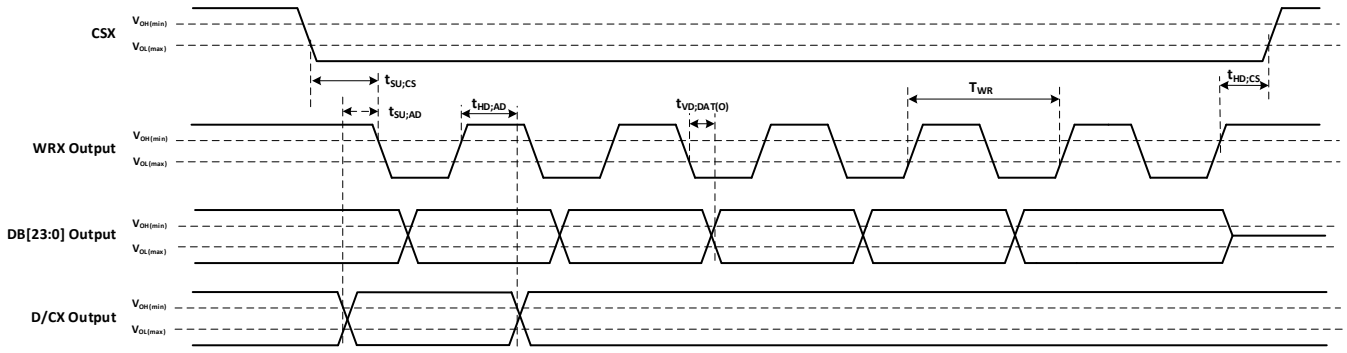


Figure 9-31 Write timing parameters for LCDC in MCU mode

9.23 Thermal Characteristics

Symbol	Parameter[1]	Package	Condition	Value[2][3]	Unit
θ_{JA}	Junction-to-ambient thermal resistance	QFN, 48-pin	56mm x 85mm 4-layer PCB with no air flow	37.82	°C/W
		QFN, 68-pin	56mm x 65mm 4-layer PCB with no air flow	33.2	
		QFN, 100-pin	56mm x 65mm 4-layer PCB with no air flow	27.58	
Ψ_{JT}	Junction-to-top center thermal characterization parameter	QFN, 48-pin	56mm x 85mm 4-layer PCB with no air flow	1.55	
		QFN, 68-pin	56mm x 65mm 4-layer PCB with no air flow	0.72	
		QFN, 100-pin	56mm x 65mm 4-layer PCB with no air flow	0.43	
Ψ_{JB}	Junction-to-board thermal characterization parameter	QFN, 48-pin	56mm x 85mm 4-layer PCB with no air flow	16.96	
		QFN, 68-pin	56mm x 65mm 4-layer PCB with no air flow	14.84	
		QFN, 100-pin	56mm x 65mm 4-layer PCB with no air flow	14.85	

NOTE

[1] Refer to EIA/JESD51-2, Integrated circuit Thermal Test Method Environment Conditions – Natural Convection (Still Air) for more information.

[2] These values are based on customized PCB systems designed by Realtek Semiconductor Corp. and will vary in function of board thermal characteristics and other components on the board.

[3] An ambient temperature of 85°C is assumed.

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

10 Mechanical Dimensions

In order to meet environmental requirements, Realtek offers devices in different grades of ECOPACK® packages, depending on the level of environmental compliance.

10.1 QFN48

The QFN48 is a 48-pin, 6mm x 6mm quad flat no-leads package with 0.4mm pitch.

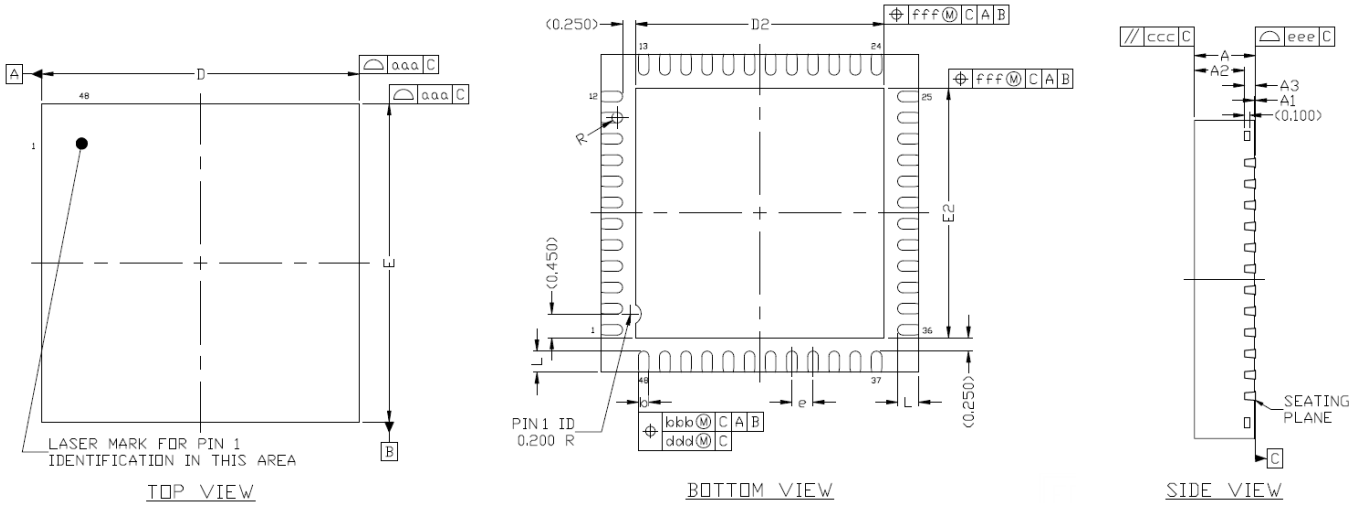


Figure 10-1 QFN48 package outline

Table 10-1 QFN48 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.100	1.150	1.200	0.043	0.045	0.047
A1	0.000	0.025	0.050	0.000	0.001	0.002
A2	-	0.950	1.000	-	0.037	0.039
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	5.900	6	6.100	0.232	0.236	0.240
D2	4.600	4.700	4.800	0.181	0.185	0.189
E	5.900	6	6.100	0.232	0.236	0.240
E2	4.600	4.700	4.800	0.181	0.185	0.189
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M. -1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

10.2 QFN68

The QFN68 is a 68-pin, 8mm x 8mm quad flat no-leads package with 0.4mm pitch.

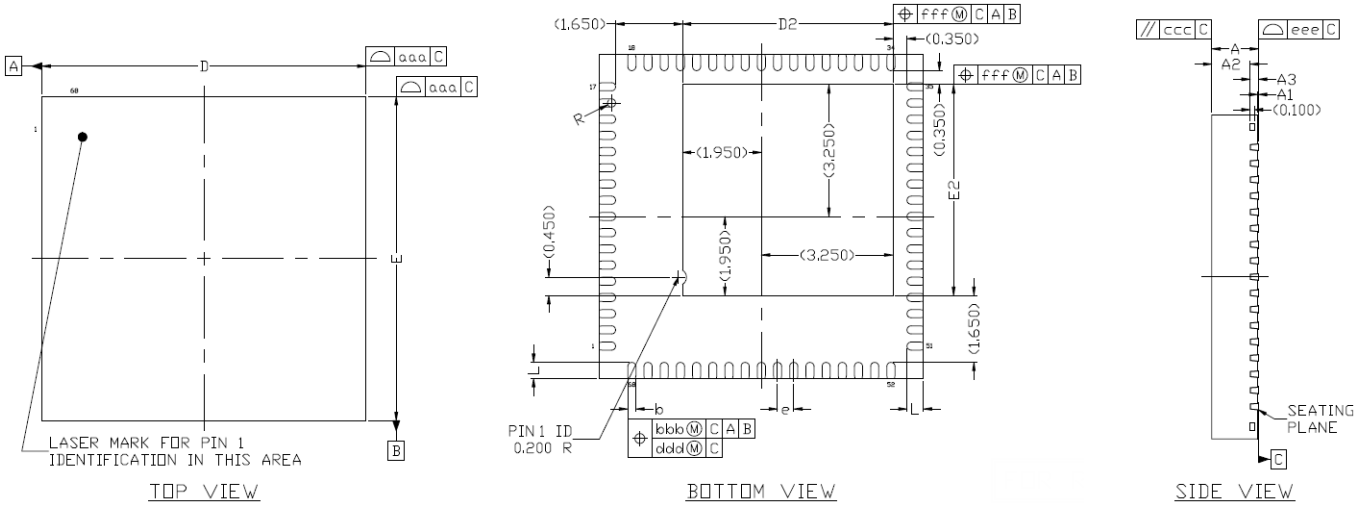


Figure 10-2 QFN68 package outline

Table 10-2 QFN68 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.100	1.150	1.200	0.043	0.045	0.047
A1	0.000	0.025	0.050	0.000	0.001	0.002
A2	-	0.950	1.000	-	0.037	0.039
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	7.900	8	8.100	0.311	0.315	0.319
D2	5.100	5.200	5.300	0.201	0.205	0.209
E	7.900	8	8.100	0.311	0.315	0.319
E2	5.100	5.200	5.300	0.201	0.205	0.209
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M. -1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

10.3 QFN100

The QFN100 is a 100-pin, 10mm x 10mm quad flat no-leads package with 0.35mm pitch.

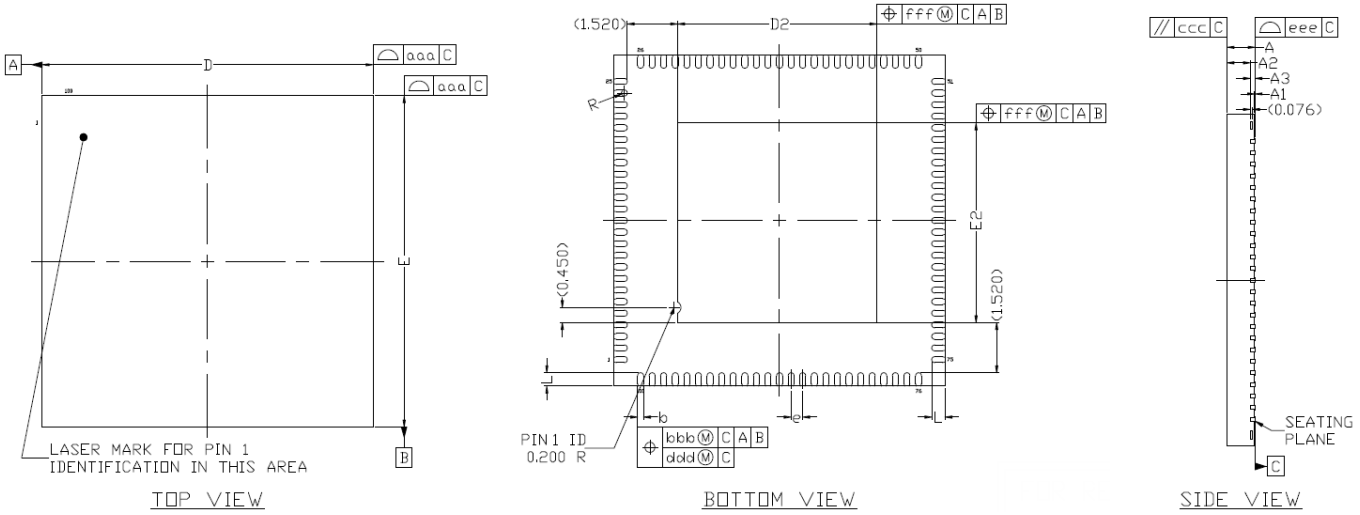


Figure 10-3 QFN100 package outline

Table 10-3 QFN100 package mechanical data

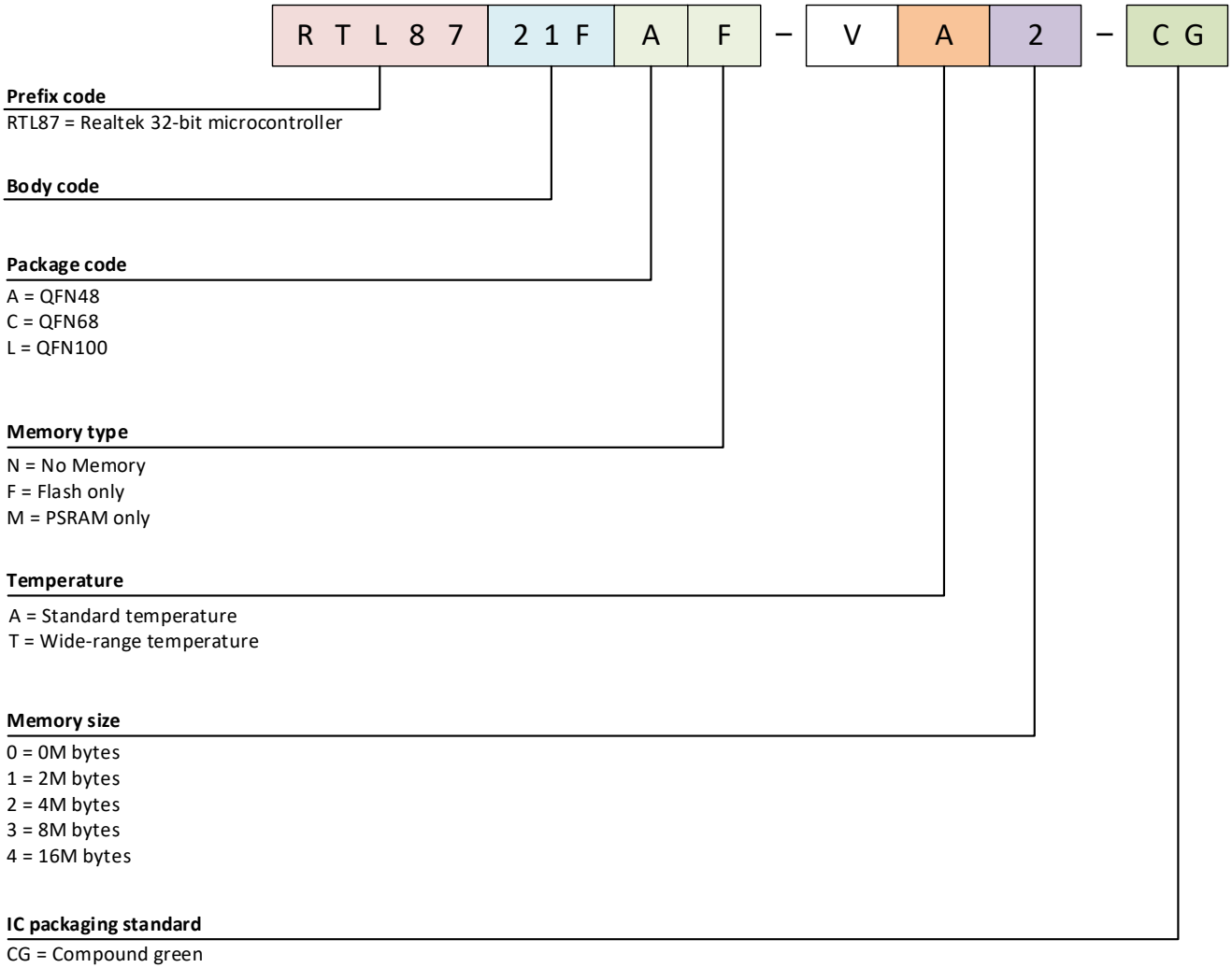
Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.800	0.850	0.900	0.031	0.033	0.035
A1	0.000	0.025	0.050	0.000	0.001	0.002
A2	-	0.700	0.750	-	0.028	0.030
A3	0.152 REF			0.006 REF		
b	0.130	0.180	0.230	0.005	0.007	0.009
D	9.900	10	10.100	0.390	0.394	0.398
D2	5.920	6.020	6.120	0.233	0.237	0.241
E	9.900	10	10.100	0.390	0.394	0.398
E2	5.920	6.020	6.120	0.233	0.237	0.241
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.350 BSC			0.014 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M. -1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

11 Ordering Information



Part number	Package	Flash	PSRAM	Status
RTL8721FAF-VA2-CG	QFN48	4M bytes	-	
RTL8721FAF-VT2-CG	QFN48	4M bytes	-	
RTL8721FAM-VA2-CG	QFN48	-	4M bytes	
RTL8721FAM-VT2-CG	QFN48	-	4M bytes	
RTL8721FCM-VA2-CG	QFN68	-	4M bytes	
RTL8721FCM-VA3-CG	QFN68	-	8M bytes	
RTL8721FCM-VA4-CG	QFN68	-	16M bytes	
RTL8721FLM-VA4-CG	QFN100	-	16M bytes	

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.

Revision History

Date	Revision	Release Notes
2025-07-09	0.5.1	Updated the section: *Ordering Information*
2025-06-23	0.5.0	● Reorganized the chapters and contents ● Added more information ● Updated some detailed description
2025-04-15	0.4.0	Updated the section: *Ordering Information*
2024-08-29	0.3.0	● Updated the series number from RTL8721E to RTL8721F ● Updated the section: *Ordering Information*
2024-08-20	0.2.0	Updated the following sections: ● *Functional Block Diagram* ● *Features* ● *Ordering Information* ● *RF Characteristics*
2024-04-09	0.1.0	Initial release

All information provided in this document is subject to legal disclaimers.
© REALTEK 2025. All rights reserved.