UM0401
RTL872xD Datasheet

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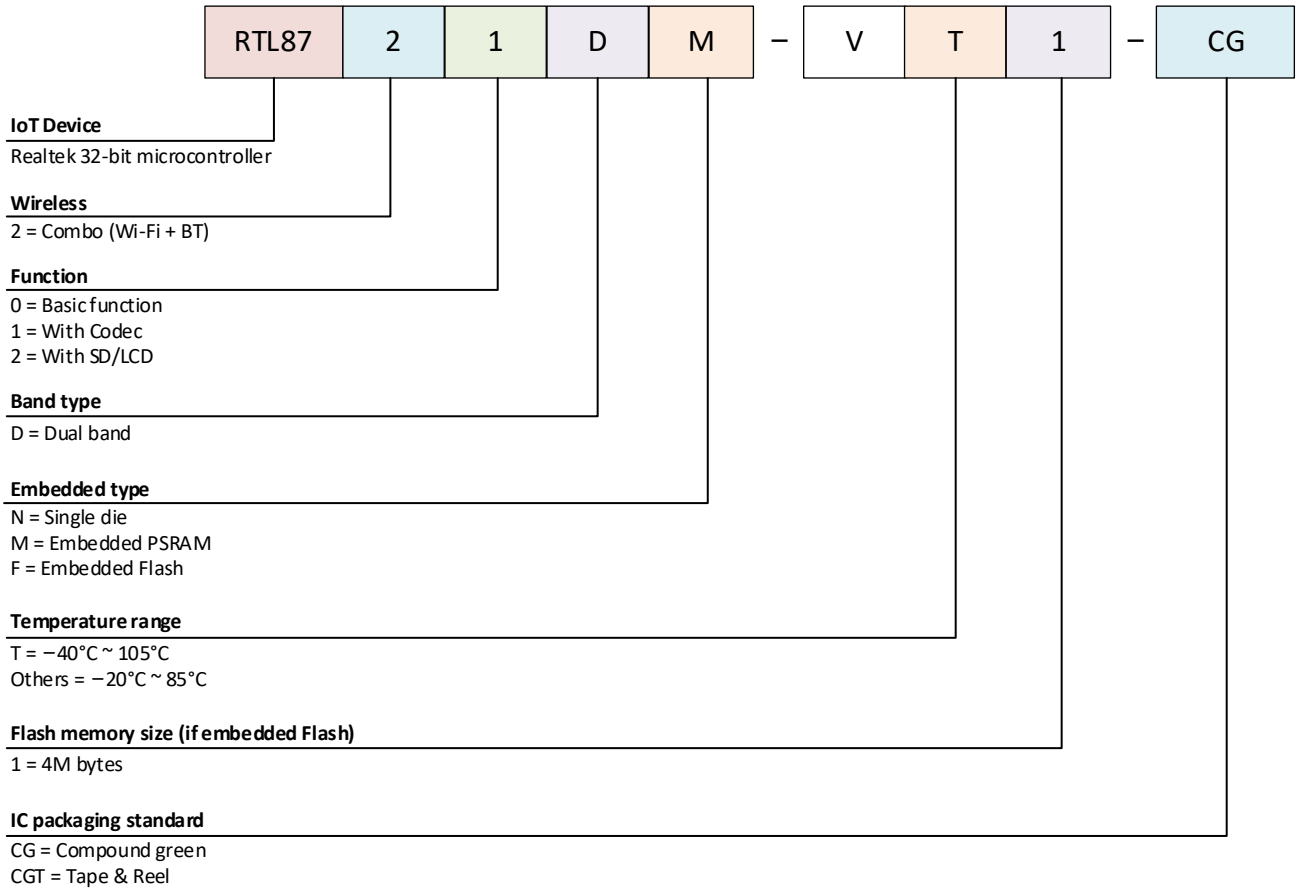


Part Number	Package	Status
RTL8720DN-VA1-CG	QFN48	MP
RTL8720DN-VA1-CGT	QFN48	MP (tape-and-reel)
RTL8720DN-VT1-CG	QFN48	MP
RTL8720DM-VA1-CG	QFN48	MP
RTL8720DF-VA1-CG	QFN48	MP
RTL8720DF-VT1-CG	QFN48	MP
RTL8720DF-VT1-CGT	QFN48	MP (tape-and-reel)
RTL8721DM-VA1-CG	QFN68	MP
RTL8721DM-VA1-CGT	QFN68	MP (tape-and-reel)
RTL8721DF-VT1-CG	QFN68	MP
RTL8722DM-VA1-CG	QFN88	MP
RTL8722DM-VA1-CGT	QFN88	MP (tape-and-reel)
RTL8722DM-VP1-CG	QFN88	ES

Contents

1 Product Overview

1.1 General Description

RTL872xD is a highly integrated single-chip low power dual bands (2.4GHz and 5GHz) Wireless LAN (WLAN) and Bluetooth Low Energy (BLE 5.0) communication controller. It consists of a high performance MCU (Armv8-M, Cortex-M33 instruction set compatible) called Real-M300 (or KM4 thereafter) and a low power MCU (Armv8-M, Cortex-M23 instruction set compatible) called Real-M200 (or KM0 thereafter), WLAN (802.11 a/b/g/n) MAC, an 1T1R capable WLAN baseband, RF, Bluetooth and peripherals.

High speed connectivity interfaces, SDIO and USB are provided. There are also audio codec, Key-Scan and touch keys integrated into this IC. Besides, flexible design configures GPIO to different functions according to applications.

RTL872xD also integrates memories (ROM/SRAM/PSRAM) for IoT (Internet of Things) Wi-Fi protocol functions and applications. The user-friendly development kits (SDK and HDK) are supported to customers for developing IoT applications.

The KM4 MCU is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, floating point computation, DSP instructions and a high level of support block integration. The KM4 MCU incorporates a 3-stage pipeline.

The KM0 coprocessor is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the KM4 core. The KM0 coprocessor offers up to 20MHz performance with a simple instruction set and reduced code size.

1.2 System Architecture

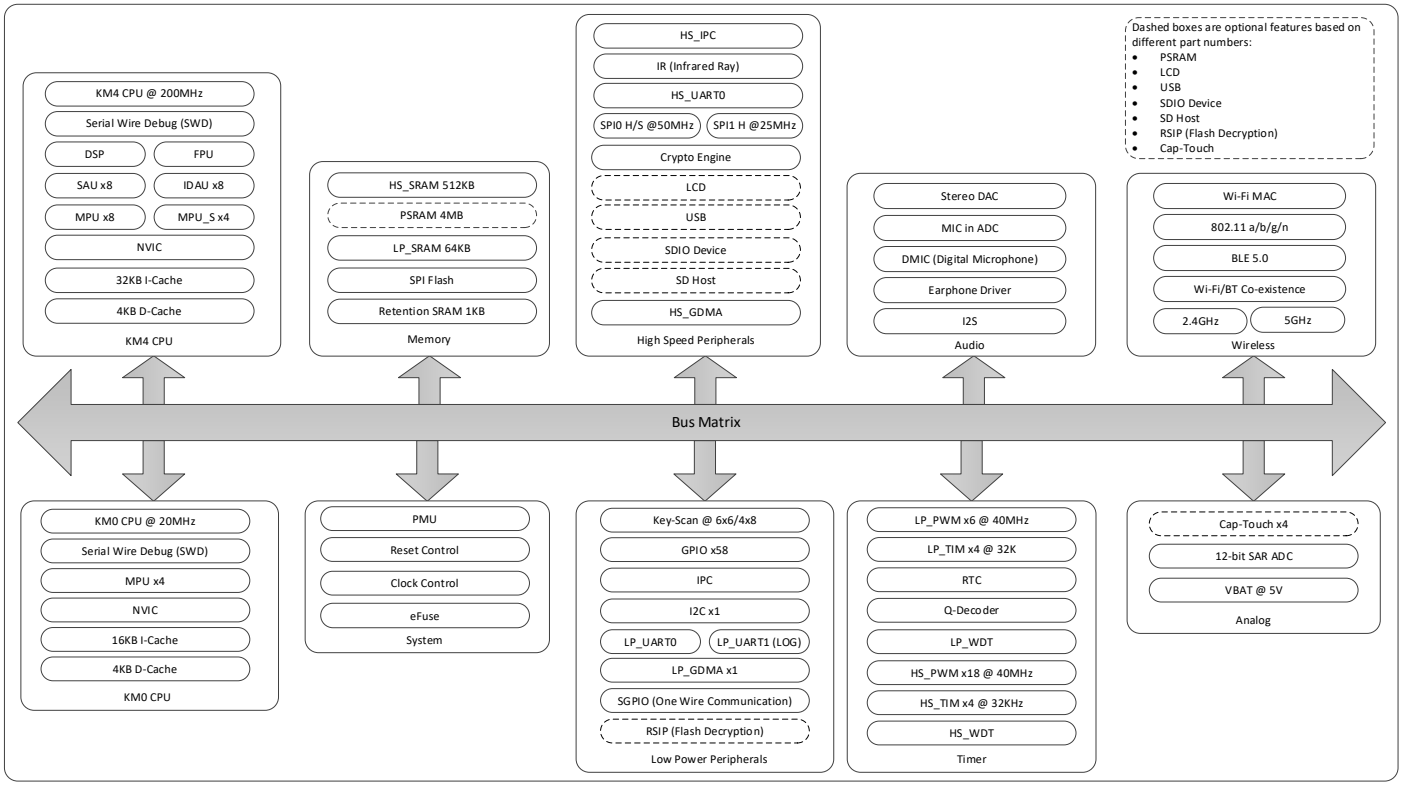


Figure 1-1 System architecture

In RTL872xD, the main system consists of 32-bit multilayer AXI bus matrix that interconnects all the masters and the slaves. The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

A multilayer AXI bus matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slave ports of the matrix to be accessed simultaneously by different bus masters.

APB peripherals are connected to the AXI bus matrix via APB buses using separate slave ports from the multilayer AXI bus matrix. This allows for better performance by reducing collisions between the CPU and the DMA controller, and also for peripherals on the asynchronous bridge to have a fixed clock that does not track the system clock.

1.3 Features

1.3.1 System and Memory

Table 1-1 System and memory features

Items	Description
Processor	● Dual processor core ● KM4: Armv8-M architecture with Cortex-M33 instruction set compatible ● KM0: Armv8-M architecture with Cortex-M23 instruction set compatible ● Equal access to address space including SRAM, peripherals and registers
KM4 CPU	● Cortex-M33 instruction set compatible ■ Floating Point Unit (FPU) ■ DSP ■ TrustZone-M ● Running at a frequency of up to 200MHz (configurable) ● Memory Protection Unit (MPU) ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Non-maskable Interrupt (NMI) with a selection of sources ● Serial Wire Debug (SWD) with 2 HW breakpoints and 1 watchpoint (without Serial Wire Output (SWO) for enhanced debug capabilities) ● System tick timer ● 32KB I-Cache and 4KB D-Cache
KM0 CPU	● Cortex-M23 instruction set compatible ● Running at a frequency of up to 20MHz ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Non-maskable Interrupt (NMI) with a selection of sources ● SWD with 2 HW breakpoints and 1 watchpoint ● System tick timer ● 16KB I-Cache and 4KB D-Cache
KM4 CPU On-Chip memory	● Up to 512KB contiguous main SRAM @200MHz ● Optional 4MB PSRAM @ 50MHz, 8-bit DDR, refer to *1.4.2*
KM0 CPU On-Chip memory	● Up to 64KB contiguous main SRAM ● Up to 1KB retention SRAM for keeping data in power saving modes
GDMA	● KM4 and KM0 both have a GDMA controller ● HS-GDMA0 supports six channels with TrustZone-M ● LP-GDMA0 supports six channels without TrustZone-M
Flash	● Optional internal 4M bytes (32M bits) Flash, refer to *1.4.2* ● SPI/DSPI/QSPI[1] Flash controller with cache ● Flash In-Circuit Programming (ICP) supported
General-Purpose I/O (GPIO)	● Up to 64 General-Purpose I/O (GPIO) pins. All GPIOs have configurable pull-up/pull-down resistors. ● GPIO interrupt trigger could be configured with rising, falling or both input edges.
IPC	Inter-Processor communication

1. Only QFN88 supports QSPI, while QFN48 and QFN68 just support SPI/DSPI.

1.3.2 Wireless

Table 1-2 Wireless features

Items	Description
Wi-Fi	● 802.11 a/b/g/n 1x1, 2.4GHz & 5GHz ● Supports 20MHz/40MHz up to MCS7 ● Low power architecture ● Low power Tx/Rx for short range application @1.85V ● Low power beacon listen mode ● Low power Rx mode ● Very low power suspends mode (DLPS) ● Built-in PA, also supports external PA and LNA ● Supports Antenna diversity ● Internal PTA interface for arbitrating data transmission between Wi-Fi and internal Bluetooth or external 2.4G devices
Bluetooth	● BLE 5.0 ● Both central and peripheral modes ● High power mode (8dbm, shares the same PA with Wi-Fi) ● Internal co-existence mechanism between Wi-Fi and BT to share the same antenna

1.3.3 Security

Table 1-3 Security features

Items	Description
Security	● AES/DES/SHA hardware engine ● Arm TrustZone-M ● Secure boot ● Debug port access protection and prohibition modes ● Secure eFuse ● Flash decryption on-the-fly

1.3.4 Communication Interface

Table 1-4 Communication interface features

Items	Description
SD/SDIO	● SD card host supported ● SDIO 2.0 SDR25 supported ● Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode ● SDIO INIC mode (SDIO to Wi-Fi transformation) ● Clock rate variable up to 50MHz ● Internal DMA supported ● SDIO device time consuming from power on to initialization completion: 64.14635ms
USB	● USB 2.0 ● HS/FS/LS mode ● Internal DMA support, DMA works based on register settings ● 1.5KByte bulk-in buffer and 1.5KByte bulk-out buffer
SPI	● Motorola SPI Serial interface operation ● Master or slave operation mode ● Providing two SPI ports: ■ SPI0 (High speed): configured as master or slave with max. baud rate 50MHz. ■ SPI1 (Normal speed): configured as master with max. baud rate 25MHz. ● DMA interface for DMA transfer supported ● Independent masking of interrupts ● FIFO depth – The transmit and receive FIFO buffers 64 words deep. The FIFO width is fixed at 16-bit.

	● Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device ● Programmable features: ■ Clock bit-rate – Dynamic control of the serial bit rate of the data transfer; used in only serial-master mode of operation. ■ Data item size (4 to 16 bits) – Item size of each data transfer under the control of programmer. ■ Configurable clock polarity and phase ■ Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.
UART (HS_UART/LP_UART)	● UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bit ● Supports up to 6MHz baud rate ● Auto flow control supported ● Interrupt control supported ● IrDA supported ● Loopback mode for test ● Fractional baud rate generator ● Low power mode for Rx path ● Monitor and eliminate Rx baud rate error and own frequency drift automatically for Rx path ● DMA mode supported ■ LP_UART: DMA mode on KM4 platform not supported ● Option for UART Rx to be DMA flow controller
IR (Infra Ray)	● Carrier frequency from 25kHz to 500kHz ● Duty from 1/2 to 1/5 ● IR diode input supported ● IR receiver module input supported ● 32*4 bytes Tx FIFO ● 32*4 bytes Rx FIFO ● Tx carrier frequency can be configured ● Tx carrier duty cycle can be configured
One wire communication (SGPIO)	● One wire communication interface for security element ● Timer Mode: ■ Rx and Multiple Timer are 16-bit timer with a 16-bit prescaler. ■ Rx and Multiple Timer can stop, reset, and interrupt by match events. ■ Rx and multiple timer/counter can stop and reset to each other. ● Capture Mode: ■ Rx timer can be captured by capture events. ■ Capture events can be Rx trigger events or the multiple match events. ■ The capture value can be transferred to '0' or '1' by comparing the value. ● Counter Mode: ■ Multiple Counter can count Rx trigger events. ● External Output Mode: ■ External output can set high, low or toggle on the match event. ● Get the serial input: ■ Shift the input value to a 32-bit FIFO by match events. ● Send the serial output: ■ Send the '0' or '1' waveform by shifting the output value of a 32-bit FIFO. This output value decides that the external match uses the match value of group 0 or group 1. ■ Change the output value by using the multiple FIFO data to update the multiple match value. ● Monitor Mode: ■ Monitor the receiving value to make the interrupt in the power saving mode.
I2C	● Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL) ● One I2C port supported ● Two Speed mode: ■ Standard (up to 100Kbps) ■ Fast (up to 400Kbps)

	● Master or Slave I2C operation ● 7- or 10-bit addressing ● Transmit and receive buffers with depth of 16 ● Tx and Rx DMA ● Multi-master ability including bus arbitration scheme ● Slave mode address match wakeup for power save (up to 100Kbps) ● Clock stretch in master/slave mode ● 7- or 10-bit combined format transfers ● General Call ● Component parameters for configurable software driver support (programmable SDA hold time, slave address, etc.) ● Filter to eliminate the glitches on signal of SDA and SCL. Programmable digital noise Filter. ● Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)

1.3.5 Audio

Table 1-5 Audio features

Items	Description
Audio DAC and earphone driver	● Sampling Frequency: 8/16/32/44.1/48/88.2/96kHz ● Integrates earphone driver ■ 40mW on 16Ω load ■ 20mW on 32Ω load ● Gain Control in DAC Path ■ Gain Step: 0.375dB/step ■ Gain Range: -64.5dB ~ 0dB ● Audio output mode ■ Line-Out Cap-less mode (QFN88) ■ Line-Out Differential mode (QFN88) ■ Line-Out Single-ended mode
Audio ADC	● Sampling Frequency: 8/16/32/44.1/48/88.2/96kHz ● ADC input gain range ■ Gain Step: 0.375dB/step ■ Gain Range: -17.625dB ~ 30dB (digital) ● MIC input boost gain stage: 0/20/30/40dB (analog) ● Audio input mode ■ Line-In ■ Analog MICx2 or Digital MIC x2
I2S	● Sample rate ■ 8/12/16/24/32/48/64/96/192/384/7.35/11.025/14.7/22.05/29.4/44.1/58.8/88.2/176.4kHz ● I2S channel number ■ mono ■ stereo ■ 5.1 channel ● Sample bit for mono ■ 16-bit ■ 32-bit ● Sample bit for stereo & 5.1 channel ■ 16-bit ■ 24-bit ■ 32-bit ● Integrated DMA engine to minimize the software efforts ● Mono and stereo Tx or Rx, or Tx & Rx mode ● 5.1 Tx mode (DAC) supported, Rx mode (ADC) not supported ● PCM mode not supported

1.3.6 Timer

Table 1-6 Timer features

Items	Description
Basic Timers (HS_TIM0 ~ HS_TIM3) (LP_TIM0 ~ LP_TIM3)	● Clock source: 32kHz ● Resolution: 32-bit ● Counter mode: up ● Interrupt generation ● Sleep mode wakeup
PWM Timers (HS_TIM5 & LP_TIM5)	● Channels: 6 ● Clock source: XTAL ● Resolution: 16-bit ● Prescaler: 8-bit ● Counter mode: up ● Statistics pulse width ● Statistics pulse counter ● Interrupt generation ● LP_TIM5 can work at sleep mode
Pulse Timers (HS_TIM4 & LP_TIM4)	● Clock source: XTAL ● Resolution: 16-bit ● Prescaler: 8-bit ● Counter mode: up ● One pulse mode ● PWM mode with polarity selection ● Interrupt generation
Real-Time clock (RTC)	● Independent BCD timer/counter ● Time with seconds, minutes, hours, days (12- or 24-hour format) ● Daylight saving compensation programmable by software ● One programmable alarm with interrupt function. The alarm can be triggered by any combination of the time fields. ● Maskable interrupts/events ■ Alarm ● Digital calibration circuit ● Register write protection

1.3.7 Human-Machine Interaction

Table 1-7 Human- machine interaction features

Items	Description
Key-matrix	● Up to 8*8 (64) Keypad Array with use of 16 GPIOs ● Configurable Rows and Columns of Keypad Array ● Hardware debounce with configurable time at each scan ● Configurable Scan Clock, Scan Interval and Release Time ● Support interrupts, provide interrupts mask, interrupts clear, interrupts status ● Multi-keys detect ● FIFO with width of 12 bits and depth of 16 to store Key Press and Release Events ● Low power mode. Key press event can wakeup CPU from sleep.
Cap-Touch	● 4 capacitive sensor channels ● Automatic channel scan: hardware scan each enabled channel automatically in sequence ● Programmable scan period: sample number and scan interval ● Difference or Absolute threshold judgement mode (with ETC function enable) ■ Automatic environment sensor capacitance tracking and calibration (ETC) ■ Hardware baseline initial automatically ● Automatic baseline and threshold update for different noise environment ● Programmable button debounce function ● Programmable interrupt enabled for each interrupt source

	● 4*12 bits FIFO ● Low power consumption
LCD	● Thin Film Transistor (TFT) color display ● 8-/16-bit MCU I8080 parallel interface ■ Resolution of 8-bit mode, (1024x1024) for still picture display ■ Resolution of 8-bit mode, (645x645) for dynamic display when refresh rate is 30F/S ■ Resolution of 16-bit mode, can be (912x912) for animate display when refresh rate is 30F/S ● 6-/16-bit RGB parallel interface ■ Resolution of 6-bit mode, less than (527x527) for dynamic display when refresh rate is 60F/S ■ Resolution of 16-bit mode, less than (912x912) for animate display when refresh rate is 60F/S ● RGB565 data format for input & output ● Programmable timings for different display panels ● Programmable polarity for HSYNC, VSYNC and Data Enable ● DMA frame buffer for RGB/MCU I/F ● I/O mode for MCU I/F

1.3.8 Analog

Table 1-8 Analog features

Items	Description
Data capture ADC and voltage comparator	● Resolution: 12-bit SAR ● Available channel number ■ 7x external 3.3V channel and 1x 5V channel ■ 3x internal channel ● Configurable input ■ Single-ended ■ Differential with predefined channel pair ● Contain 64 FIFO entries which is 16-bit width ● Multi-Channel DMA support ● Multi sampling trigger sources ■ Software ■ Timer ● 1 low power voltage comparator for battery voltage measurement ● Conversion item control or another FIFO level to trigger wakeup circuit

1.4 Package Comparison

1.4.1 Peripheral Counts

The peripheral counts of RTL872xD under different packages are shown in Table 1-9.

Table 1-9 Peripheral counts under different packages

Item	Peripheral	Description	QFN48		QFN68		QFN88	
			RTL8720DN RTL8720DM	RTL8720DF	RTL8721DM	RTL8721DF	RTL8722DM-VA1	RTL8722DM-VP1
UART	HS_UART0		-	✓	✓	✓	✓	✓
	LP_UART1	Low power mode wakeup	✓	✓	✓	✓	✓	✓
	LP_UART0	LOGUART/low power mode wakeup	✓	✓	✓	✓	✓	✓
SPI	HS_SPI0	Max. 50MHz, Master/Slave	-	✓	✓	✓	✓	✓
	HS_SPI1	Max. 25MHz, Master	✓	✓	✓	✓	✓	✓
RTC	RTC_OUT		✓	✓	✓	✓	✓	✓
	EXT_32K		✓	✓	✓	✓	✓	✓
	LP_TIM4_TRIG	Timer capture	-	✓	✓	✓	✓	✓
	LP_TIM5_TRIG	Timer capture	-	✓	✓	✓	✓	✓

IR	IR		✓	✓	✓	✓	✓	✓
I²C	LP_I²C	Standard (up to 100Kbps) Fast (up to 400Kbps)	✓	✓	✓	✓	✓	✓
SDIO	SDIO 2.0 Device	Max. 50MHz	-	✓	-	-	✓	✓
	SD HOST	Max. 50MHz	-	✓	-	-	✓	✓
PWM	HS_PWM0 ~ 17		8	13	11	12	17	17
	LP_PWM0 ~ 5	Low power mode	4	6	6	6	6	6
I²S	I²S		-	✓	✓	✓	✓	✓
DMIC	DMIC		✓	-	✓	✓	✓	✓
LCD	LCD	● 6-/16-bit RGB mode ● 8-/16-bit MCU mode ● LED mode	-	-	-	-	✓	✓
Q-Decoder	Q-Decoder		-	✓	✓	✓	✓	✓
SGPIO	SGPIO		✓	✓	✓	✓	✓	✓
Key-Scan	Key-Scan		5x2/4x3	5x2/4x3	7x3/5x5	4x8/6x6	4x8/6x6	4x8/6x6
Wake Pin	Wake Pin	Wakeup from deep-sleep	7	7	10	12	12	12
HS Timer	HS_TIM4_TRIG	Timer capture	✓	✓	✓	✓	✓	✓
	HS_TIM5_TRIG	Timer capture	✓	-	✓	✓	✓	✓
Analog Pin	USB	USB host or device (selectable)	✓	✓	✓	✓	✓	✓
	ADC	0 ~ 3.3V	3	3	7	7	7	7
	VBAT_MEAS	0 ~ 5V	-	-	✓	✓	✓	✓
	Cap-Touch		-	-	4	4	4	4
	Audio Output	Analog audio codec output	-	-	Single-ended	Single-ended	Differential Single-ended	Differential Single-ended
	Audio Input	Analog audio codec input	-	-	Single-ended	Single-ended	Differential Single-ended AUXIN	Differential Single-ended

1.4.2 Memory

The memory of RTL872xD under different packages are shown in Table 1-10.

Table 1-10 Memory under different packages

Item	**QFN48**			**QFN68**		**QFN88**
	RTL8720DN	RTL8720DM	RTL8720DF	RTL8721DM	RTL8721DF	RTL8722DM
Embedded Flash	-	-	4M bytes	-	4M bytes	-
Embedded PSRAM	-	4M bytes	-	4M bytes	-	4M bytes

2 Package

2.1 Package Types

There are three package types named QFN48, QFN68 and QFN88 in RTL872xD, the GPIO details are shown in Table 2-1.

Table 2-1 Package types

Port name	QFN48		QFN68		QFN88	
	RTL8720DN RTL8720DM	RTL8720DF	RTL8721DM	RTL8721DF	RTL8722DM-VA1	RTL8722DM-VP1
PA[0]			✓	✓	✓	
PA[1]					✓	
PA[2]			✓	✓	✓	
PA[4]			✓	✓	✓	
PA[5]					✓	
PA[6]					✓	
PA[7]	✓	✓	✓	✓	✓	✓
PA[8]	✓	✓	✓	✓	✓	✓
PA[9]					✓	✓
PA[10]					✓	✓
PA[11]					✓	✓
PA[12]	✓	✓	✓	✓	✓	✓
PA[13]	✓	✓	✓	✓	✓	✓
PA[14]	✓	✓	✓	✓	✓	✓
PA[15][1]	✓	✓	✓	✓	✓	✓
PA[16][1]	✓	✓	✓	✓	✓	✓
PA[17]			✓	✓	✓	✓
PA[18]			✓	✓	✓	✓
PA[19]			✓	✓	✓	✓
PA[20]				✓	✓	✓
PA[21]				✓	✓	✓
PA[22]					✓	✓
PA[23]					✓	✓
PA[24]					✓	✓
PA[25]	✓	✓	✓	✓	✓	✓
PA[26]	✓	✓	✓	✓	✓	✓
PA[27]	✓	✓	✓	✓	✓	✓
PA[28]	✓	✓	✓	✓	✓	✓
PA[30]	✓	✓	✓	✓	✓	✓
PA[31]					✓	✓
PB[0]					✓	✓
PB[1]	✓	✓	✓	✓	✓	✓
PB[2]	✓	✓	✓	✓	✓	✓
PB[3]	✓	✓	✓	✓	✓	✓
PB[4]			✓	✓	✓	✓
PB[5]			✓	✓	✓	✓
PB[6]			✓	✓	✓	✓
PB[7]			✓	✓	✓	✓
PB[8]						✓
PB[9]						✓
PB[10]						✓
PB[11]						✓
PB[12]					✓	✓

PB[13]	✓		✓		✓	✓
PB[14]	✓		✓		✓	✓
PB[15]					✓	✓
PB[16]	✓		✓		✓	✓
PB[17]	✓		✓		✓	✓
PB[18]		✓		✓	✓	✓
PB[19]		✓		✓	✓	✓
PB[20]	✓	✓		✓	✓	✓
PB[21]	✓	✓		✓	✓	✓
PB[22]		✓	✓	✓	✓	✓
PB[23][2]		✓	✓	✓	✓	✓
PB[24][2]		✓				✓
PB[25]						✓
PB[26]			✓	✓		
PB[28]					✓	✓
PB[29]			✓	✓	✓	✓
PB[30]					✓	✓
PB[31]			✓	✓	✓	✓

NOTE

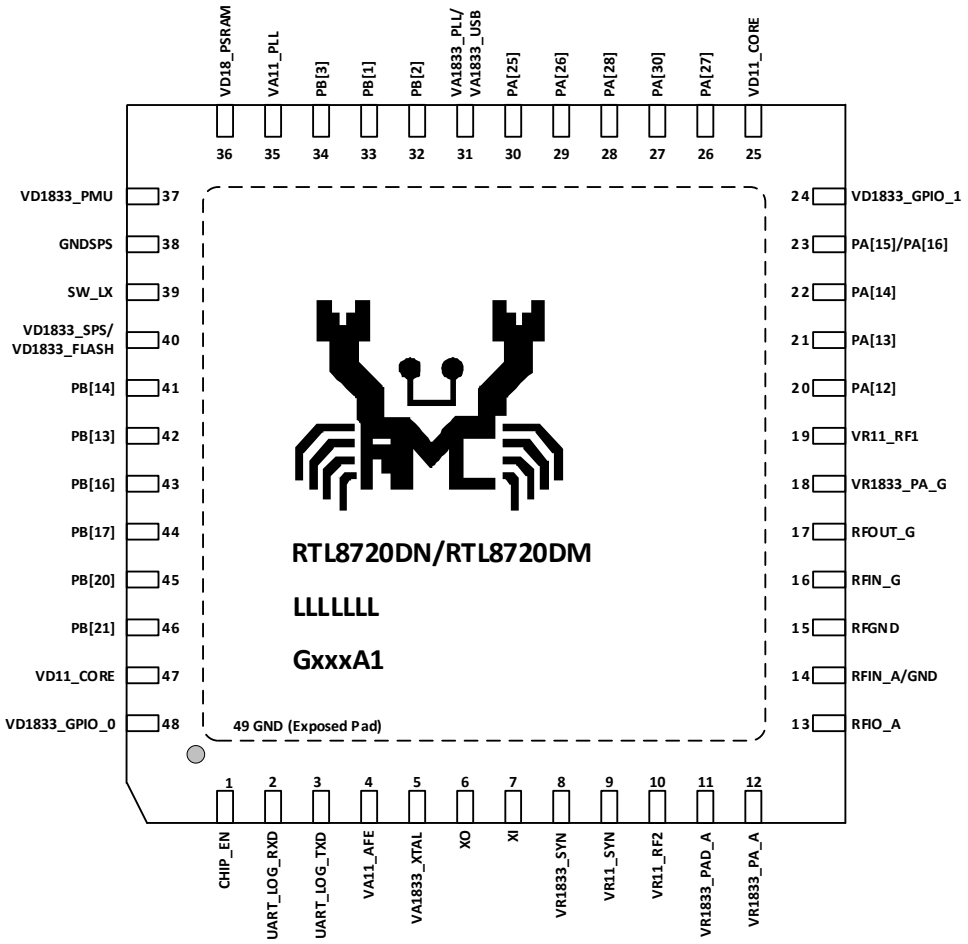
[1] For QFN48 packages, PA[15] & PA[16] are co-bonded and selectable, do not use them at the same time.

[2] For RTL8720DF package, PB[23] and PB[24] are co-bonded and selectable, do not use them at the same time.

2.2 Pin Assignment

2.2.1 QFN48

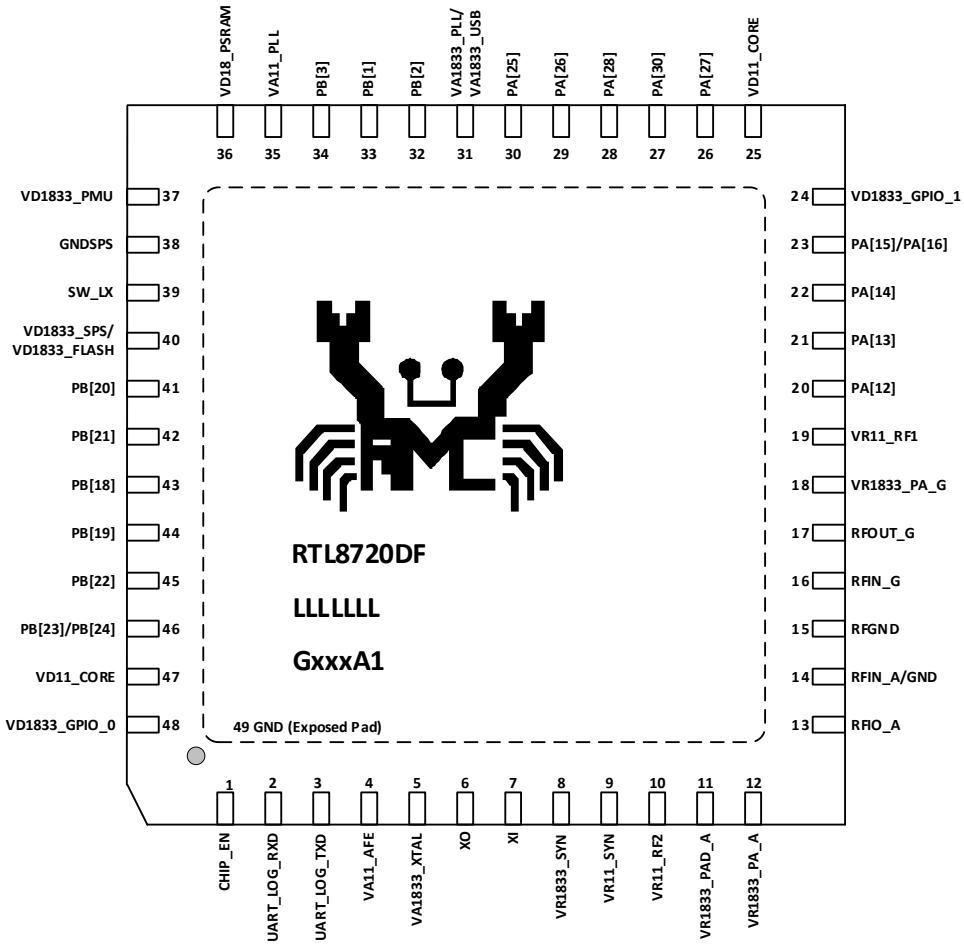
2.2.1.1 RTL8720DN/RTL8720DM



Note: For #23, PA[15] & PA[16] are co-bonded and selectable, do not use them at the same time.

Figure 2-1 Pin assignments of RTL8720DN/RTL8720DM

2.2.1.2 RTL8720DF



Note:

- For #23, PA[15] & PA[16] are co-bonded and selectable, do not use them at the same time.
- For #46, PB[23] & PB[24] are co-bonded and selectable, do not use them at the same time.

Figure 2-2 Pin assignments of RTL8720DF

2.2.2 QFN68

2.2.2.1 RTL8721DM

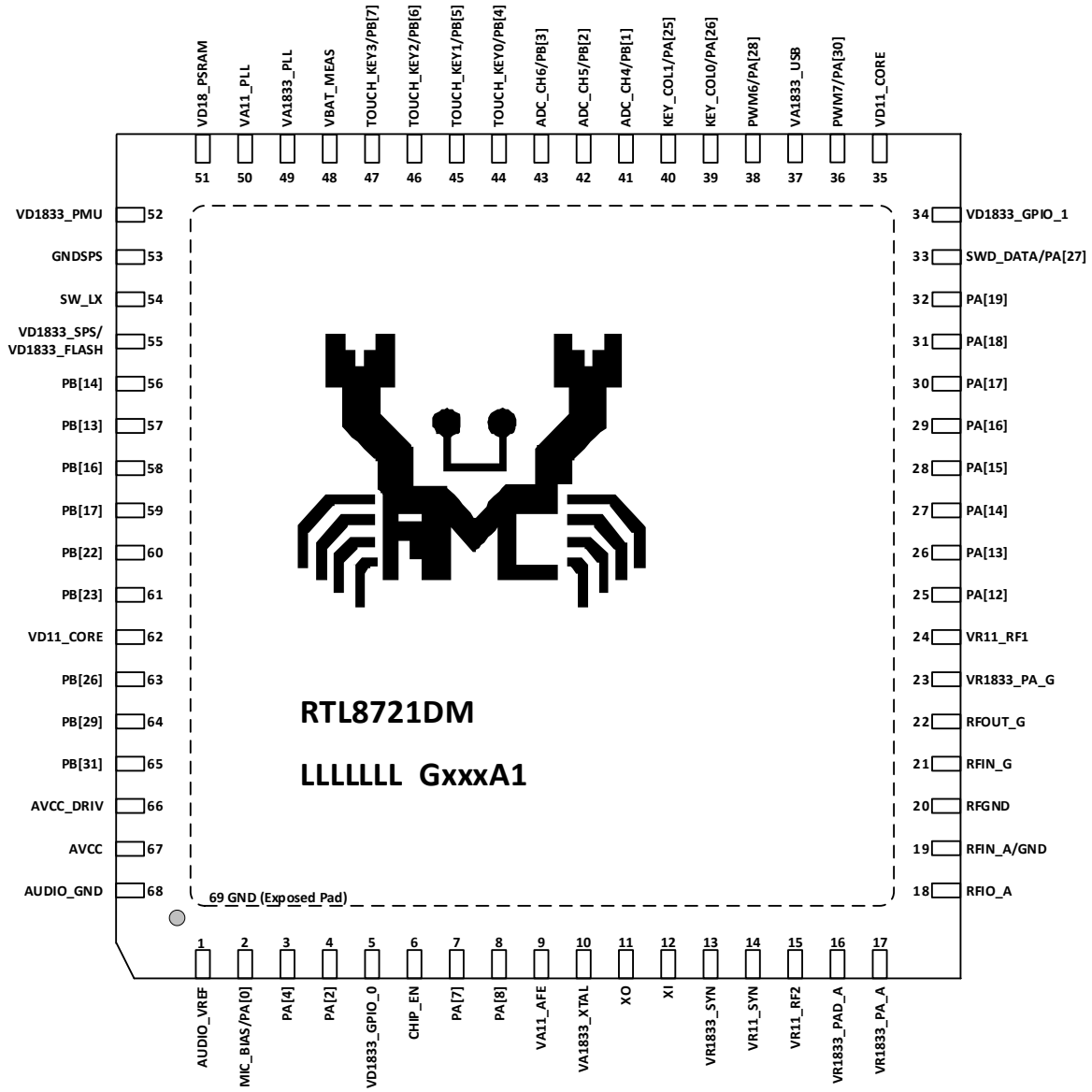


Figure 2-3 Pin assignment of RTL8721DM

2.2.2.2 RTL8721DF

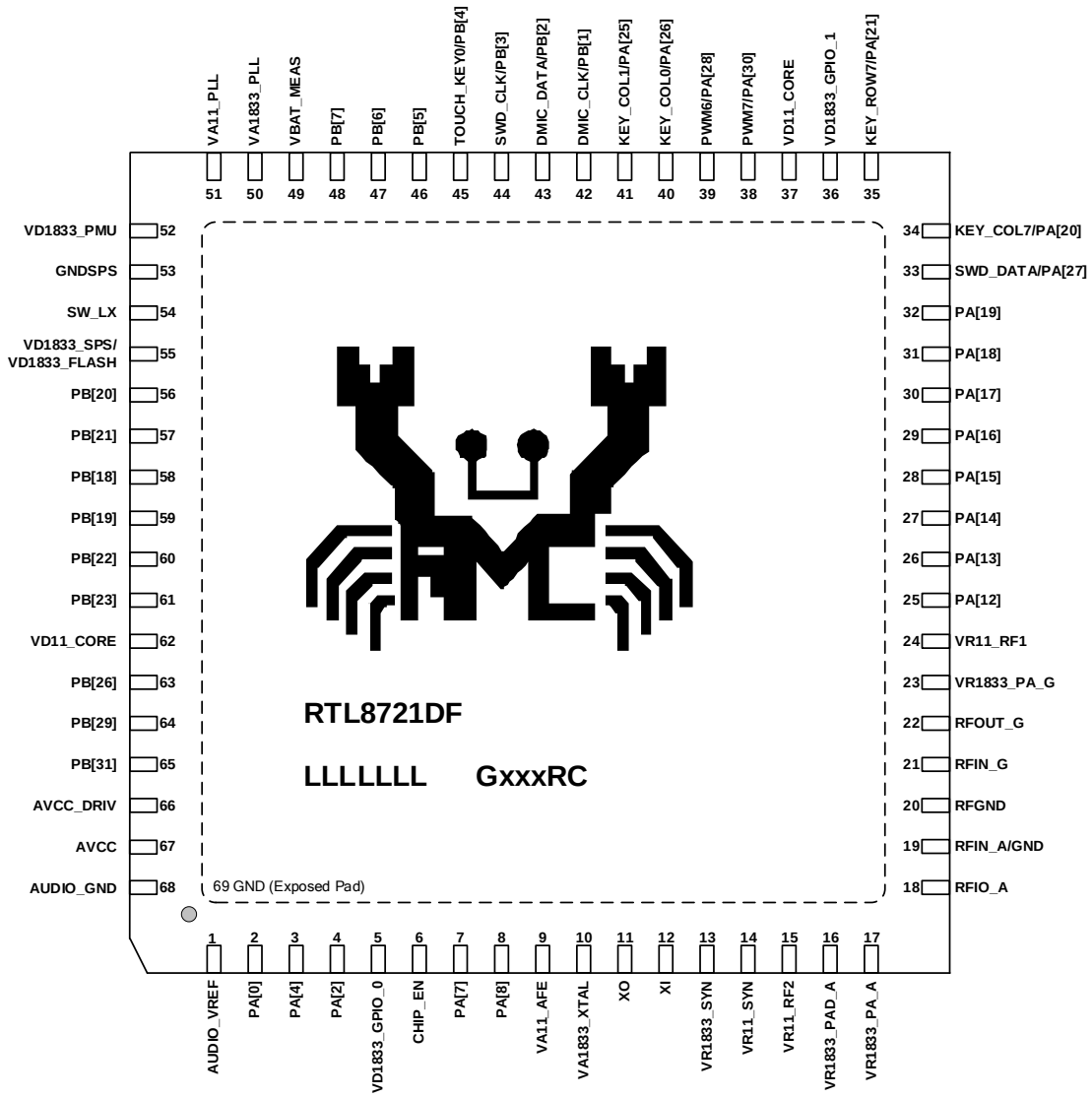


Figure 2-4 Pin assignment of RTL8721DF

2.2.3 QFN88

2.2.3.1 RTL8722DM-VA1

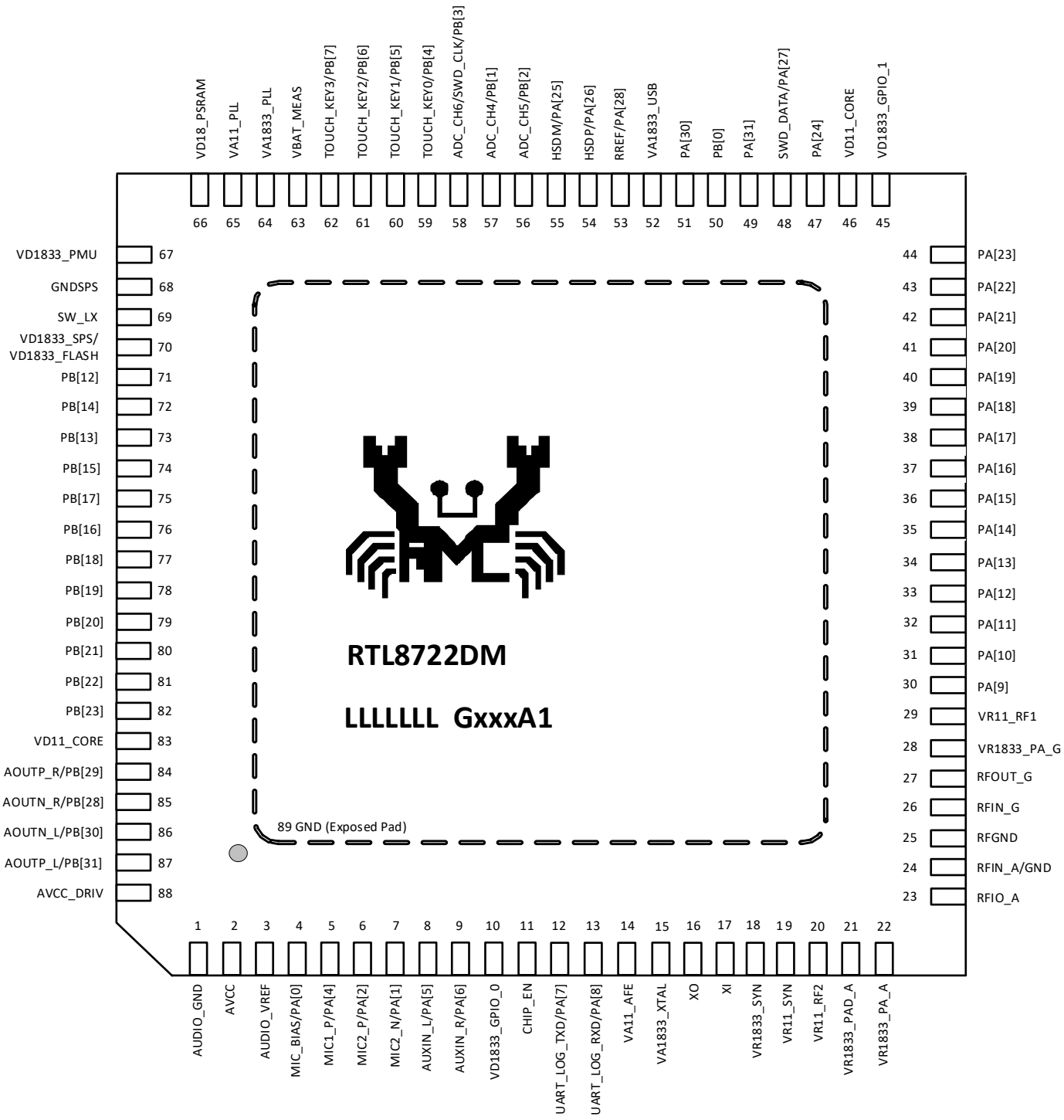


Figure 2-5 Pin assignments of RTL8722DM-VA1

2.2.3.2 RTL8722DM-VP1

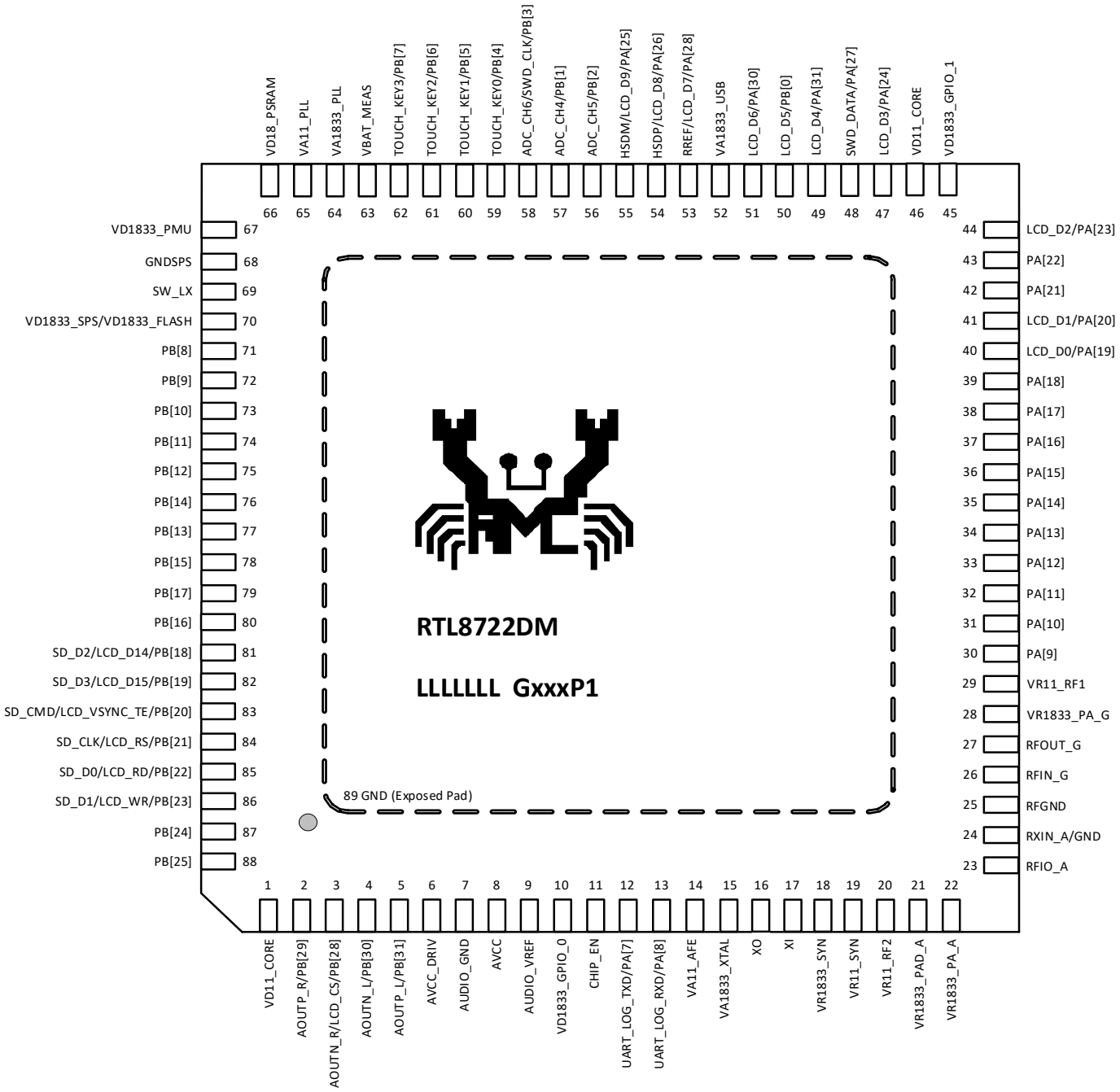


Figure 2-6 Pin assignments of RTL8722DM-VP1

2.3 Low Power Pins

These pins can work and wakeup MCU under deep-sleep mode, as Table 2-2 shows. All these pins are located at Key-Scan pins.

Table 2-2 Low power pins

Pin Name/GPIO	Ext32K	Key-Scan Row	Key-Scan Column	Wakeup
PA[12]		KEY_ROW0		LGPIO[0]
PA[13]		KEY_ROW1		LGPIO[1]
PA[14]	RTC_OUT	KEY_ROW2		LGPIO[2]
PA[15]	RTC EXT_32K	KEY_ROW3	KEY_COL6	LGPIO[3]
PA[16]		KEY_ROW4	KEY_COL5	LGPIO[0]
PA[17]		KEY_ROW6	KEY_COL3	LGPIO[1]
PA[18]	RTC_OUT	KEY_ROW5	KEY_COL4	LGPIO[2]
PA[19]			KEY_COL2	LGPIO[3]
PA[20]			KEY_COL7	LGPIO[0]
PA[21]		KEY_ROW7		LGPIO[1]
PA[25]			KEY_COL1	LGPIO[2]
PA[26]			KEY_COL0	LGPIO[3]

2.4 Pin Default Configuration

All pins are configured as GPIO without pull resistors except some special function like SWD or LOGUART. The pin default configuration is listed in Table 2-3.

Table 2-3 Pin default configuration

Pin Name	Default Function	Default PU/PD
PA[7]	LOGUART	Internal UP
PA[8]	LOGUART	Internal UP
PA[13]	PA[13]	eFuse Pull Control 0
PA[15]	PA[15]	eFuse Pull Control 1
PA[25]	PA[25]	eFuse Pull Control 2
PA[27][1]	SWD_DATA when eFuse enable	Internal UP
PA[28]	PA[28]	eFuse Pull Control 3
PA[30]	PA[30]	External UP
PB[1]	PB[1]	eFuse Pull Control 4
PB[3][1]	SWD_CLK when eFuse enable	No pull
PB[7]	PB[7]	eFuse Pull Control 5
PB[18][2]	SWD_CLK when eFuse enable, or SD_D2 when eFuse enable SDIO	No pull
PB[19][2]	SWD_DATA when eFuse enable, or SD_D3 when eFuse enable SDIO	eFuse Pull Control 6
PB[20]	SD_CMD when eFuse enable SDIO	No pull
PB[21]	SD_CLK when eFuse enable SDIO	No pull
PB[22]	SD_D0 when eFuse enable SDIO	eFuse Pull Control 7
PB[23]	SD_D1 when eFuse enable SDIO	No pull

NOTE

[1] When bit[0] of logical eFuse 0x0E is '0' by default, PA[27] and PB[3] are used for SWD function, and PA[27] is internal pull up.

[2] When bit[0] of logical eFuse 0x0E is programmed to '1', PB[18] and PB[19] are used for SWD function, and PB[19] is internal pull up.

3 Pin Descriptions

Table 3-1 Pin type description

Symbol	Type	Symbol	Type
I	Input pin	O	Output pin
P	Power pin	AH	Analog and digital hybrid programmable pin
PI	Power input pin	PO	Power Output pin

3.1 Power on Trap Pins

Table 3-2 Power on trap pins

Symbol	Type	QFN48	QFN68		QFN88	Description
			RTL8721DM	RTL8721DF		
NORMAL_MODE_SEL	I	26	33	33	48	Shared with PA[27] ● 1: Normal operation mode ● 0: Enter into test/debug mode This pin is not allowed to pull down when power on, otherwise: ● Realtek test mode will be selected. ● Boot will fail.
UART_DOWNLOAD	I	3	7	7	12	Shared with PA[7], low active ● 1: Boot from Flash ● 0: Download image from UART
SPS_SEL	I	27	36	38	51	Shared with PA[30] ● 1: Internal 1.1V regulator works at SPS mode ● 0: Internal 1.1V regulator works at LDO mode

3.2 RF Pins

Table 3-3 RF pins

Symbol	Type	QFN48	QFN68	QFN88	Description
RFGND	P	15	20	25	RF ground
RFIO_A	I/O	13	18	23	WL 5GHz RF signal
RXIN_A/GND	I	14	19	24	WL 5GHz RF input signal or RF ground
RFIN_G	I	16	21	26	WL/BT 2.4GHz RF input signal
RFOUT_G	O	17	22	27	WL/BT 2.4GHz RF output signal

3.3 Chip Enable Pin

Table 3-4 Chip enable pin

Symbol	Type	QFN48	QFN68	QFN88	Description
CHIP_EN	I	1	6	11	Enable chip ● 1: Enable chip ● 0: Shut down chip

3.4 Power Pins

Table 3-5 Power pins

Symbol	Type	QFN48	QFN68		QFN88		Description
			RTL8721DM	RTL8721DF	RTL8721DM-VA1	RTL8721DM-VP1	
VA1833_XTAL	P	5	10	10	15	15	1.85V/3.3V power for Crystal Oscillator
VA11_AFE	P	4	9	9	14	14	1.1V power for WL/BT Analog Front End
VR1833_SYN	P	8	13	13	18	18	1.85V/3.3V power for RF Synthesizer
VR11_SYN	P	9	14	14	19	19	1.1V power for RF Synthesizer
VR1833_PA_A	P	12	17	17	22	22	1.85V/3.3V power for RF 5G Power amplifier
VR1833_PAD_A	P	11	16	16	21	21	1.85V/3.3V power for RF
VR11_RF2	P	10	15	15	20	20	1.1V power for RF 5G path
VR1833_PA_G	P	18	23	23	28	28	1.85V/3.3V power for RF 2.4G Power amplifier
VR11_RF1	P	19	24	24	29	29	1.1V power for RF 2.4G path
VD11_CORE	P	47, 25	62, 35	62, 37	83, 46	1, 46	1.1V power for digital core power
VD1833_SPS/ VD1833_FLASH	P	40	55	55	70	70	1.85V/3.3V power for Flash I/O power and internal regulator input from 1.85V/3.3V to 1.1V
SW_LX	P	39	54	54	69	69	1.1V power output from Switching/Linear Regulator
GNDSPS	P	38	53	53	68	68	Ground for Switching/Linear Regulator
VA1833_USB	P	31	37	36	52	52	3.3V power for USB analog
VA1833_PLL	P	31	49	50	64	64	1.85V/3.3V power for PLL
VA11_PLL	P	35	50	51	65	65	1.1V power for PLL
VD18_PSRAM	P	36	51	-	66	66	1.85V power output from internal linear regulator for PSRAM
VD1833_PMU	P	37	52	52	67	67	1.85V/3.3V power for Power Management Unit
AVCC_DRIV	P	-	66	66	88	6	1.85V/3.3V power supply for internal audio codec LDO.
AVCC	P	-	67	67	2	8	AVCC output from internal audio codec LDO, add a 1uF cap as close as possible.
AUDIO_VREF	P	-	1	1	3	9	Codec bandgap reference output, add a 4.7nF cap as close as possible.
MIC_BIAS	P	-	2	2	4	-	Microphone bias output
VD1833_GPIO	P	24, 48	5, 34	5, 36	10, 45	10, 45	1.85V/3.3V power for digital GPIO
AUDIO_GND	P	-	68	68	1	7	Audio ground

3.5 XTAL Pins

Table 3-6 XTAL pins

Symbol	Type	QFN48	QFN68	QFN88	Description
XI	I	7	12	17	Input of 40MHz Crystal Clock Reference
XO	O	6	11	16	Output of 40MHz Crystal Clock Reference

3.6 ADC and Cap-Touch Pins

Table 3-7 ADC and Cap-Touch pins

Symbol	Type	QFN48	QFN68		QFN88	Description
			RTL8721DM	RTL8721DF		
ADC_0/TOUCH_KEY0	I	-	44	45	59	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_1/TOUCH_KEY1	I	-	45	46	60	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_2/TOUCH_KEY2	I	-	46	47	61	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_3/TOUCH_KEY3	I	-	47	48	62	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_4	I	33	41	42	57	ADC input pin, 3.3V tolerance
ADC_5	I	32	42	43	56	ADC input pin, 3.3V tolerance
ADC_6	I	34	43	44	58	ADC input pin, 3.3V tolerance
VBAT_MEAS	I	-	48	49	63	ADC input pin, 5V tolerance

When the pin is configured as ADC function, it is not necessary to set the pad status, which should be NO PULL.

Table 3-8 ADC pad status

Pin Function	Func PU/PD	Slp PU/PD	DSlp PU/PD
ADC	NO PULL	KEEP	KEEP

3.7 USB Pins

Table 3-9 USB pins

Symbol	Type	QFN48	QFN68		QFN88	Description
			RTL8721DM	RTL8721DF		
HSDP	I/O	29	39	40	54	USB differential bus
HSDM	I/O	30	40	41	55	USB differential bus
RREF	I	28	38	39	53	External reference resistor for USB analog, 1% accuracy

3.8 Audio Codec Pins

Table 3-10 Audio codec pins

Symbol	Type	QFN48	QFN68	QFN88		Description
				RTL8722DM-VA1	RTL8722DM-VP1	
MIC1_P	AH	-	3	5	-	The pin can be configured as digital I/O or analog input. ● Analog input: MIC1 input positive ● Digital I/O: programmable GPIO, pull high/low input configurable It is used as main MIC in dual MIC application.
MIC2_N	AH	-	-	7	-	The pin can be configured as digital I/O or analog input. ● Analog input: MIC2 input ● Digital I/O: programmable GPIO, pull high/low input configurable It is used as main MIC in dual MIC application.
MIC2_P	AH	-	4	6	-	The pin can be configured as digital I/O or analog input. ● Analog input: MIC2 input positive ● Digital I/O: programmable GPIO, pull high/low input configurable It is used as 2nd MIC in dual MIC application.
AOUTN_R	AH	-	-	85	3	The pin can be configured as digital I/O or analog output. ● Analog output: Right channel output negative ● Digital I/O: programmable GPIO, pull high/low input configurable
AOUTP_R	AH	-	64	84	2	The pin can be configured as digital I/O or analog output. ● Analog output: Right channel output positive ● Digital I/O: programmable GPIO, pull high/low input configurable
AOUTN_L	AH	-	-	86	4	The pin can be configured as digital I/O or analog output. ● Analog output: Left channel output negative ● Digital I/O: programmable GPIO, pull high/low input configurable
AOUTP_L	AH	-	65	87	5	The pin can be configured as digital I/O or analog output. ● Analog output: Left channel output positive ● Digital I/O: programmable GPIO, pull high/low input configurable
AUXIN_R	AH	-	-	9	-	The pin can be configured as digital I/O or analog input. ● Analog input: Right channel AUX input ● Digital I/O: programmable GPIO, pull high/low input configurable
AUXIN_L	AH	-	-	8	-	The pin can be configured as digital I/O or analog input. ● Analog input: Right channel AUX input ● Digital I/O: programmable GPIO, pull high/low input configurable
AVCC_DRIV	PI	-	66	88	6	1.85V/3.3V power supply for internal audio codec LDO.
MIC_BIAS	PO	-	2	4	-	Microphone bias output
AUDIO_VREF	PO	-	1	3	9	Codec bandgap reference output, add a 4.7nF capacitor as close as possible.
AVCC	PO	-	67	2	8	AVCC output from internal audio codec LDO, add a 1uF capacitor as close as possible.
AUDIO_GND	PO	-	68	1	7	Audio ground

NOTE

These pins are multiplexed but recommended to be used as audio pins in priority. If audio function is not needed in your application, you can use them as normal GPIOs.

4 Memory Organization

4.1 Introduction

The RTL872xD incorporates several distinct memory regions. Program memory, data memory, registers and I/O ports are organized within the same linear 4Gbytes address space. The bytes are coded in memory in Little-Endian format.

The addressable memory space is divided into multiple main blocks, as shown in Table 4-1. All the memory areas that are not allocated to on-chip memories and peripherals are considered “RSVD” (reserved).

Table 4-1 Address space main blocks

Base Address	Top Address	Size	Function	Description
0x0000_0000	0x0001_FFFF	128KB	KM0 ITCM ROM (actually 96KB)	32MB: KM0 Memory Address
0x0002_0000	0x0002_7FFF	32KB	KM0 DTCM ROM (actually 16KB)	
0x0002_8000	0x0007_FFFF	352KB	RSVD	
0x0008_0000	0x0008_FFFF	64KB	KM0 SRAM	
0x0009_0000	0x000B_FFFF	192KB	RSVD	
0x000C_0000	0x000C_3FFF	16KB	Retention SRAM (actually 1KB) (the same port with KM0 SRAM)	
0x000C_4000	0x000F_FFFF	240KB	RSVD	
0x0010_0000	0x01FF_FFFF	31MB	RSVD	
0x0200_0000	0x07FF_FFFF	96MB	External PSRAM	224MB: External Memory Address
0x0800_0000	0x0FFF_FFFF	128MB	External Flash	
0x1000_0000	0x1007_FFFF	512KB	KM4 SRAM	256MB: KM4 Memory Address
0x1008_0000	0x100D_FFFF	384KB	RSVD	
0x100E_0000	0x100F_FFFF	128KB	Extension SRAM (the same port with KM4 SRAM)	
0x1010_0000	0x101B_FFFF	768KB	KM4 ITCM ROM (actually 256KB)	
0x101C_0000	0x101D_7FFF	96KB	KM4 DTCM ROM	
0x101D_8000	0x101F_FFFF	160KB	RSVD	
0x1020_0000	0x1FFF_FFFF	254MB	RSVD	
0x2000_0000	0x3FFF_FFFF	512MB	RSVD	Reserved
0x4000_0000	0x47FF_FFFF	128MB	KM4 Peripherals	KM4 Peripherals Address
0x4800_0000	0x4FFF_FFFF	128MB	KM0 Peripherals	KM4 Peripherals Secure Address
0x5000_0000	0x57FF_FFFF	128MB	KM4 Peripherals Secure	KM0 Peripherals Address
0x5800_0000	0xDFFF_FFFF	2176MB	RSVD	Reserved
0xE000_0000	0xE0FF_FFFF	16MB	System PPB Device	RAM predefined
0xE100_0000	0xFFFF_FFFF	496MB	RSVD	Reserved

For the detailed mapping of available memory and register areas, refer to the following sections.

4.2 KM4 Memory

4.2.1 Memory Map and Register Boundary Addresses

Table 4-2 gives the boundary addresses of the peripherals available in the KM4 devices.

Table 4-2 KM4 register boundary addresses

Port Name	Security	Base Address	Top Address	Size
KM4_SRAM1	IDAU	0x1000_0000	0x1003_FFFF	256KB
KM4_SRAM2	IDAU	0x1004_0000	0x1007_FFFF	256KB
Extension SRAM	IDAU	0x100E_0000	0x100F_FFFF	128KB
PSRAM Memory	IDAU	0x0200_0000	0x07FF_FFFF	96MB

HS_SYSON	Non-Secure	0x4000_0000	0x4000_0FFF	4KB
	Secure	0x5000_0000	0x5000_0FFF	4KB
HS_TIM0 ~ 3/4/5	Non-Secure	0x4000_2000	0x4000_2FFF	4KB
HS_UART0	Non-Secure	0x4000_4000	0x4000_4FFF	4KB
HS_IPC	Non-Secure	0x4000_6000	0x4000_6FFF	4KB
HS_UART1 (Bluetooth)	Non-Secure	0x4000_A000	0x4000_AFFF	4KB
RXI300_KM4	Non-Secure	0x4000_C000	0x4000_CFFF	4KB
	Secure	0x5000_C000	0x5000_CFFF	4KB
HS_SPI1	Non-Secure	0x4000_E000	0x4000_E7FF	2KB
Audio Codec	Non-Secure	0x4001_0000	0x4001_0FFF	4KB
HS_IR	Non-Secure	0x4001_2000	0x4001_2FFF	4KB
PSRAM Controller	Non-Secure	0x4001_4000	0x4001_4FFF	4KB
I^2S	Non-Secure	0x4002_0000	0x4002_03FF	1KB
Secure Engine	Non-Secure	0x4002_2000	0x4002_5FFF	16KB
	Secure	0x5002_2000	0x5002_5FFF	16KB
SDIO Host	Non-Secure	0x4002_6000	0x4002_9FFF	16KB
HS_GDMA0	Non-Secure	0x4002_A000	0x4002_BFFF	8KB
	Secure	0x5002_A000	0x5002_BFFF	8KB
SDIO Device	Non-Secure	0x4002_C000	0x4002_FFFF	16KB
USB	Non-Secure	0x4004_0000	0x4006_FFFF	192KB
LCD Controller	Non-Secure	0x4007_0000	0x4007_4FFF	20KB
HS_SPI0	Non-Secure	0x4007_8000	0x4007_87FF	2KB
Wi-Fi	Non-Secure	0x4008_0000	0x400A_FFFF	192KB
KM0 BRG	Non-Secure	0x0008_0000	0x0008_FFFF	64KB
		0x000C_0000	0x000C_3FFF	16KB
		0x4800_0000	0x4803_FFFF	256KB
Flash Controller	Non-Secure	0x4808_0000	0x4808_0FFF	4KB
Flash Memory	IDAU	0x0800_0000	0x0FFF_FFFF	128MB

4.2.2 Embedded SRAM

The KM4 contains up to a total 512KB of contiguous, on-chip static RAM memory. This embedded SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits). It is divided into the following two blocks which can be accessed by both KM4 and KM0.

- KM4 SRAM1 (up to 256KB)
- KM4 SRAM2 (up to 256KB)

Dividing SRAM into two slave ports allows user's program to potentially obtain better performance. For example, simultaneous access to SRAM1 by the CPU and by the system DMA controller does not result in any bus stalls for either master.

Generally speaking, the CPU reads or writes all peripheral data at some point, even when all such data is read from or sent to a peripheral by DMA. So, minimizing stalls is likely to involve putting data to/from different peripherals in RAM on each port.

Alternatively, sequences of data from the same peripheral can be alternated between RAM on each port. This could be helpful if DMA fills or empties a RAM buffer, and signals the CPU before proceeding on to a second buffer. The CPU then tends to access the data while the DMA is using the other RAM.

In power domains, the entire SRAM is also divided into three blocks:

- SRAM_PD1 (up to 256KB)
- SRAM_PD2 (up to 128KB)
- SRAM_PD3 (up to 128KB)

Each block can be disabled or enabled individually in the Power Management Unit (PMU) block to save power, and the entire SRAM can also keep power for quickly resuming from sleep mode when system enters sleep mode.

4.2.3 Extension SRAM

When Bluetooth is disabled, more 64KB SRAM will be extended. This SRAM can also be accessed by both KM4 and KM0, up to 50MHz*32 bits.

4.3 KM0 Memory

4.3.1 Memory Map and Register Boundary Addresses

Table 4-3 gives the boundary addresses of the peripherals available in the KM0 devices.

Table 4-3 KM0 register boundary addresses

Port Name	Base Address	Top Address	Size
KM0_SRAM	0x0008_0000	0x0008_FFFF	64KB
1KB Retention SRAM	0x000C_0000	0x000C_3FFF	16KB
KM4 BRG	0x1000_0000	0x1007_FFFF	512KB
	0x4000_0000	0x4007_FFFF	512KB
Wi-Fi FW	0x4008_0000	0x400A_FFFF	192KB
LP_SYSON	0x4800_0000	0x4800_0FFF	4KB
LP_TIM0 ~ 3/4/5	0x4800_2000	0x4800_2FFF	4KB
LP_RTC	0x4800_4000	0x4800_43FF	1KB
LP_IPC	0x4800_6000	0x4800_63FF	1KB
Key-Scan	0x4800_A000	0x4800_A3FF	1KB
I^2C0	0x4800_C000	0x4800_C3FF	1KB
UART3	0x4800_E000	0x4800_E3FF	1KB
LP_GDMA0	0x4801_0000	0x4801_07FF	2KB
UART2 (LOGUART)	0x4801_2000	0x4801_23FF	1KB
GPIOA/B	0x4801_4000	0x4801_47FF	2KB
RXI300_KM0	0x4801_8000	0x4801_8FFF	4KB
SGPIO	0x4801_A000	0x4801_AFFF	4KB
Cap-Touch	0x4801_C000	0x4801_C7FF	2KB
ADC	0x4801_C800	0x4801_CBFF	1KB
Comparator	0x4801_CC00	0x4801_CFFF	1KB
Q-Decoder	0x4801_E000	0x4801_EFFF	4KB
Flash Controller	0x4808_0000	0x4808_0FFF	4KB
Flash Memory	0x0800_0000	0x0FFF_FFFF	128MB

4.3.2 Embedded SRAM

The KM0 features 64KB of system SRAM, the embedded SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits).

This SRAM can be accessed by both KM4 and KM0.

4.4 Retention SRAM

The RTL872xD features 1KB of retention SRAM in order to allow saving data with minimal power usage during deep-sleep mode.

This SRAM can be accessed by both KM4 and KM0.

4.5 SPI Flash Memory

The SPI Flash Controller manages CPU I-Code and D-Code accesses to the Flash memory. It implements the erase and program Flash memory operations, and the read/write protection mechanisms. It accelerates code execution with a system of instruction prefetch and cache lines.

4.6 PSRAM

4MB 8IO DDR PSRAM is included in RTL872xD, up to 50MHz DDR.

5 Radio Characteristics

5.1 RF Block Diagram

The radio frequency (RF) block diagram of RTL872xD, including Wi-Fi modem and BLE modem, is given in Figure 5-1.

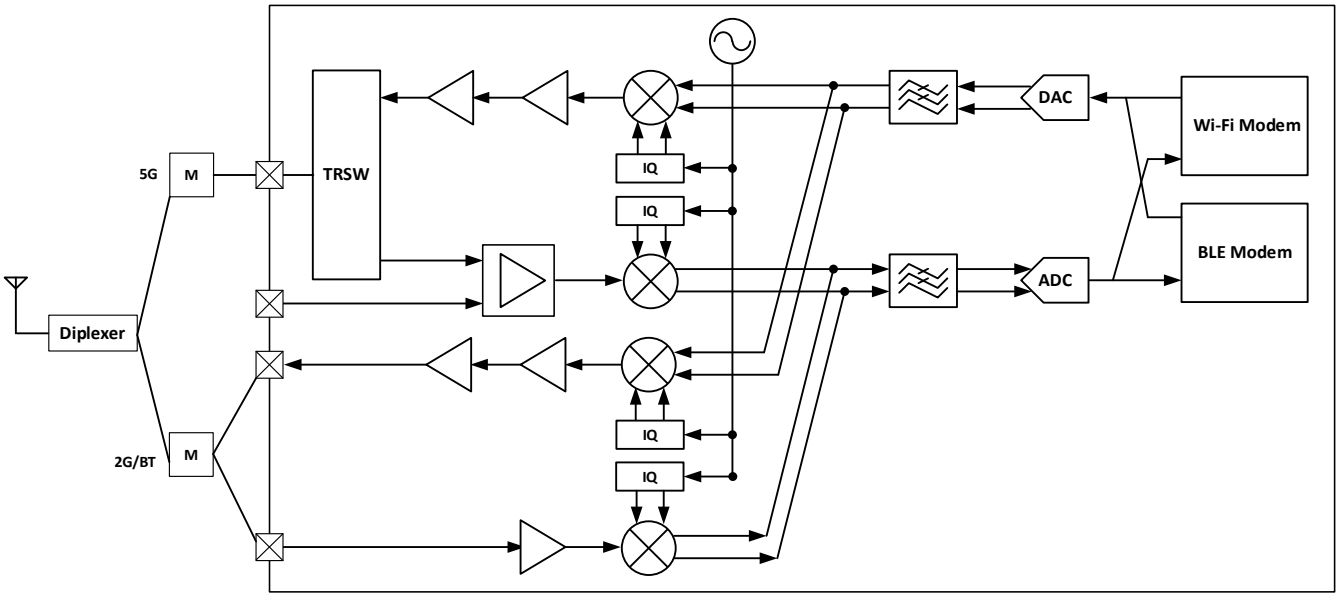


Figure 5-1 RF block diagram

5.2 Wi-Fi Radio Characteristics

The RF specifications of Wi-Fi are described in the tables below. These values are measured on the QFN68 board.

5.2.1 Wi-Fi 2.4GHz Band RF Receiver Specifications

Parameter	Description	Performance (1.85V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412	-	2484	2412	-	2484	MHz
Rx Sensitivity	1Mbps CCK	-	-98	-	-	-98	-	dBm
	2Mbps CCK	-	-96	-	-	-96	-	
	5.5Mbps CCK	-	-94	-	-	-94	-	
	11Mbps CCK	-	-91	-	-	-91	-	
Rx Sensitivity	BPSK rate 1/2, 6Mbps OFDM	-	-96	-	-	-95	-	dBm
	BPSK rate 3/4, 9Mbps OFDM	-	-94	-	-	-94	-	
	QPSK rate 1/2, 12Mbps OFDM	-	-93	-	-	-93	-	
	QPSK rate 3/4, 18Mbps OFDM	-	-90	-	-	-90	-	
	16QAM rate 1/2, 24Mbps OFDM	-	-87	-	-	-87	-	
	16QAM rate 3/4, 36Mbps OFDM	-	-84	-	-	-84	-	
	64QAM rate 1/2, 48Mbps OFDM	-	-79	-	-	-79	-	
	64QAM rate 3/4, 54Mbps OFDM	-	-77	-	-	-77	-	
Rx Sensitivity BW = 20MHz	MCS 0, BPSK rate 1/2	-	-95	-	-	-95	-	dBm
	MCS 1, QPSK rate 1/2	-	-92	-	-	-92	-	

Mixed Mode 800ns Guard Interval Non-STBC	MCS 2, QPSK rate 3/4	-	-89	-	-	-89	-	
	MCS 3, 16QAM rate 1/2	-	-86	-	-	-86	-	
	MCS 4, 16QAM rate 3/4	-	-83	-	-	-83	-	
	MCS 5, 64QAM rate 2/3	-	-78	-	-	-78	-	
	MCS 6, 64QAM rate 3/4	-	-77	-	-	-77	-	
	MCS 7, 64QAM rate 5/6	-	-75	-	-	-75	-	
Rx Sensitivity BW = 40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-	-93	-	-	-93	-	dBm
	MCS 1, QPSK rate 1/2	-	-89	-	-	-89	-	
	MCS 2, QPSK rate 3/4	-	-86	-	-	-86	-	
	MCS 3, 16QAM rate 1/2	-	-83	-	-	-83	-	
	MCS 4, 16QAM rate 3/4	-	-80	-	-	-80	-	
	MCS 5, 64QAM rate 2/3	-	-75	-	-	-75	-	
	MCS 6, 64QAM rate 3/4	-	-74	-	-	-74	-	
	MCS 7, 64QAM rate 5/6	-	-72	-	-	-72	-	
Maximum Receive Level	6Mbps OFDM	-	0	-	-	0	-	dBm
	54Mbps OFDM	-	0	-	-	0	-	
	MCS 0	-	0	-	-	0	-	
	MCS 7	-	0	-	-	0	-	
Receive Adjacent Channel Rejection	1Mbps CCK	-	43	-	-	43	-	dB
	11Mbps CCK	-	40	-	-	41	-	
	BPSK rate 1/2, 6Mbps OFDM	-	40	-	-	40	-	
	64QAM rate 3/4, 54Mbps OFDM	-	22	-	-	22	-	
	HT20, MCS 0, BPSK rate 1/2	-	39	-	-	39	-	
	HT20, MCS 7, 64QAM rate 5/6	-	20	-	-	20	-	
	HT40, MCS 0, BPSK rate 1/2	-	30	-	-	29	-	
	HT40, MCS 7, 64QAM rate 5/6	-	11	-	-	10	-	

5.2.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications

Parameter	**Description**	**Performance (1.85V)**			**Performance (3.3V)**			**Unit**
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412	-	2484	2412	-	2484	MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK	-	14	15	-	20	21	dBm
	11Mbps CCK	-	12	15	-	18	21	
	BPSK rate 1/2, 6Mbps OFDM	-	14	15	-	20	21	
	64QAM rate 3/4, 54Mbps OFDM	-	11	12	-	17	18	
	HT20-MCS 0, BPSK rate 1/2	-	13	14	-	19	20	
	HT20-MCS 7, 64QAM rate 5/6	-	10	11	-	16	17	
	HT40-MCS 0, BPSK rate 1/2	-	13	14	-	19	20	
	HT40-MCS 7, 64QAM rate 5/6	-	10	11	-	16	17	
Tx EVM	BPSK rate 1/2, 6Mbps OFDM	-	-	-5	-	-	-5	dB
	64QAM rate 3/4, 54Mbps OFDM	-	-	-25	-	-	-25	
	HT20-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	
	HT20-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	
	HT40-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	
	HT40-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	
Output power variation[2]	After do power trim at FT	-1.5	-	1.5	-1.5	-	1.5	dBm
Carrier suppression		-	-	-30	-	-	-30	dBm
Harmonic output power (IC port)	2nd harmonic	-	-36	-34	-	-23	-21.9	dBm
	3rd harmonic	-	-26	-24	-	-15	-14	

NOTE

[1] The power level is tested after Digital Pre-Distortion (DPD) enable.

[2] The VDD18 voltage is within ±5% of typical value.

5.2.3 Wi-Fi 5GHz Band RF Receiver Specifications

Parameter	Description	Performance (1.85V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180	-	5825	5180	-	5825	MHz
Rx Sensitivity	BPSK rate 1/2, 6Mbps OFDM	-	-94	-	-	-93	-	dBm
	BPSK rate 3/4, 9Mbps OFDM	-	-93	-	-	-93	-	
	QPSK rate 1/2, 12Mbps OFDM	-	-92	-	-	-92	-	
	QPSK rate 3/4, 18Mbps OFDM	-	-89	-	-	-89	-	
	16QAM rate 1/2, 24Mbps OFDM	-	-86	-	-	-86	-	
	16QAM rate 3/4, 36Mbps OFDM	-	-83	-	-	-83	-	
	64QAM rate 1/2, 48Mbps OFDM	-	-78	-	-	-78	-	
	64QAM rate 3/4, 54Mbps OFDM	-	-76	-	-	-76	-	
Rx Sensitivity BW = 20MHz HT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-	-94	-	-	-93	-	dBm
	MCS 1, QPSK rate 1/2	-	-91	-	-	-91	-	
	MCS 2, QPSK rate 3/4	-	-88	-	-	-88	-	
	MCS 3, 16QAM rate 1/2	-	-85	-	-	-85	-	
	MCS 4, 16QAM rate 3/4	-	-82	-	-	-82	-	
	MCS 5, 64QAM rate 2/3	-	-77	-	-	-77	-	
	MCS 6, 64QAM rate 3/4	-	-76	-	-	-75	-	
	MCS 7, 64QAM rate 5/6	-	-74	-	-	-74	-	
Rx Sensitivity BW = 40MHz HT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-	-91	-	-	-91	-	dBm
	MCS 1, QPSK rate 1/2	-	-88	-	-	-88	-	
	MCS 2, QPSK rate 3/4	-	-85	-	-	-85	-	
	MCS 3, 16QAM rate 1/2	-	-82	-	-	-82	-	
	MCS 4, 16QAM rate 3/4	-	-79	-	-	-79	-	
	MCS 5, 64QAM rate 2/3	-	-74	-	-	-74	-	
	MCS 6, 64QAM rate 3/4	-	-73	-	-	-73	-	
	MCS 7, 64QAM rate 5/6	-	-71	-	-	-71	-	
Maximum Receive Level	6Mbps OFDM	-	0	-	-	0	-	dBm
	54Mbps OFDM	-	0	-	-	0	-	
	MCS 0	-	0	-	-	0	-	
	MCS 7	-	0	-	-	0	-	
Receive Adjacent Channel Rejection	BPSK rate 1/2, 6Mbps OFDM	-	21	-	-	21	-	dB
	64QAM rate 3/4, 54Mbps OFDM	-	12	-	-	11	-	
	HT20, MCS 0, BPSK rate 1/2	-	21	-	-	19	-	
	HT20, MCS 7, 64QAM rate 5/6	-	7	-	-	7	-	
	HT40, MCS 0, BPSK rate 1/2	-	30	-	-	30	-	
	HT40, MCS 7, 64QAM rate 5/6	-	12	-	-	13	-	

5.2.4 Wi-Fi 5GHz Band RF Transmitter Specifications

Parameter	Description	Performance (1.85V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180	-	5825	5180	-	5825	MHz
Output power with spectral mask and EVM compliance[1]	BPSK rate 1/2, 6Mbps OFDM	-	12	13	-	18	19	dBm
	64QAM rate 3/4, 54Mbps OFDM	-	9	10	-	14	15	
	HT20-MCS 0, BPSK rate 1/2	-	11	12	-	17	18	
	HT20-MCS 7, 64QAM rate 5/6	-	8	9	-	13	14	
	HT40-MCS 0, BPSK rate 1/2	-	11	12	-	17	18	
	HT40-MCS 7, 64QAM rate 5/6	-	8	9	-	13	14	
Tx EVM	BPSK rate 1/2, 6Mbps OFDM	-	-	-5	-	-	-5	dB
	64QAM rate 3/4, 54Mbps OFDM	-	-	-25	-	-	-25	

	HT20-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	
	HT20-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	
	HT40-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	
	HT40-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	
Output power variation[2]	After doing power trim at FT	-1.5	-	1.5	-1.5	-	1.5	dBm
Carrier suppression		-	-	-30	-	-	-30	dBm

NOTE

[1] The power level is tested after Digital Pre-Distortion (DPD) enable.
[2] The VDD18 voltage is within ±5% of typical value.

5.3 BT Radio Characteristics

The RF specifications of BT are described in the tables below. Both the transmitter specifications and the receiver specifications basically follow the Bluetooth SIG specifications.

5.3.1 BT RF Transmitter Specifications

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
Tx Output Power	LE1M	-10	4.5	10	dBm
	LE2M				
Modulation Characteristics (LE1M)	ΔF1 Avg.	225		275	kHz
	ΔF2 Max.	185			kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8			
Modulation Characteristics (LE2M)	ΔF1 Avg.	450		550	kHz
	ΔF2 Max.	370			kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8			
Modulation Characteristics Stable Modulation (LE1M)	ΔF1 Avg.	247.5		252.5	kHz
	ΔF2 Max.	185			kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8			
Modulation Characteristics Stable Modulation (LE2M)	ΔF1 Avg.	495		505	kHz
	ΔF2 Max.	370			kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8			

5.3.2 BT RF Receiver Specifications

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range		2402	-	2480	MHz
Rx Sensitivity	LE1M	-100.9	-	-	dBm
	LE2M	-96.8	-	-	

6 Electrical Characteristics

6.1 Parameters Definitions

6.1.1 Minimum and Maximum Values

Unless otherwise specified, all data are guaranteed by design, simulation and samples test to be applicable to all declared temperature, voltage ranges and processes, and are not tested in production.

6.1.2 Typical Values

Unless otherwise specified, the typical values are reference results when the IC is at an ambient temperature of 25°C and an operating voltage of 3.3V. This value is for reference design only and is not actually tested.

6.1.3 Pin Status

6.1.3.1 Loading Capacitor

Unless otherwise specified, the load refers to the equivalent capacitance mounted on the chip pin. Schematic diagram used for loading capacitor measurements is illustrated in Figure 6-1.

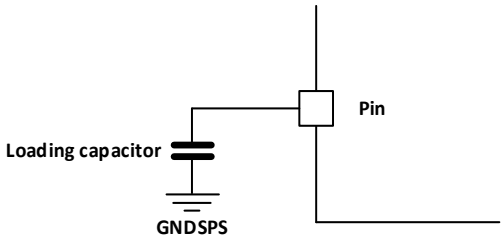


Figure 6-1 Loading capacitor diagram of pin

6.1.3.2 Input Voltage

Unless otherwise specified, the input voltage of the chip pin refers to the voltage difference between the pin and ground. The schematic diagram is illustrated in Figure 6-2.

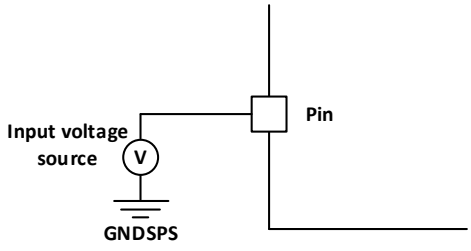


Figure 6-2 Input voltage diagram of pin

6.2 Absolute Maximum Ratings

Stresses beyond absolute maximum ratings may cause permanent damage to the device. These are emphasized ratings only and do not imply the functional operation of the device. All voltages are defined with respect to GNDSPS.

Table 6-1 Absolute maximum ratings

Symbol	Description	Condition	Min.	Max.	Unit
VA1833_XTAL, VR1833_SYN, VR1833_PA_A, VR1833_PAD_A, VR1833_PA_G, VD1833_SPS/ VD1833_FLASH, VA1833_USB, VA1833_PLL, VD1833_PMU, VD1833_GPIO_0, VD1833_GPIO_1, AVCC_DRIV	External supply voltage	Input DC voltage at power pin	-0.3	3.63	V
VD18_PSRAM	External supply voltage	Input DC voltage at power pin	-0.3	1.98	V
V_{IN}	Input voltage on PAx & PBx pins	Input DC voltage at digital I/O pin, VD1833_GPIO≤3.63V	-0.3	VD1833_GPIO+0.3	V
	Input voltage on MICx & LINEx pins	Input DC voltage at analog pin, AVCC_DRIV≤3.63V		AVCC_DRIV+0.3	
P_ANT	Maximum power at receiver	Input RF power at antenna pin		0	dBm
T_{STORE}	Storage temperature range		-65	+150	°C
MSL	Moisture Sensitivity Level			MSL3	
HBM	ESD Human Body Model	T_A = 25°C, conforming to JESD22-A114F		Class 2	
CDM	ESD Charged Device Model	T_A = 25°C, conforming to JESD22-C101F		Class C2	

6.3 Power Consumption

Table 6-2 Specification of power consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{deep-sleep}$	Deep-sleep power consumption (VDD=3.3V)	CPU OFF RF OFF Interrupt OFF SRAM: 1K retained I/O: 12 I/O retained		10		uA
	Deep-sleep power consumption (VDD=1.85V)			10		
I_{sleep}	Sleep power consumption (VDD=3.3V)	KM4 power-gating KM0 clock-gating RF OFF Interrupt ON SRAM: all retained I/O: all retained		75		uA
	Sleep power consumption (VDD=1.85V)			89		
I_{active}	Active mode power consumption (VDD=3.3V)	KM0 & KM4 idle RF OFF KM4: 200MHz		20		mA
	Active mode power consumption (VDD=1.85V)			40		
I_{RF}	RF Tx mode power consumption (VDD=3.3V)	1T-MCS7/BW40M (15dBm@2G)		206		mA
		1T-MCS7/BW40M (15dBm@5G)		286		
		1T-Legacy OFDM54M (19dBm@2G)		262		
		1T-Legacy OFDM54M (18dBm@5G)		325		
	RF Tx mode power consumption (VDD=1.85V)	1T-MCS7/BW40M (12dBm@2G)		205		
		1T-MCS7/BW40M (11dBm@5G)		222		
		1T-Legacy OFDM54M (13dBm@2G)		201		
		1T-Legacy OFDM54M (12dBm@5G)		229		
	RF Rx mode power consumption (VDD=3.3V)	1R-MCS7/BW40M (Pin= -60dBm@2G)		63		
		1R-MCS7/BW40M (Pin= -60dBm@5G)		65		

		1R-Idle/BW40 @2G		50		
		1R-Idle/BW40 @5G		51		
	RF Rx mode power consumption (VDD=1.85V)	1R-MCS7/BW40M (Pin= -60dBm@2G)		100		
		1R-MCS7/BW40M (Pin= -60dBm@5G)		103		
		1R-Idle/BW40 @2G		80		
		1R-Idle/BW40 @5G		80		
I_{VDD33}[1]	3.3V rating current (with internal regulator and integrated CMOS PA)				450[2]	mA
I_{VDD18}[1]	1.85V rating current (with internal regulator and integrated CMOS PA)				800	mA

NOTE

[1] I_{VDD33} is for 3.3V supply voltage, and I_{VDD18} is for 1.85V supply voltage, to supply pins VA1833_XTAL, VR1833_SYN, VR1833_RF2, VR1833_RF1, VR1833_PA_G, VA1833_USB, VA1833_PLL, VD1833_PMU, VD1833_SPS/VD1833_FLASH, AVCC_DRIV, VD1833_GPIO_0, and VD1833_GPIO_1.

[2] The maximum Peak Current is 800mA when Digital Pre-Distortion (DPD) enable.

[3] The typical values listed in the table are the overall IC power consumption at room temperature (25°C).

6.4 Power Sequence

Table 6-3 Timing specification of power sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{PRDY}	VDD*x* ready time	0.1	0.6	4.6	ms
T_{CORE}	HS core power ready time		15	-	ms
T_{BOOT}	HS MCU boot time	200	200	-	ms
V_{PD_LOW}	Power-down low voltage	0	0	0.3	V
V_{RST}	Shutdown occurs after CHIP_EN lower than this voltage	0	0	0.2 * VDD*x*	V
T_{RST}	Required time that CHIP_EN lower than V_{RST}	1	1	-	ms

NOTE

- *VDDx indicates the power supply of VA1833_XTAL, VR1833_SYN, VR1833_PA_A, VR1833_PAD_A, VR1833_PA_G, VA1833_USB, VA1833_PLL, VD1833_PMU, AVCC_DRIV, VD1833_SPS/VD1833_FLASH, and VD1833_GPIO_0. VDD_IO indicates the power supply of VD1833_GPIO_1. VDDx, VDD_IO, and CHIP_EN in the timing sequence are all from the same power source, so their behaviors are the same.*
- *HS core power ready time T_{CORE} is characterized under 3.3V power supply and 25°C.*
- *During power-on, the voltage needs to rise steadily, and needs to rise above 1.76V or 2.97V (depending on whether the IC is powered by 1.85V or 3.3V) within the required time.*
- *During power-down, the voltage needs to drop below V_{PD_LOW} before the IC can be powered-on again.*
- *There is no restriction whether the CHIP_EN is pulled up before or after VD1833 is pulled up. After the voltage of VD1833 is stabilized, IC can enter shutdown mode by pulling CHIP_EN down, and pulling the CHIP_EN up again to re-initialize. The time of pulling CHIP_EN down should be no less than 1ms.*

6.4.1 Power-on or Resuming from Deep-sleep Sequence

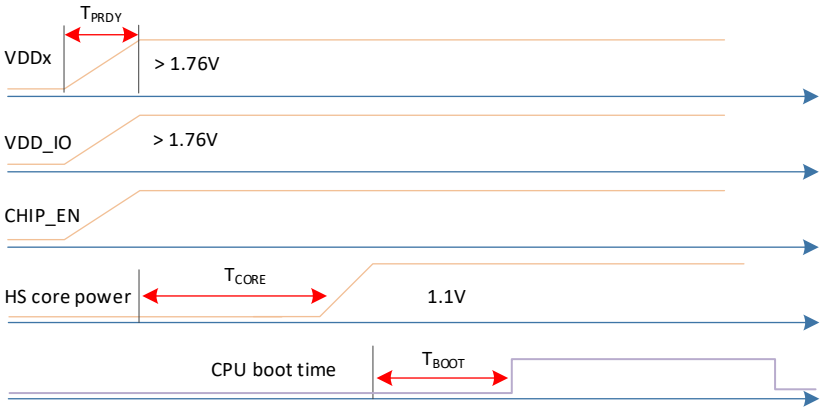


Figure 6-1 Timing sequence of power on or resuming from deep-sleep

6.4.2 Power-down Sequence

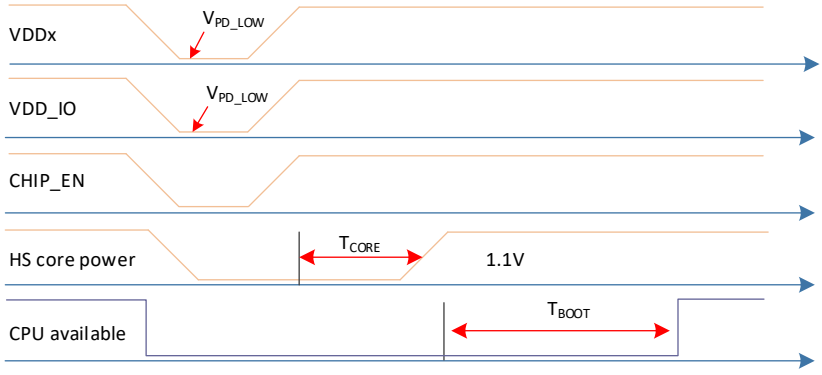


Figure 6-2 Timing sequence of power-down

6.4.3 Shutdown Sequence

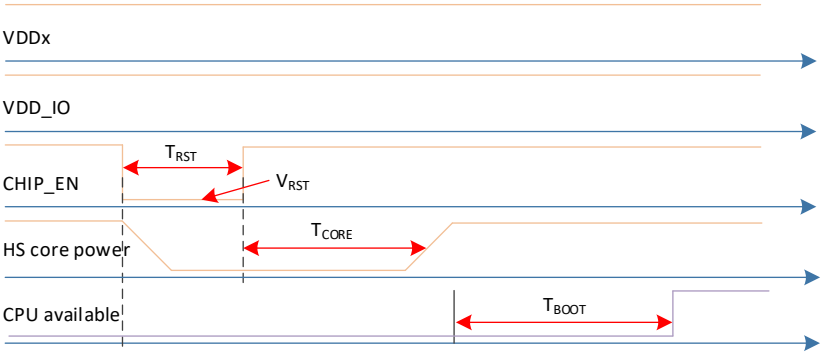


Figure 6-3 Timing sequence of shutdown

6.5 Crystal Characteristics

The RTL872xD has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned. The characteristic requirements of external crystal oscillator are listed in Table 6-4.

Table 6-4 Characteristic requirements of external crystal oscillator

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
Equivalent series resistance (ESR)			40	ohms
Typical load capacitance (CL)			12	pF
Shunt capacitance (Co)			2	pF

6.6 DC Characteristics

The direct current (DC) characteristics of power supply and digital I/O pin are illustrated in the following sections.

6.6.1 Operation Conditions

Table 6-5 Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VA1833_XTAL, VR1833_SYN, VR1833_PA_A, VR1833_PAD_A, VR1833_PA_G, VA1833_USB, VA1833_PLL, VD1833_PMU, AVCC_DRIV, VD1833_SPS/VD1833_FLASH, VD1833_GPIO_0[1]	Power pin voltage	2.97	3.3	3.63	V
	Power pin voltage	1.76	1.85	2.03	V
VD18_PSRAM	Power pin voltage	1.7	1.85	1.95	V
VA11_AFE, VR11_SYN, VR11_RF1, VR11_RF2, VD11_CORE, VA11_PLL	Power pin voltage	1.05	1.1	1.21	V
VD1833_GPIO_1[2]	Digital I/O supply voltage	1.76	1.85/3.3	3.63	V
T_J	Junction temperature	-40	-	+125	°C

NOTE

[1] All these power pins must be powered by the same voltage. For IC's stable performance, voltage ripple on these pins is suggested to be under +/-75mV.

[2] Power for VD1833_GPIO_1 needs to be not higher than power for VD1833_GPIO_0.

There are some restrictions both for the application of 1.85V supply voltage and 3.3V supply voltage.

- On 1.85V supply voltage module, make sure that external or internal Flash can work normally under expected power supply range.
- On 3.3V supply voltage module, make sure that your circuit satisfy the following two points; otherwise, you should refer to HDK to add a Reset IC.
  - The power-on voltage waveform is consistent with Figure 6-4.
  - The power-off voltage can drop to under 0.3V finally.

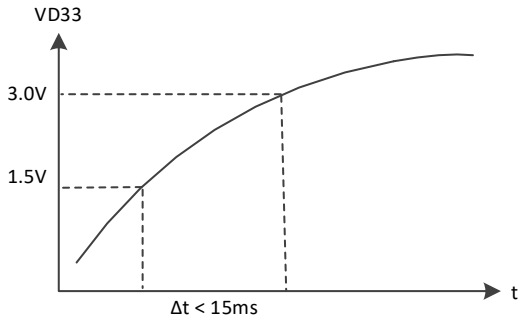


Figure 6-4 Power-on waveform

6.6.2 Digital I/O Pin

Table 6-6 Digital I/O pin DC characteristics (3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input-High Voltage	CMOS level	2.0	-	-	V
V_{IL}	Input-Low Voltage	CMOS level	-	-	0.8	V
V_{OH}	Output-High Voltage	CMOS level VDD=3.3V±10% I_{OH} max.	2.4	-	-	V
V_{OL}	Output-Low Voltage	TTL level VDD=3.3V±10% I_{OL} max.	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level	-	1.78	1.87	1.97	V
V_{T-}	Schmitt-trigger Low Level	-	1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	V_{IN} = 3.3V or 0	-10	±1	10	μA
C_{IN}	Input Capacitance	-	-	3.7	-	pF

NOTE

For the values of I_{OH} max. and I_{OL} max., refer to Table 6-8.

Table 6-7 Digital I/O pin DC characteristics (1.85V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input-High Voltage	CMOS level	0.65 * Vcc	-	-	V
V_{IL}	Input-Low Voltage	CMOS level	-	-	0.35 * Vcc	V
V_{OH}	Output-High Voltage	CMOS level VDD=3.3V±10% I_{OH} max.	Vcc –0.45	-	-	V
V_{OL}	Output-Low Voltage	CMOS level VDD=3.3V±10% I_{OL} max.	-	-	0.45	V
V_{T+}	Schmitt-trigger High Level	-	1.02	1.09	1.14	V
V_{T-}	Schmitt-trigger Low Level	-	0.67	0.73	0.87	V
I_{IL}	Input-Leakage Current	V_{IN} = 1.85V or 0	-10	±1	10	μA
C_{IN}	Input Capacitance	-	-	3.7	-	pF

NOTE

For the values of I_{OH} max. and I_{OL} max., refer to Table 6-8.

6.7 GPIO Characteristics

6.7.1 GPIO Types

Table 6-8 I_{OH} and I_{OL} with 3.3V and 1.85V power supply

Pad type	Pin name		Driving strength[1] (3.3V)		Driving strength[1] (1.85V)		Internal pull resistor (kΩ)			Resistor available in deep-sleep mode?
	PA	PB	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	Min.	Typ.	Max.	
Normal	PA[7] PA[8] PA[9] PA[10] PA[11] PA[22] PA[23] PA[24] PA[27] PA[28]	PB[8] PB[9] PB[10] PB[11] PB[12] PB[13] PB[14] PB[15] PB[16] PB[17]	4/8/12/16	4/8/12/16	2/4/6/8	2/4/6/8	25	50	75	Yes
SDIO		PB[18] PB[19] PB[20] PB[21] PB[22] PB[23] PB[24] PB[25]	4~16	4~16	2~8	2~8	25	50	75	Yes
Key-Scan	PA[12] PA[13] PA[14] PA[15] PA[16] PA[17] PA[18] PA[19] PA[20] PA[21] PA[25] PA[26]		8/16	8/16	4/8	4/8	2.3/25	4.7/50	7.1/75	Yes
Audio[2]	PA[0] PA[1] PA[2] PA[3] PA[4] PA[5] PA[6]	PB[28] PB[29] PB[30] PB[31]	8/16	8/16	4/8	4/8	PU: 23.9 PL: 17.9	PU: 29 PL: 26	PU: 38.9 PL: 42.3	No
Cap-Touch		PB[4] PB[5] PB[6] PB[7]	4/8	4/8	2/4	2/4	25	50	75	Yes
I2C	PA[29] PA[30] PA[31]	PB[0] PB[1] PB[2] PB[3] PB[26] PB[27]	8/16	8/16	4/8	4/8	2.3/5	4.7/10	7.1/15	Yes

NOTE

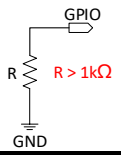
[1] All I/Os support 1.85V and 3.3V I/O power, and the driving capability is related to the I/O powers. Refer to Table 6-6 and Table 6-7 for V_{OH} and V_{OL}.

[2] In deep-sleep mode, the audio pins (PA[0] ~ PA[6] and PB[28] ~ PB[31]) are in floating state, and the internal resistors of these pins are not available. If the circuit connected with these GPIOs needs to be pulled to high or low state, external resistor on PCB is needed. In other modes except deep-sleep mode, internal resistors of all GPIOs are available.

6.7.2 GPIO Pull Low Restriction

When one of the GPIOs listed below needs to be pulled low by a resistor on PCB, the pull low resistor value must > 1kΩ.

Table 6-9 GPIO pull low resister value

Port Name	Schematic	Resistor Value
PA[7] ~ PA[31] PB[0] ~ PB[3] PB[8] ~ PB[17] PB[26] PB[27]		R > 1kΩ

6.8 ADC Characteristics

Table 6-10 SAR ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_s	ADC sample frequency		31.25	167	250	kHz
V_{IN}	Conversion input voltage range	Normal channel single-ended	0	-	Min(3.3, V_{DDA})	V
		Normal channel differential	0	-	Min(3.3, V_{DDA})/2	
		VBAT_MEAS	0	-	5	
R	Input impedance	Normal channel	450	550	650	kΩ
		VBAT_MEAS	80	100	120	
I_{DDA}	Power consumption	V_{DDA} = 1.76V ~ 3.63V -40°C ~ +125°C	177	190	425	uA
Resolution			-	12	-	Bits
EO	Offset error	fs = 167kHz V_{DDA} = 3.3V T = 25°C	-	-	16	LSB
EG	Gain error		-	-	16	
INL	Integral linearity error		-	-	16	
DNL	Differential linearity error		-	-	3	
SFDR	Spurious Free Dynamic Range		-	48	-	dB
THD	Total harmonic distortion		-	-46	-	
SNR[1]	Signal-to-noise ratio		62	-	-	
ENOB[1]	Effective number of bits		10	-	-	bits

NOTE

[1] It is the ADC performance which does not include harmonic distortion.

6.9 BOR Characteristics

Table 6-11 BOR characteristics

Symbol	Parameter	Conditions[2]	Min	Typ.	Max.	Unit
V_{INT_H2L}[1]	Brown-out detection voltage of interrupt mode	VDD drops from 3.3V linearly	-10%	2.5	+10%	V
V_{INT_L2H}[1]	Brown-out release voltage of interrupt mode	VDD rises from 1.85V linearly	-10%	2.6	+10%	V
V_{RST_H2L}[1]	Brown-out detection voltage of reset mode	VDD drops from 3.3V linearly	-10%	2.05	+10%	V
V_{RST_L2H}[1]	Brown-out release voltage of reset mode	VDD rises from 1.85V linearly	-10%	2.15	+10%	V

NOTE

[1] The voltage is steady state level.

[2] BOR threshold is characterized under default setting. The default BOD_REG setting is 0x100. Refer to AN0400 (Chapter: Brownout Detector) for more information about high/low threshold voltage values of interrupt mode and reset mode.

6.10 SPI Characteristics

The SPI has the following features:

- Providing two SPI ports:
  - SPI0: configured as master or slave with maximum baud rate 50MHz.
  - SPI1: configured as master with maximum baud rate 25MHz.
- Limited choices with fixed group usage, that is to say, only the specified pins configured as function ID3 can be used in combination:
  - SPI0 Group1 (PA[16], PA[17], PA[18], PA[19])
  - SPI0 Group2 (PB[18], PB[19], PB[20], PB[21])
  - SPI1 Group1 (PA[12], PA[13], PA[14], PA[15])
  - SPI1 Group2 (PB[4], PB[5], PB[6], PB[7])

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.76V to 2.03V.
- The process includes all corners.
- Refer to section 6.6.2 for the definitions of $V_{OH(min)}$, $V_{OL(max)}$, $V_{IH(min)}$, and $V_{IL(max)}$.

6.10.1 Timing Data

Table 6-12 Timing data of SPI0

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.85V I/O (1.76V~2.03V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	20	-	20	-	ns
		Slave	40	-	40	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	$1.5*T_{SCL} - 2$	-	$1.5*T_{SCL} - 2$	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
		Slave	-	14	-	19	ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-2	2	-2	2	ns
		Slave	-	15	-	20	ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	2	-	2	-	ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	1	-	1	-	ns

NOTE

- *The maximum value of $t_{VD;DAT(SO)}$ is already greater than half of a clock cycle, so when used as a slave, the maximum speed supported by SPI is 25MHz. But if the connected master supports sampling with a delay, it could support a higher speed.*
- *The timing data of $t_{SU;DAT(MI)}$ is only applicable to speeds of 25MHz or below. When the chip is used as a master running at 50MHz, due to the sample delay function of IC, the accepted minimum value of $t_{SU;DAT(MI)}$ can be -16ns.*

Table 6-13 Timing data of SPI1

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.85V I/O (1.76V~2.03V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	40	-	40	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
$t_{su;CS(M)}$	CS setup time	Master	$1.5*T_{SCL} - 2$	-	$1.5*T_{SCL} - 2$	-	ns
$t_{HD;CS(M)}$	CS hold time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
$t_{AC;DAT(MO)}$	Data output access time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
$t_{VD;DAT(MO)}$	Data output valid time	Master	-2	2	-2	2	ns
$t_{SU;DAT(MI)}$	Data input setup time	Master	4	-	4	-	ns
$t_{HD;DAT(MI)}$	Data input hold time	Master	2	-	2	-	ns

6.10.2 Timing Diagram

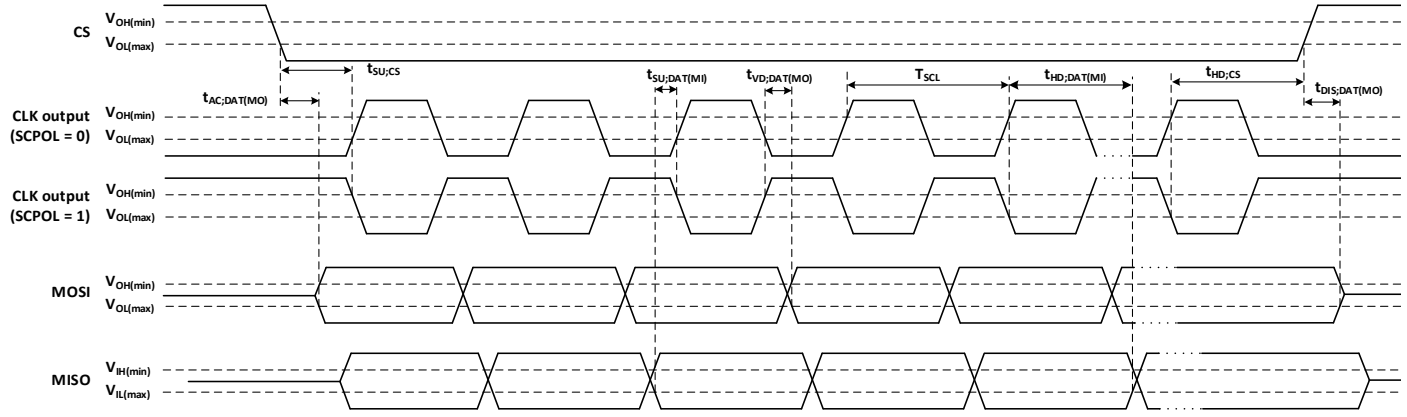


Figure 6-5 SPI timing diagram – master (SCPH = 0)

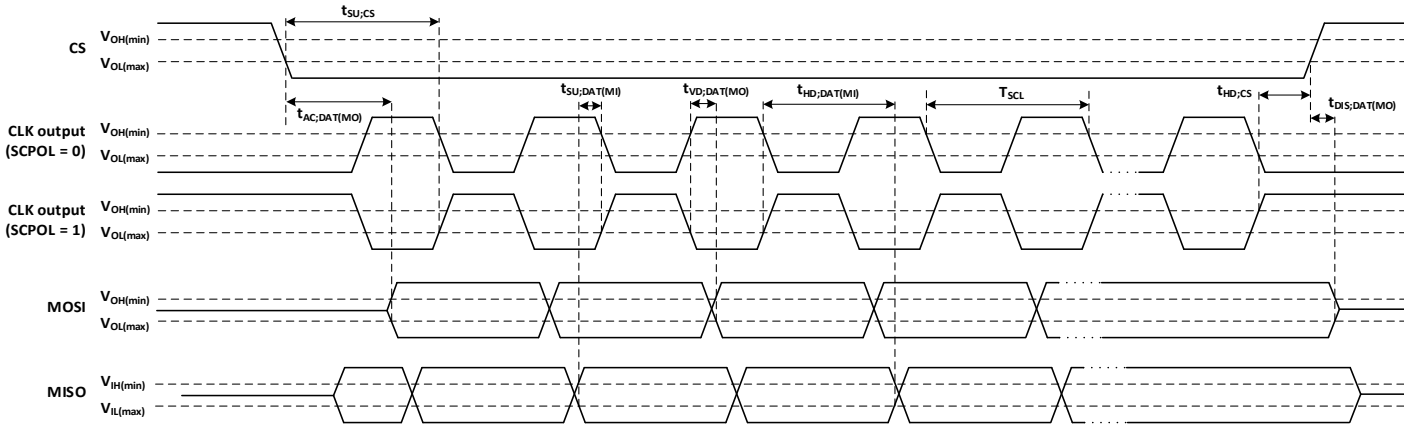


Figure 6-6 SPI timing diagram – master (SCPH = 1)

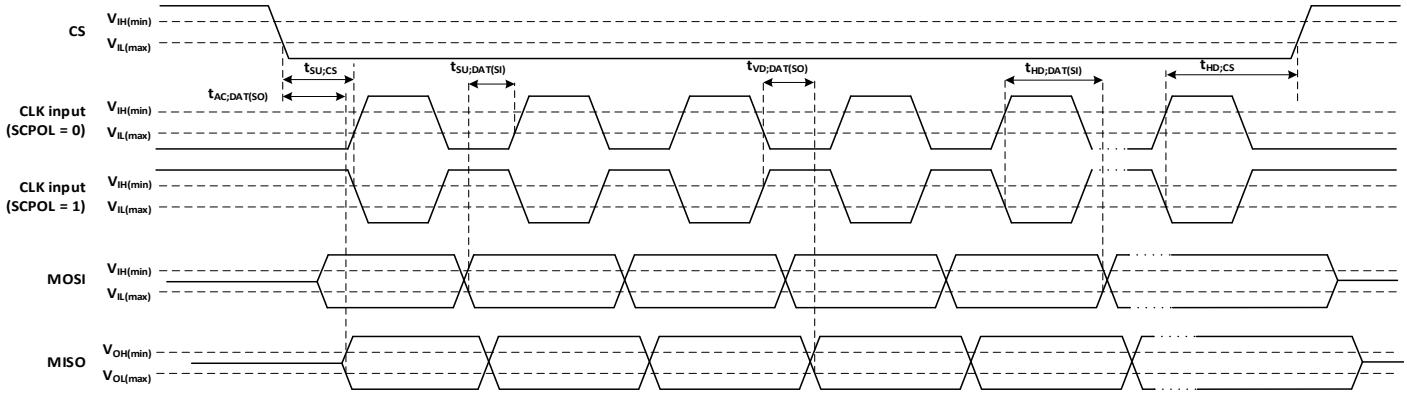


Figure 6-7 SPI timing diagram – slave (SCPH = 0)

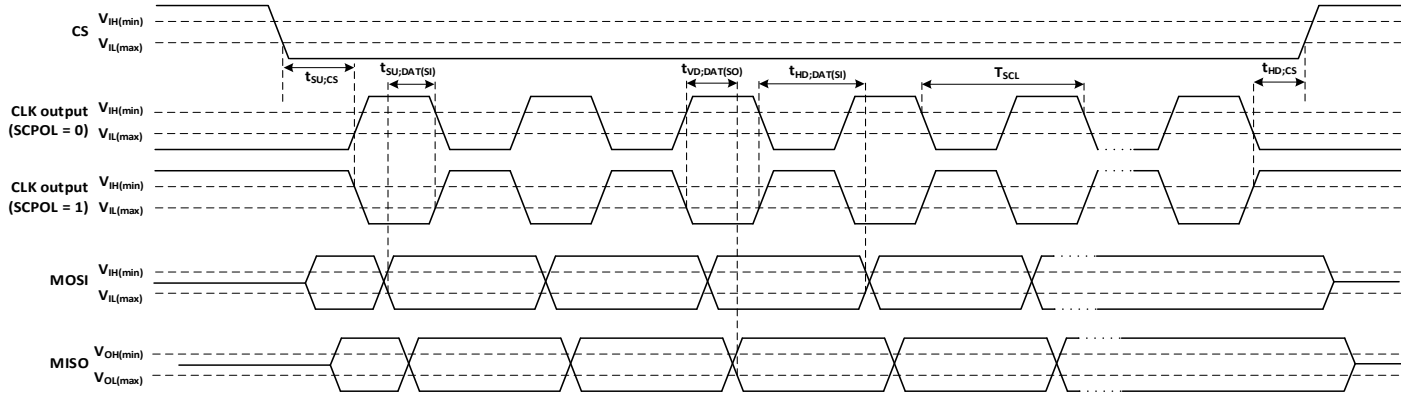


Figure 6-8 SPI timing diagram – slave (SCPH = 1)

6.11 I2S Characteristics

The Inter-IC Sound (I2S) supports both master and slave operations. All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.76V to 2.03V.
- The process includes all corners.
- Refer to section 6.6.2 for the definitions of $V_{OH(min)}$, $V_{OL(max)}$, $V_{IH(min)}$, and $V_{IL(max)}$.

Table 6-14 Timing data of I2S

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.85V I/O (1.76V~2.03V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	I2S clock	Master	41	1953	41	1953	ns
		Slave	41	1953	41	1953	ns
Duty	Clock duty	Master	45	55	45	55	%
		Slave	35	65	35	65	%
$t_{SU;DAT(I)}$	Input data setup time	Master	8	-	8	-	ns
$t_{SU;DAT(I)}$/$t_{SU;WS}$	Input data/WS setup time	Slave	3	-	3	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Master	0	-	0	-	ns
		Slave	3	-	3	-	ns
$t_{VD;DAT(O)}$	Output data valid time	Master	-5	5	-6	6	ns
$t_{VD;WS}$	Output WS valid time	Master	-5	5	-6	6	ns
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	14	-	19	ns

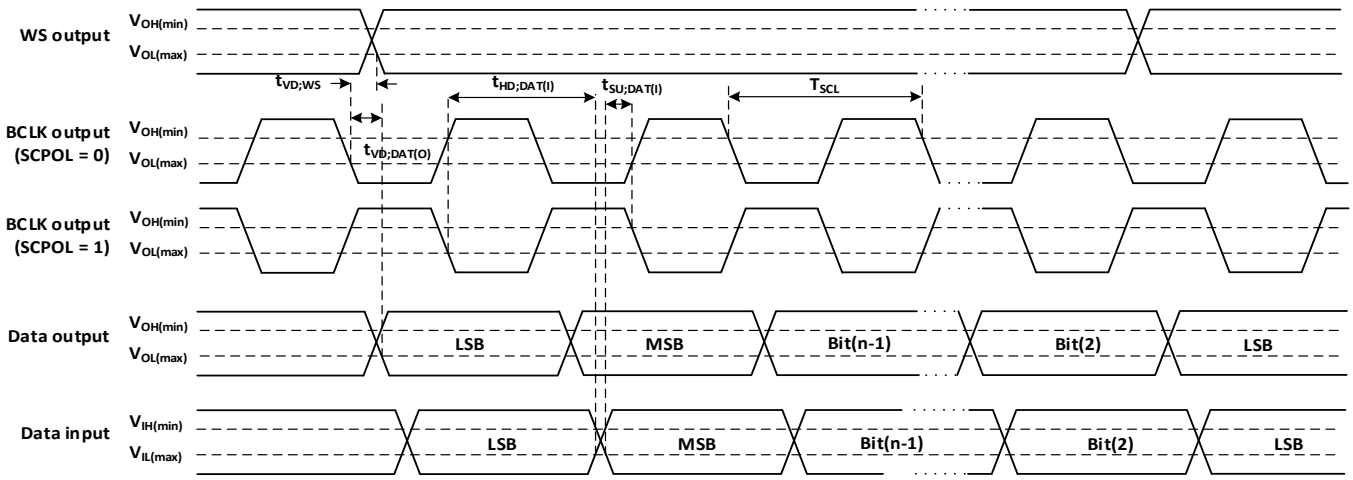


Figure 6-9 I2S timing diagram – master

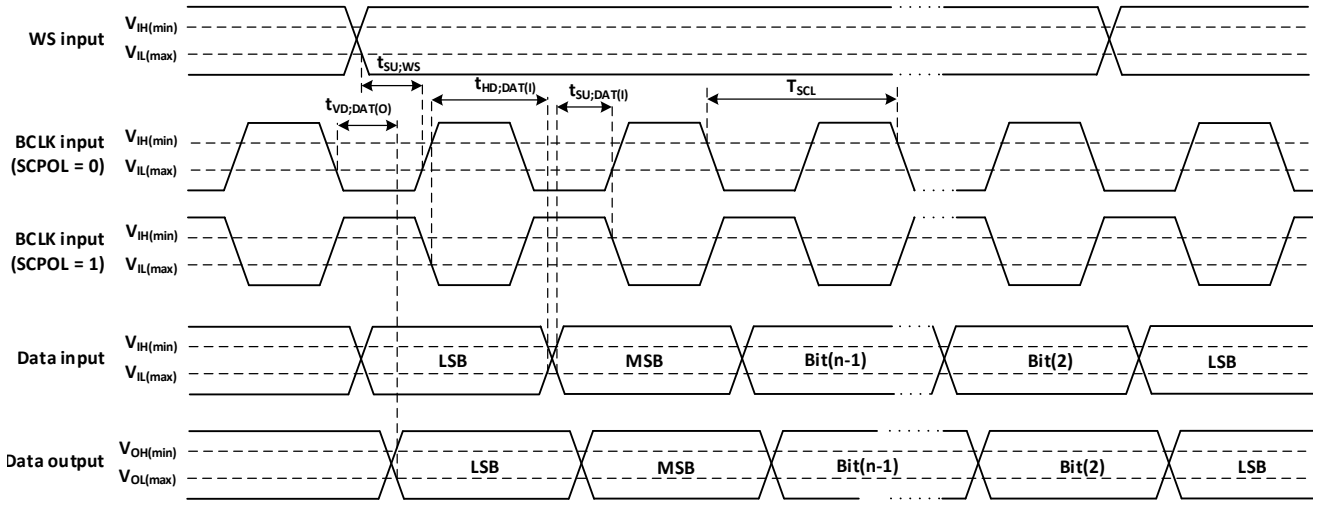


Figure 6-10 I2S timing diagram – slave

6.12 I2C Characteristics

The I2C timing data is suitable for both master and slave.

- The I/O operating voltage ranges from 2.97V to 3.63V or 1.76V to 2.03V
- The junction temperature of IC is between -40°C and 125°C.
- The process includes all corners.

6.12.1 Standard Mode & Fast Mode

Table 6-15 I2C-bus timing data (standard mode & fast mode)

Symbol	Parameter	Standard mode (Cb=400pF max.)		Fast mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	Programmable	100	Programmable	400	kHz
$t_{HD;STA}$	Hold time START condition	4	-	0.6	-	µs
t_{LOW}	LOW period of SCL clock	Programmable		Programmable		µs
t_{High}	HIGH period of SCL clock					
t_r	Rise time of both SDA and SCL signals	-	1000	-	300	ns

t_f	Fall time of both SDA and SCL signals	-	300	-	300	ns
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	us
$t_{SU;DAT}$	Data setup time	0.25	-	0.1	-	µs
$t_{SU;STO}$	Setup time for STOP condition	4	-	0.6	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs

NOTE

Cb is the bus load.

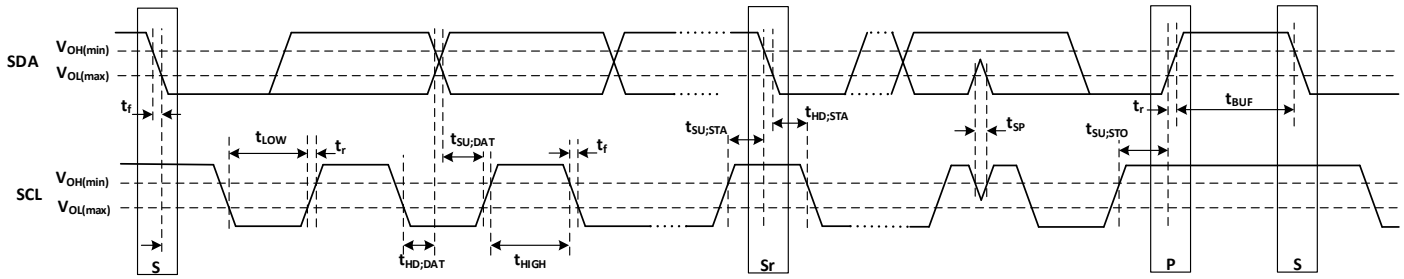


Figure 6-11 I2C-bus timing diagram (standard mode & fast mode)

6.12.2 High-Speed Mode

Table 6-16 I2C-bus timing data (high-speed mode)

Symbol	Parameter	High-Speed mode (Cb=100pF max.)		Unit
		Min.	Max.	
F_{SCL}	SCL clock frequency	Programmable	3.4	MHz
$t_{HD;STA}$	Hold time START condition	160	-	ns
$t_{SU;STA}$	Setup time for a repeated START condition	160	-	ns
$t_{HD;DAT}$	Data hold time	0	70	ns
$t_{SU;DAT}$	Data set-up time	10	-	ns
$t_{SU;STO}$	Setup time for STOP condition	160	-	ns
t_{high}	HIGH period of SCL clock	Programmable		ns
t_{low}	LOW period of SCL clock			ns
t_{rCL}	Rise time of SCLH signal	-	40	ns
t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	ns
t_{rDA}	Rise time of SDAH signal	10	80	ns
t_{fCL}	Fall time of SCLH signal	-	80	ns
t_{fDA}	Fall time of SDAH signal	-	80	ns

NOTE

Cb is the bus load.

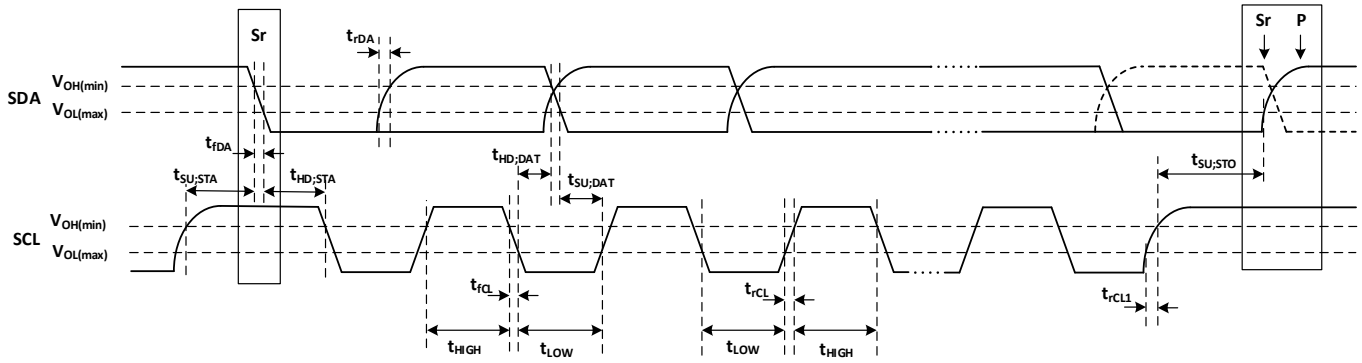


Figure 6-12 I2C-bus timing diagram (high-speed mode)

NOTE

In high-speed mode, the first rising edge of SCLH signal after a repeated start condition is push-pull output instead of open-drain output.

6.13 Timer Characteristics

Table 6-17 Timer characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{avg}	Average frequency of 32.768kHz clock source	VDD = 3.3V±10% (with calibration circuit on)	32767	32768	32769	Hz

6.14 QSPI Flash Controller Characteristics

This section describes the timing characteristics of the Quad Serial Peripheral Interface (QSPI) for Flash controller. All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.76V to 2.03V.
- The process includes all corners.
- Refer to section 6.6.2 for the definitions of $V_{OH(min)}$, $V_{OL(max)}$, $V_{IH(min)}$, and $V_{IL(max)}$.

Table 6-18 Timing data of QSPI Flash controller

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.85V I/O (1.76V~2.03V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	Clock period	Master	10	-	10	-	ns
t_{LOW}	Clock low time	Master	45%*T_{SCL}	55%*T_{SCL}	45%*T_{SCL}	55%*T_{SCL}	ns
t_{HIGH}	Clock high time	Master	45%*T_{SCL}	55%*T_{SCL}	45%*T_{SCL}	55%*T_{SCL}	ns
t_r	Data/Clock raise time	Master	-	1	-	1	ns
t_f	Data/Clock fall time	Master	-	1	-	1	ns
$t_{SU;DAT(I)}$	Data input setup time	Master	2	-	2	-	ns
$t_{HD;DAT(I)}$	Data input hold time	Master	1	-	1	-	ns
$t_{SU;DAT(O)}$	Data output setup time	Master	(T_{SCL}/2) − 2	-	(T_{SCL}/2) − 2	-	ns
$t_{HD;DAT(O)}$	Data output hold time	Master	(T_{SCL}/2) − 2	-	(T_{SCL}/2) − 2	-	ns
$t_{VD;DAT(O)}$	Data output valid time	Master	-2	2	-2	2	ns
$t_{SU;CS(A)}$	CS active setup time relative to CLK	Master	(T_{SCL}/2) − 2	-	(T_{SCL}/2) − 2	-	ns
$t_{HD;CS(A)}$	CS active hold time relative to CLK	Master	T_{SCL} − 2	-	T_{SCL} − 2	-	ns

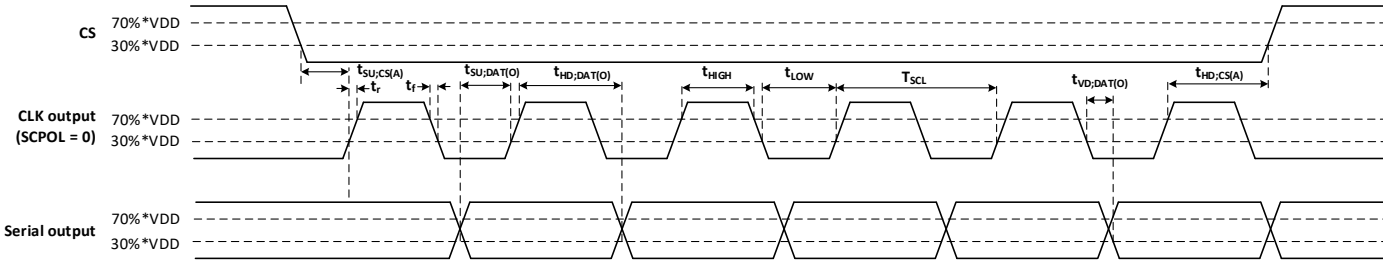


Figure 6-13 Output timing diagram (SCPH = 0)

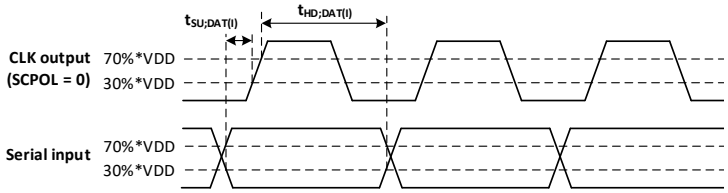


Figure 6-14 Input timing diagram (SCPH = 0)

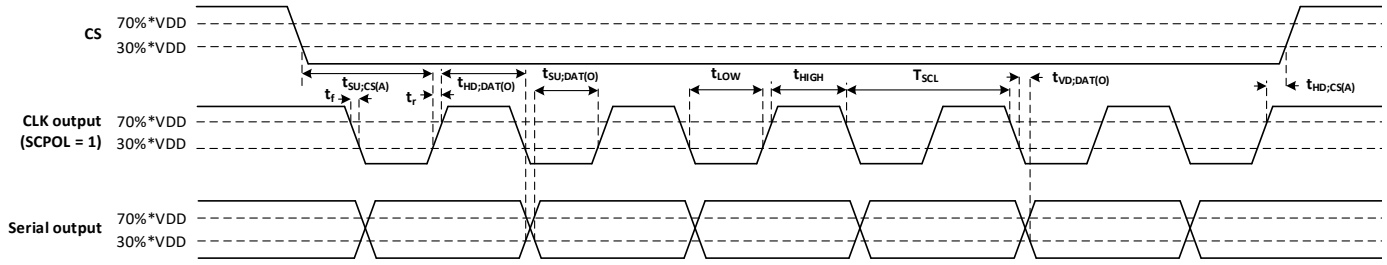


Figure 6-15 Output timing diagram (SCPH = 1)

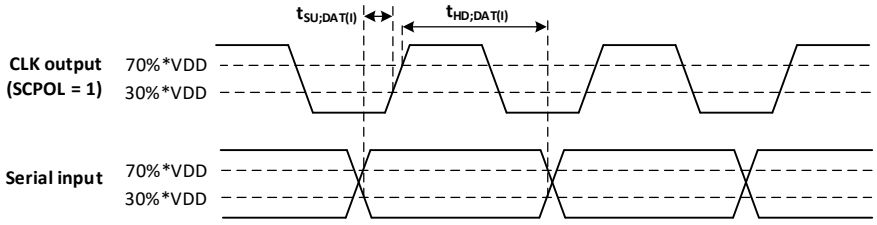


Figure 6-16 Input timing diagram (SCPH = 1)

6.15 Debug Interface Characteristics (SWD)

The debug interface of RTL872xD includes Arm standard bi-directional Serial Wire Debug (SWD). All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.76V to 2.03V.
- The process includes all corners.
- Refer to section 6.6.2 for the definitions of $V_{OH(min)}$, $V_{OL(max)}$, $V_{IH(min)}$, and $V_{IL(max)}$.

Table 6-19 Timing data of SWD

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.85V I/O (1.76V~2.03V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SWCLK clock period	Slave	50	-	50	-	ns
Duty cycle	Input clock duty cycle	Slave	30	70	30	70	%
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	15	-	19	ns
$t_{VD;DAT(I)}$	Input data setup time	Slave	2	-	2	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Slave	2	-	2	-	ns

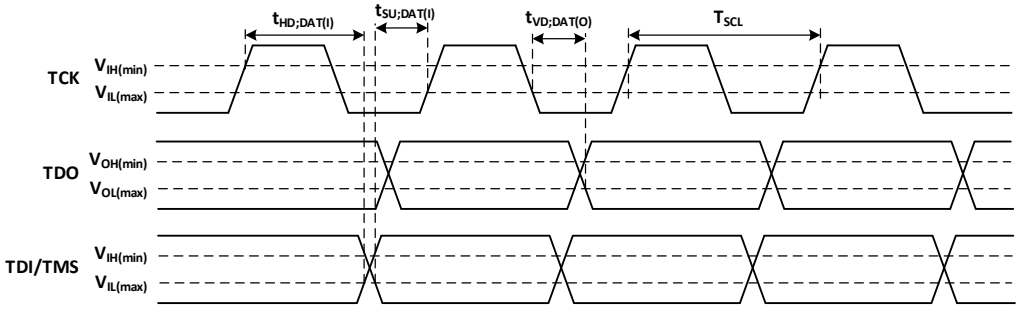


Figure 6-17 Timing diagram of SWD

6.16 UART Characteristics

All measurements are tested under the following conditions:

- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 3.0V to 3.6V or 1.76V to 2.035V.
- The process includes all corners.
- Refer to section 6.6.2 for the definitions of $V_{OH(min)}$, $V_{OL(max)}$, $V_{IH(min)}$, and $V_{IL(max)}$.

Table 6-20 Timing data of UART

Item	Conditions	Min.	Typ.	Max.	Unit
Transfer rate	TXD Clock Source: 40MHz XTAL			6000000	bps
	RXD Clock Source: 40MHz XTAL			6000000	bps
	RXD Clock Source: 2MHz OSC			115200	bps

NOTE

Total baud rate error shall be less than 3% in order to communicate correctly, which includes three parts: the error of real baud rate of Tx device and expected communication baud rate, the frequency drift of Rx IP clock, and the calculation baud error of Rx device. Users can enable the function of monitoring baud rate of Rx data to decrease the baud rate error.

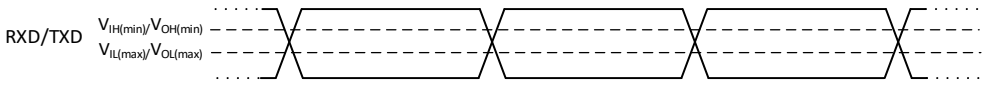


Figure 6-18 Timing diagram of UART

6.17 USB Characteristics

All measurements are tested under the following conditions:

- The junction temperature of IC is between -40°C and 125°C.
- The operating voltage ranges from 2.97V to 3.63V.
- The process includes all corners.

Table 6-21 Data rate of USB

Item	Conditions	Typ.	Unit
Transfer rate	High rate	480M	bps
	Full speed	12M	bps
	Low speed	1.5M	bps

The USB comply with the Universal Serial Bus (USB) v2.0 standard. All AC parameters related to these buffers can be found within the USB 2.0 electrical specifications. The following sections gives a brief overview of the electrical requirements on a USB interface. For extensive information, refer to the USB specification.

6.17.1 Signaling Level

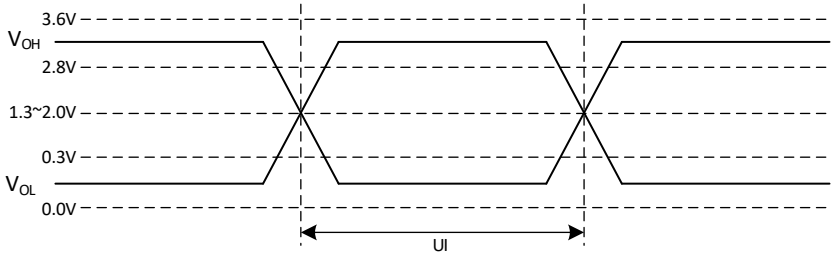


Figure 6-19 Signaling level of USB

Table 6-22 Signaling level of USB

Symbol	Parameter	Conditions	3.3V (2.97V~3.63V)		Unit
			Min.	Max.	
V_{OL}	Output low voltage	Low speed & full speed	0	0.3	V
		High speed	-10	10	mV
V_{OH}	Output high voltage	Low speed & full speed	2.8	3.6	V
		High speed	360	440	mV
UI	Bit period	Low speed & full speed	-	83	ns
		High speed	-	2.08	ns

6.17.2 Signal Rise and Fall Time

The rise and fall time is measured from 10%~90% of the signal low and high levels.

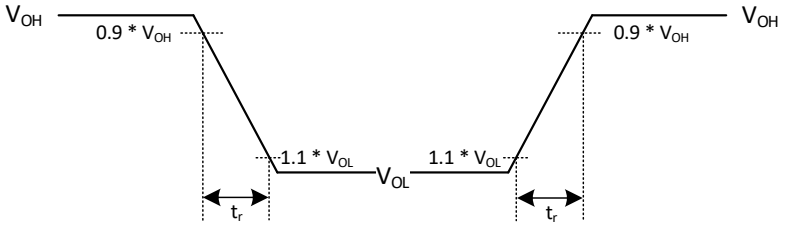


Figure 6-20 Signal rise and fall time of USB

Table 6-23 Signal rise and fall time of USB

Symbol	Parameter	Conditions	3.3V (2.97V~3.63V)		Unit
			Min.	Max.	
t_r	Rise/fall time (10%~90%)	Low speed	75	300	ns
		Full speed	4	20	ns
		High speed	500	-	ps

7 Package Specifications

7.1 Package Outline

7.1.1 QFN48

The QFN48 package specification of RTL872xD is shown in Figure 7-1 and Table 7-1.

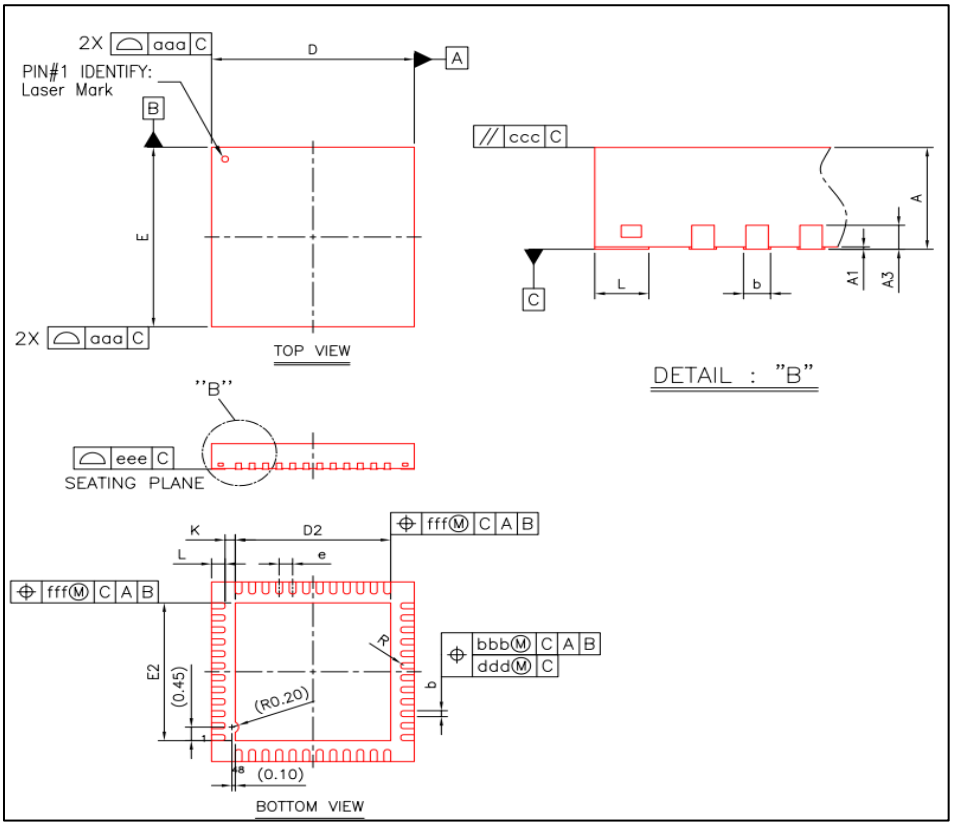


Figure 7-1 QFN48 package outline

Table 7-1 QFN48 package mechanical data

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.8	0.85	0.9	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20REF			0.008REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00BSC			0.236BSC		
E	6.00BSC			0.236BSC		
D2/E2	4.50	4.60	4.70	0.177	0.181	0.185
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		

bbb	0.07	0.003
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.08	0.003
fff	0.10	0.004

NOTE

- *Controlling dimension: millimeter (mm).*
- *Reference document: JEDEC MO-220.*

7.1.2 QFN68

The QFN68 package specification of RTL872xD is shown in Figure 7-2 and Table 7-2.

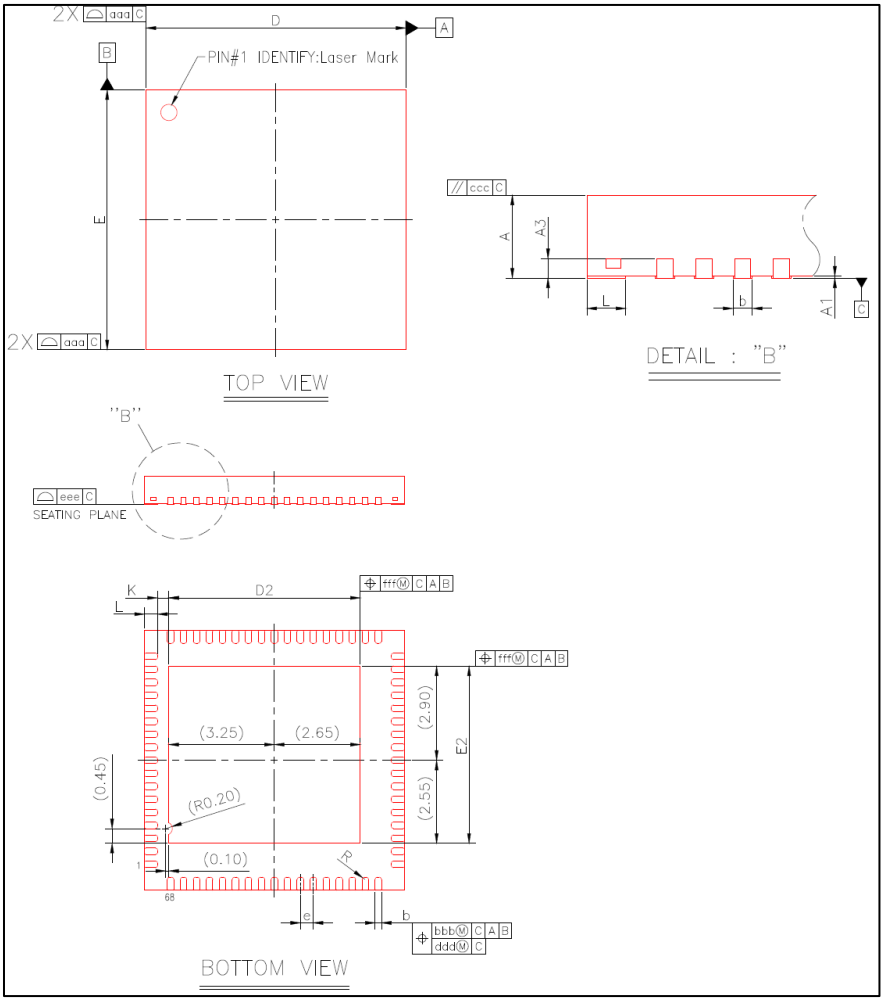


Figure 7-2 QFN68 package outline

Table 7-2 QFN68 package mechanical data

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.2 REF			0.008 REF		

b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D_2	5.80	5.90	6.00	0.205	0.209	0.213
E_2	5.35	5.45	5.55	0.217	0.220	0.224
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE

- *Controlling dimension: millimeter (mm).*
- *Reference document: JEDEC MO-220.*

7.1.3 QFN88

The QFN88 package specification of RTL872xD is shown in Figure 7-3 and Table 7-3.

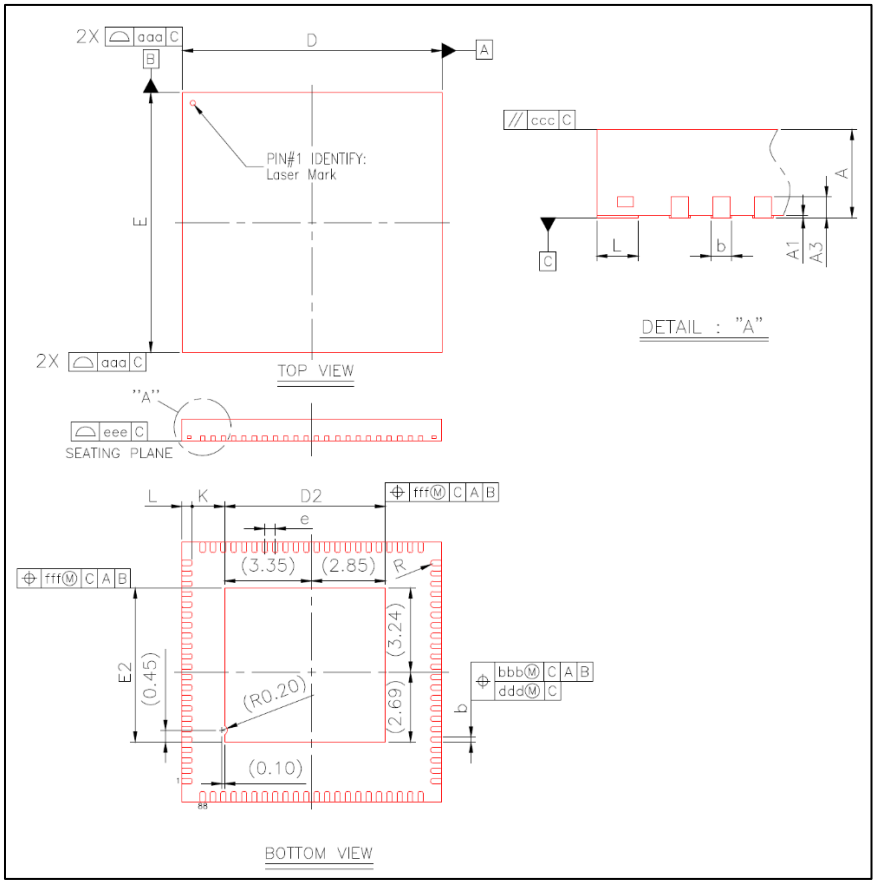


Figure 7-3 QFN88 package outline

Table 7-3 QFN88 package mechanical data

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D_2	6.10	6.20	6.30	0.240	0.244	0.248
E_2	5.83	5.93	6.03	0.230	0.233	0.237
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE

- *Controlling dimension: millimeter (mm).*
- *Reference document: JEDEC MO-220.*

7.2 Thermal Characteristics

Symbol	Parameter[1]	Package	Condition	Value[2][3]	Unit
θ_{JA}	Junction-to-ambient thermal resistance	QFN, 48-pin	2-layer PCB with no air flow	33.2	°C/W
			4-layer PCB with no air flow	27.1	
		QFN, 68-pin	2-layer PCB with no air flow	57.9	
		QFN, 88-pin	2-layer PCB with no air flow	26.1	
			4-layer PCB with no air flow	21.8	
θ_{JC}	Junction-to-case (top) thermal resistance	QFN, 48-pin	2-layer PCB with no air flow	10.5	°C/W
			4-layer PCB with no air flow	9.5	
		QFN, 68-pin	2-layer PCB with no air flow	11.9	
		QFN, 88-pin	2-layer PCB with no air flow	8.3	
			4-layer PCB with no air flow	7.5	
θ_{JB}	Junction-to-board thermal resistance	QFN, 48-pin	2-layer PCB with no air flow	8.5	°C/W
			4-layer PCB with no air flow	8.0	
		QFN, 68-pin	2-layer PCB with no air flow	16.1	
		QFN, 88-pin	2-layer PCB with no air flow	9.5	
			4-layer PCB with no air flow	8.5	
Ψ_{JT}	Junction-to-case (top) thermal characterization parameter	QFN, 48-pin	2-layer PCB with no air flow	0.23	°C/W
			4-layer PCB with no air flow	0.21	
		QFN, 68-pin	2-layer PCB with no air flow	0.9	
		QFN, 88-pin	2-layer PCB with no air flow	0.3	
			4-layer PCB with no air flow	0.3	
Ψ_{JB}	Junction-to-board thermal characterization parameter	QFN, 48-pin	2-layer PCB with no air flow	8.1	°C/W
			4-layer PCB with no air flow	7.6	
		QFN, 68-pin	2-layer PCB with no air flow	15.8	
		QFN, 88-pin	2-layer PCB with no air flow	9.2	
			4-layer PCB with no air flow	8.2	

NOTE

[1] Refer to EIA/JESD51-2, Integrated circuit Thermal Test Method Environment Conditions – Natural Convection (Still Air) for more information.

[2] These values are based on customized PCB systems, and will vary in function of board thermal characteristics and other components on the board.

[3] An ambient temperature of 85°C is assumed.

Revision History

Date	Version	Description
2025-09-03	4.8	Update Table 6-15 I2C-bus timing data (standard mode & fast mode)
2025-05-08	4.7	● Update Table 6-5 Recommended operation conditions ● Add Table 3-8 ADC pad status
2024-03-28	4.6	Delete the information of USI
2024-03-22	4.5	Update the pin name in Table 6-5 Recommended operation conditions
2023-12-22	4.4	● Add the section: Parameters Definitions ● Update Table 6-2 Specification of power consumption ● Update Table 6-5 Recommended operation conditions
2023-11-20	4.3	Add the information of RTL8722DM-VP1 (QFN88) to support LCDC 16-bit mode
2023-11-08	4.2	● Update the following sections: ■ Absolute Maximum Ratings ■ Power Consumption ■ Power Sequence ■ DC Characteristics ■ GPIO Characteristics ■ ADC Characteristics ■ SPI Characteristics ■ I2S Characteristics ■ I2C Characteristics ● Add the following sections: ■ QSPI Flash Controller Characteristics ■ Debug Interface Characteristics ■ UART Characteristics ■ Thermal Characteristics
2023-06-20	4.1	● Update Table 6-1 ● Add note to Table 6-5
2022-11-01	4.0	● Update Figure 1-1 ● Update the ADC counts in Table 1-9 ● Add notes to Table 6-6 and Table 6-7 ● Update BOR characteristic Table 6-11 ● Update LCDC parameters
2022-08-30	3.9	● Update the ordering information ● Update the following sections: ■ Power Consumption ■ Digital I/O Pin ■ GPIO Type ■ ADC Characteristics ● Add the following sections: ■ BOR Characteristics ■ SPI Characteristics ■ I2S Characteristics ■ I2C Characteristics ■ Timer Characteristics
2022-07-18	3.8	● Update the note of Table 2-3 ● Update Table 6-6 and Table 6-7
2022-03-03	3.7	Update Table 1-9: RTL8720DF supports SDIO host and device.
2022-01-12	3.6	Add the information of RTL8721DF (QFN68)
2021-12-02	3.5	Remove the function of VBAT_MEAS
2021-08-03	3.4	Update the section: Peripheral Counts of LCDC description
2021-06-23	3.3	Fix the max. Bluetooth Tx output power to 10dBm
2021-05-24	3.2	● Add the section: Thermal Characteristics ● Update the number of breakpoint and watchpoint for KM0 and KM4 in Table 1-1

2021-03-03	3.1	● Update Table 6-3 and add the table note ● Add the section: Power-down Sequence ● Update the pin assignment of RTL8720DF (QFN48)
2021-02-08	3.0	Update the ordering information
2021-01-20	2.9	Update the ordering information
2020-11-4	2.8	● Add the section: GPIO Type ● Add the information of RTL8720DF (QFN48)
2020-08-17	2.7	● Add the section: SAR ADC characteristics ● Update the ordering information
2020-06-24	2.6	● Update the ordering information ● Update the chapter: Memory Organization ● Update the RF receiver specification ● Update the figure: System architecture ● Update the feature of UART
2020-02-18	2.5	Update the feature of USB
2020-02-13	2.4	Add some description of PA[15] & PA[16] for QFN48
2020-01-13	2.3	Update the features
2019-12-25	2.2	● Update the temperature limit ● Update the part number and ordering information
2019-12-09	2.1	● Update the chapter: Memory Organization ● Update the section: General Description ● Update the specifications of Wi-Fi 2.4GHz/5GHz RF transmitter output power
2019-09-20	2.0	● Add the section: BT Radio Characteristics ● Update the value of Wi-Fi RF transmitter
2019-07-19	1.9	Update the section: Package Types
2019-06-03	1.8	● Update the description of Flash features ● Update the BLE Tx power to 8dbm
2019-04-10	1.7	● Add the chapter: Radio Characteristics ● Update the table: Timing specification of power sequence ● Add the note of interrupt priority ● Add the section: GPIO Pull Low Restriction ● Update the pin assignments for QFN88
2019-02-21	1.6	● Add the section: Power Sequence ● Re-organize the section: DC Characteristics
2019-01-25	1.5	● Modify the pin name (pin49) of QFN88 package ● Update the memory address
2018-12-26	1.4	Update the package specification of QFN68
2018-12-20	1.3	● Update the peripherals under different packages ● Revise the incorrect pin number
2018-12-17	1.2	Update the description of power pins
2018-12-13	1.1	● Re-organize the structure of document ● Update package types of RTL872xD and QFN68/QFN88 pin assignments ● Update the operating temperature limit
2018-10-18	1.0	Add the description about AUDIO_GND
2018-10-09	0.9	● Add description about SDIO device time consuming ● Unify and normalize the technical items and expression
2018-07-04	0.8	Add pin default configuration when boot
2018-07-04	0.7	Change audio & Secure
2018-07-04	0.6	Change system architecture
2018-07-03	0.5	Update system architecture
2018-06-29	0.4	Update power architecture
2018-06-28	0.3	Add Peripherals
2018-06-27	0.2	Add all features
2018-06-24	0.1	Initial version