DS0600
RTL8730E Datasheet

This document provides features and information on RTL8730E microcontroller.

Rev. 5.5

May, 2025

Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

DISCLAIMER

Please Read Carefully:
Realtek Semiconductor Corp., (Realtek) reserves the right to make corrections, enhancements, improvements and other changes to its products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

Reproduction of significant portions in Realtek data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Realtek is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions.

Buyers and others who are developing systems that incorporate Realtek products (collectively, "Customers") understand and agree that Customers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Customers have full and exclusive responsibility to assure the safety of Customers' applications and compliance of their applications (and of all Realtek products used in or for Customers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Customer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Customer agrees that prior to using or distributing any applications that include Realtek products, Customer will thoroughly test such applications and the functionality of such Realtek products as used in such applications.

Realtek's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation kits, (collectively, "Resources") are intended to assist designers who are developing applications that incorporate Realtek products; by downloading, accessing or using Realtek's Resources in any way, Customer (individually or, if Customer is acting on behalf of a company, Customer's company) agrees to use any particular Realtek Resources solely for this purpose and subject to the terms of this Notice.

Realtek's provision of Realtek Resources does not expand or otherwise alter Realtek's applicable published warranties or warranty disclaimers for Realtek's products, and no additional obligations or liabilities arise from Realtek providing such Realtek Resources. Realtek reserves the right to make corrections, enhancements, improvements and other changes to its Realtek Resources. Realtek has not conducted any testing other than that specifically described in the published documentation for a particular Realtek Resource.

Customer is authorized to use, copy and modify any individual Realtek Resource only in connection with the development of applications that include the Realtek product(s) identified in such Realtek Resource. No other license, express or implied, by estoppel or otherwise to any other Realtek intellectual property right, and no license to any technology or intellectual property right of Realtek or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Realtek products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of Realtek Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from Realtek under the patents or other Realtek's intellectual property.

Realtek's Resources are provided "as is" and with all faults. Realtek disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any epidemic failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights.

Realtek shall not be liable for and shall not defend or indemnify Customer against any claim, including but not limited to any infringement claim that related to or is based on any combination of products even if described in Realtek Resources or otherwise. In no event shall Realtek be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of Realtek's Resources or use thereof, and regardless of whether Realtek has been advised of the possibility of such damages. Realtek is not responsible for any failure to meet such industry standard requirements.

Where Realtek specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Customers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any Realtek products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death. Such equipment includes, without limitation, all medical devices identified by the U.S.FDA as Class III devices and equivalent classifications outside the U.S.

Customers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Customers' own risk. Customers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Customer will fully indemnify Realtek and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's

non-compliance with the terms and provisions of this Notice.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the engineer's reference and provides detailed development information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this document.

Contents

Conventions

The RTL8730E is new launched chip series on AmebaSmart family.

The following abbreviations apply to indicate the MCUs and platforms of RTL8730E of Realtek.

CA32	AP (Application Processor), dual-core Arm® Cortex®-A32 processor based on 32-bit Armv8-A architecture
Real-M300V (KM4)	NP (Network Processor), Arm Cortex-M55 compatible instruction set based on Armv8.1-M architecture
Real-M200 (KM0)	LP (Low-power Processor), Arm Cortex-M23 compatible instruction set based on Armv8-M baseline architecture
HP	A high-performance platform, consisting of CA32 & KM4 MCUs, high-speed RAM and high-speed peripherals, etc.
LS	A low-speed platform, consisting of KM0 MCU, low-speed RAM and low-speed peripherals, etc.

1 Product Overview

1.1 General Description

The RTL8730E is a highly integrated multi-core microcontroller based on dual-core Arm® Cortex®-A32 and KM4 (Arm® Cortex®-M55 32-bit compatible instruction set) RISC cores, with independently controlled isolated domains for maximum effectiveness and security. The microcontroller is designed for optimized power efficiency, RF performance, and ultra-low-power consumption. It encompasses all the characteristics of the low-power chip, including fine-grained clock gating, multiple power modes, and dynamic power scaling.

The Cortex-A32 (CA32), acting as application processor (AP), is the most power-efficient application processor capable of seamlessly supporting 32-bit code, running at a frequency of up to 1.2GHz. The CA32 processor employs an efficient, 8-stage, in-order pipeline that has been extensively optimized to provide 32-bit Armv8-A features within the smallest footprint and power. The built-in ARM's TrustZone secures the application codes from potential malicious attacks. It is an ideal choice for wearables, IoT (Internet of Things) devices, and embedded applications, especially those requiring a platform operating system.

The KM4 (also called Real-M300V), acting as network processor (NP), is a 3-staged pipelined 32-bit processor that bases on Armv8.1-M architecture supporting Cortex-M55 compatible instruction set, running at a frequency of up to 333MHz. It offers system enhancements such as low power consumption, enhanced debug features, single-precision floating-point unit (FPU), Digital Signal Processing (DSP) extension and M-profile Vector Extension (MVE) instructions, TrustZone-M security for hardware-enforced isolation, and a high level of support block integration.

The RTL8730E is a dual-band (2.4GHz and 5GHz) communication controller that integrates the specifications of Wi-Fi (Wi-Fi 6) and Bluetooth (Bluetooth 5.3). It supports 802.11 a/b/g/n/ac/ax wireless LAN (WLAN) network with 20MHz bandwidth. It consists of WLAN MAC, a 1T1R capable WLAN baseband, RF, Bluetooth and peripherals, delivering complete Wi-Fi and Bluetooth functionalities. It is designed with advanced features, enhanced RF performance, reduced audio transmission latency and system power consumption.

A variety of peripheral interfaces, including USB, serial ports, MIPI, LEDC, IR, ADC, etc., as well as sensor controllers (such as ADC, thermal) are integrated into RTL8730E seamlessly. Besides, the RTL8730E has rich audio features for smart audio applications with dedicated microphone interfaces (AMIC/DMIC), built-in voice activity detection (VAD), acoustic echo cancellation (AEC) reference ADC, stereo audio DAC, headphone out (HPO), and I2S. Abundant general-purpose I/O (GPIOs) can be configured to different functions according to different secure IoT applications flexibly, especially for intelligent voice interaction applications. The user-friendly development kits (SDK and HDK) are provided to customers for developing applications.

The RTL8730E also incorporates high-speed memories with on-chip SRAM and stacked selectable DRAM (either DDR or PSRAM). A dedicated SPI Flash controller provides a flexible and efficient way to access NOR/NAND Flash (e.g. byte and block access). A multi-layer AXI interconnect supports internal and external memory access.

1.2 Block Diagram

The functional block diagram is summarized in *Figure 1-1*. This diagram provides a view of the chip's major functional components and core complexes.

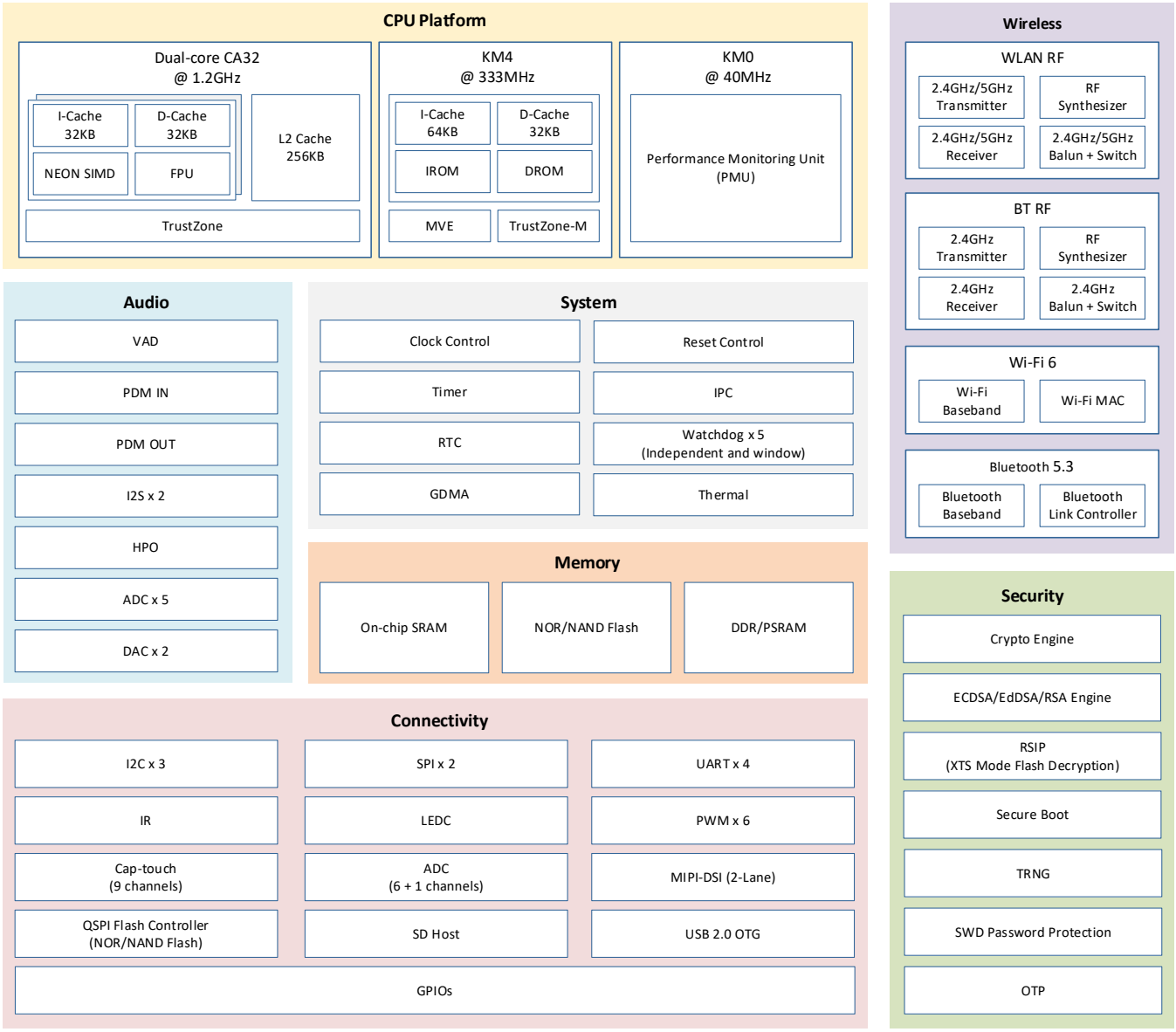


Figure 1-1 Block diagram

1.3 General Features

Parameter	Description
Number of Cores	4
CA32 Processor	● Dual-core Arm Cortex-A32: ■ L1 I-Cache: 32K bytes per core ■ L1 D-Cache: 32K bytes per core ■ L2 Cache: 256K bytes ● Running at a frequency of up to 1.2GHz per core ● Arm TrustZone security technology ● Integrated generic interrupt controller (GIC) with 256 shared peripheral interrupts ● Serial Wire Debug (SWD) with 6 instruction breakpoints and 4 data watchpoints
KM4 Processor	● Arm Cortex-M55 compatible instruction set ■ I-Cache: 64K bytes ■ D-Cache: 32K bytes ● Running at a frequency of up to 333MHz ● Memory Protection Unit (MPU) with up to 16 regions per security state ● Single-precision floating-point unit (FPU)

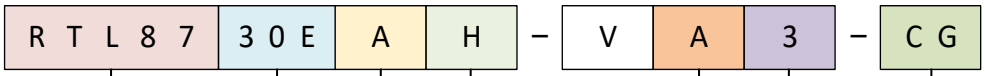
	● Digital Signal Processing (DSP) extension and M-profile Vector Extension (MVE) instructions ● Built-in Nested Vectored Interrupt Controller (NVIC) ● SWD with 8 instruction breakpoints and 1 data watchpoint
Memory	● Built-in PSARM/DDR (selectable) ● NAND Flash ● NOR Flash ● SD/eMMC card
WLAN	● 2.4GHz + 5GHz Wi-Fi 6 (802.11 a/b/g/n/ac/ax), 1x1 ● Integrated 2.4GHz/5GHz PA and LNA, and T/R switch ● Integrated 2.4GHz/5GHz balun ● Antenna diversity
Bluetooth	● Bluetooth 5.3 specification compliant, dual mode ■ Bluetooth Basic Rate/Enhanced Data Rate (BR/EDR) ■ Bluetooth Low Energy (BLE) ● Separated antenna for Bluetooth ● Supports scatter-net (concurrent central and peripheral mode) ● Supports SIG Mesh v1.0 and v1.1 ● AoA and AoD (both connection-oriented and connectionless) ● ISO (both CIS and BIS) ● BLE Connection Isochronous Channel
Audio	● Built-in a low-energy Voice Activity Detection (VAD) ● Up to128KB VAD buffer ● 5-channel Audio ADC, SNR > 98dB A-weighted and THD+N < -80dB ● Stereo audio DAC, SNR > 98dB A-weighted and THD+N < -85dB ● PDM interface function for external speaker AMP ● 8-channel digital microphone interface supported ● I2S x 2 ● Supports up to 8-channel I2S transmitter and receiver by TDM or PCM mode ● Up to 4 serial data outputs/inputs are transmitted within a sample period
Display	● 2-lane MIPI-DSI interface with D-PHY ● Max. bit rate: 1Gbps per lane
USB	USB 2.0 OTG controllers with integrated PHY
Serial Communication	● I2C x 3 ● UART x 4 ● SPI x 2 ● USB ● SD host
GPIO	Up to 61 GPIOs with configurable pull-up/pull-down resistors
Operating System	● Linux® OS ● FreeRTOS®
Package	● QFN100, 10mm x 10mm, 0.35mm pitch ● DR-QFN144, 11mm x 11mm, 0.5mm pitch

1.4 Target Applications

The integrated dual-core Arm© Cortex-A32 CPU and RISC low-power MCU can meet a wide range of customer AIoT application needs. Combined with abundant peripheral interfaces, the RTL8730E series has been successfully used in various products, such as:

- Smart speaker
- Central control panel
- Home theater
- Wireless gateway
- Smart kitchen appliance
- Industrial control panel
- …

1.5 Ordering Information



Prefix code
RTL87 = Realtek 32-bit microcontroller

Body code

Package code
A = QFN100
L = DR-QFN144

Memory type
F = Flash only
M = PSRAM/DDR only
H = Flash + PSRAM/DDR

Flash size
A = Same size as PSRAM or DDR
D = Double size of PSRAM or DDR
H = Half size of PSRAM or DDR
F = Four times size of PSRAM or DDR
Q = Quarter size of PSRAM or DDR

PSRAM/DDR size
3 = 8M bytes
4 = 16M bytes
5 = 32M bytes
6 = 64M bytes
7 = 128M bytes
8 = 256M bytes

IC packaging standard
CG = Compound green

Part number	Package	Flash (bytes)	PSRAM (bytes)	DDR (bytes)	CA32 (Max.)	Status
RTL8730EAH-VA3-CG	QFN100	8M (NOR)	8M	-	1.2GHz	
RTL8730EAH-VD3-CG	QFN100	16M (NOR)	8M	-	1.2GHz	
RTL8730EAH-VH6-CG	QFN100	32M (NOR)	-	64M (DDR2)	1.2GHz	
RTL8730EAM-VA6-CG	QFN100	-	-	64M (DDR2)	1.2GHz	
RTL8730ELH-VA3-CG	DR-QFN144	8M (NOR)	8M	-	1.2GHz	
RTL8730ELH-VA7-CG*	DR-QFN144	128M (NAND)	-	128M (DDR2)	1.32GHz	
RTL8730ELH-VA8-CG*	DR-QFN144	256M (NAND)	-	256M (DDR3L)	1.32GHz	
RTL8730ELM-VA7-CG	DR-QFN144	-	-	128M (DDR2)	1.2GHz	
RTL8730ELM-VA8-CG	DR-QFN144	-	-	256M (DDR3L)	1.2GHz	

NOTE

** No longer to kick off new projects with RTL8730ELH-VA7-CG or RTL8730ELH-VA8-CG after now.*

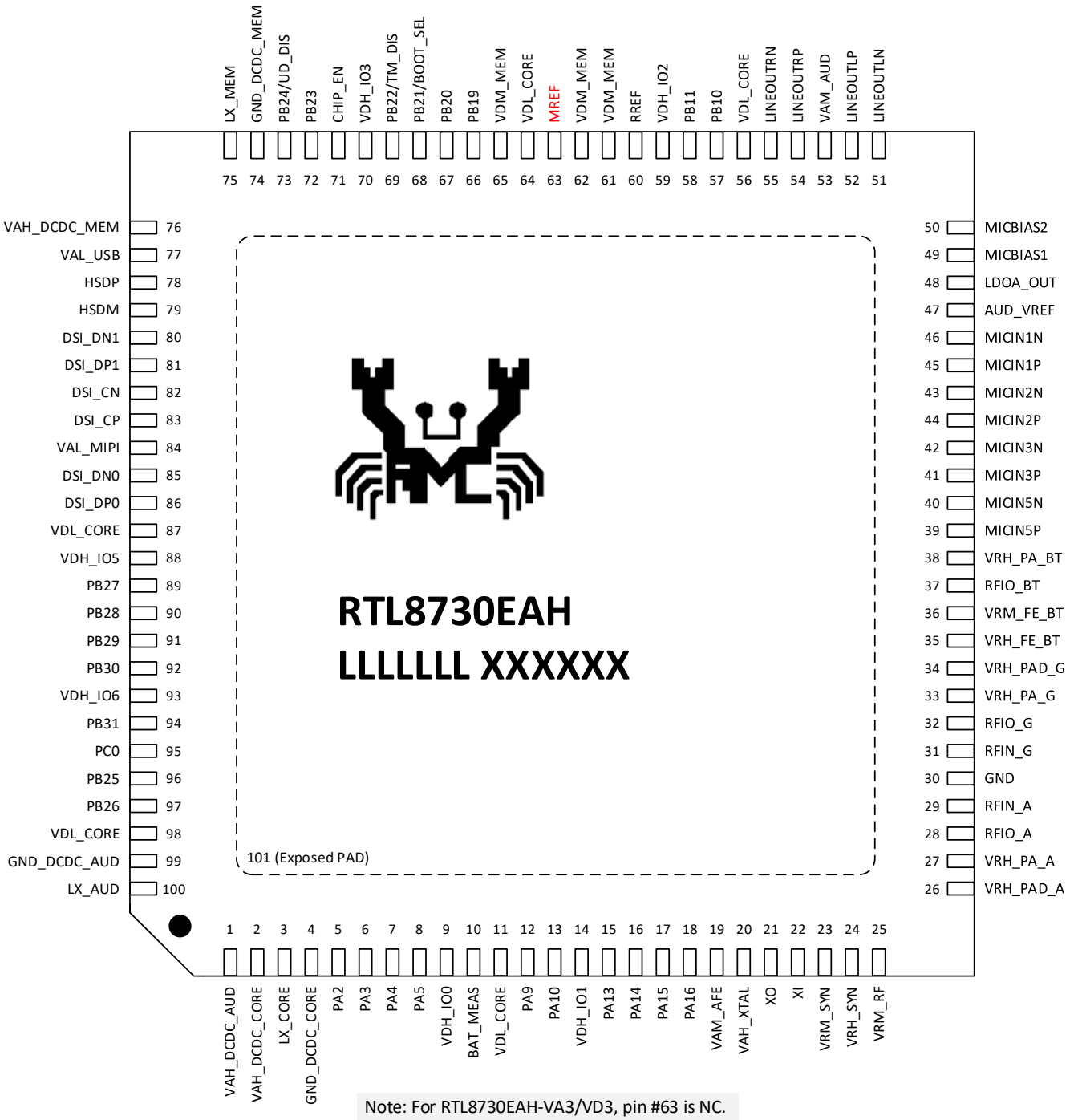
2 Pinout Information

2.1 Pin Assignments

2.1.1 QFN100

The RTL8730EAH series and RTL8730EAM series are packaged with quad flat no-leads (QFN) and 100-pin out.

2.1.1.1 RTL8730EAH



Note: For RTL8730EAH-VA3/VD3, pin #63 is NC.

Figure 2-1 Pin assignments of RTL8730EAH series

2.1.1.2 RTL8730EAM

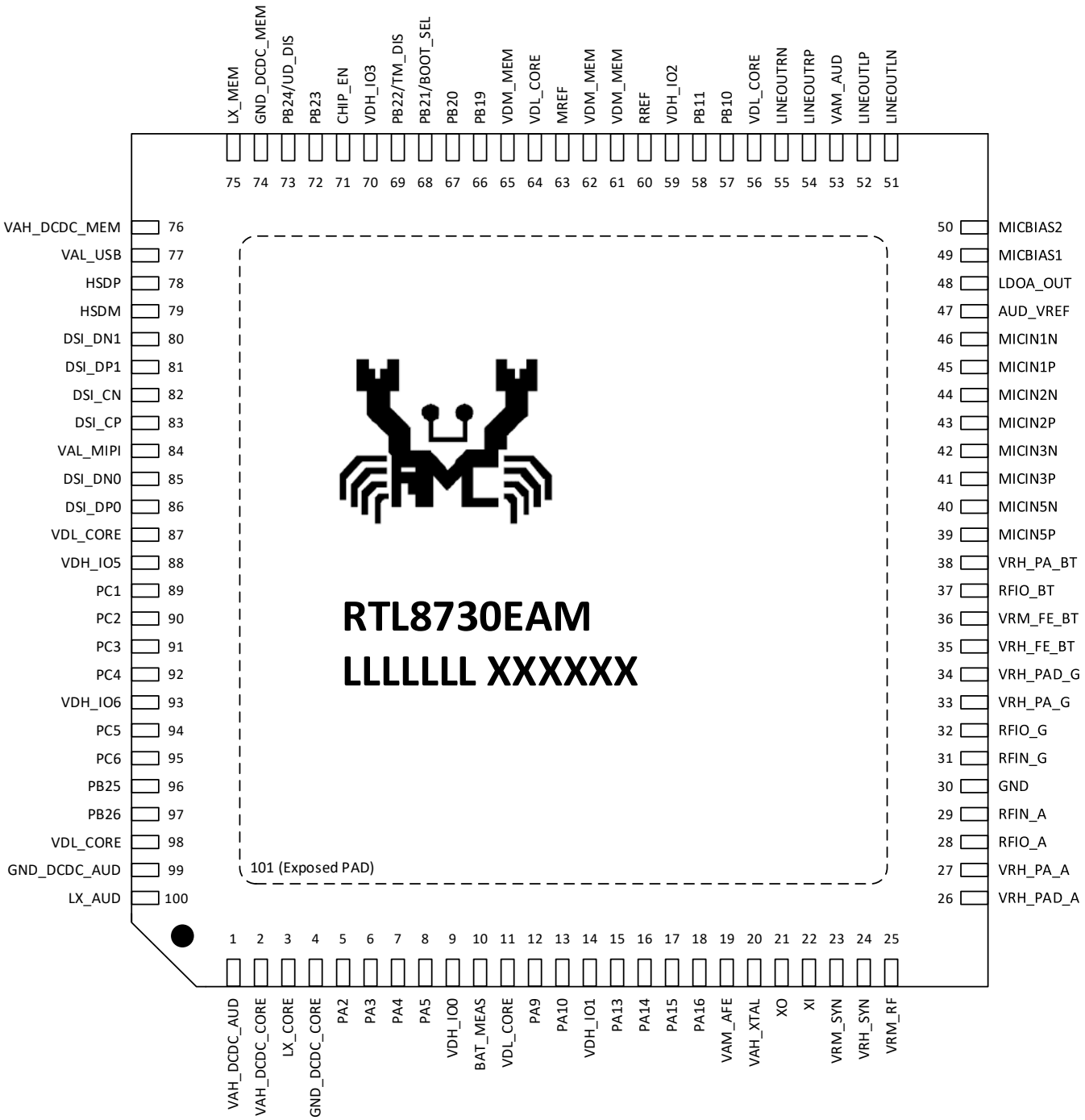
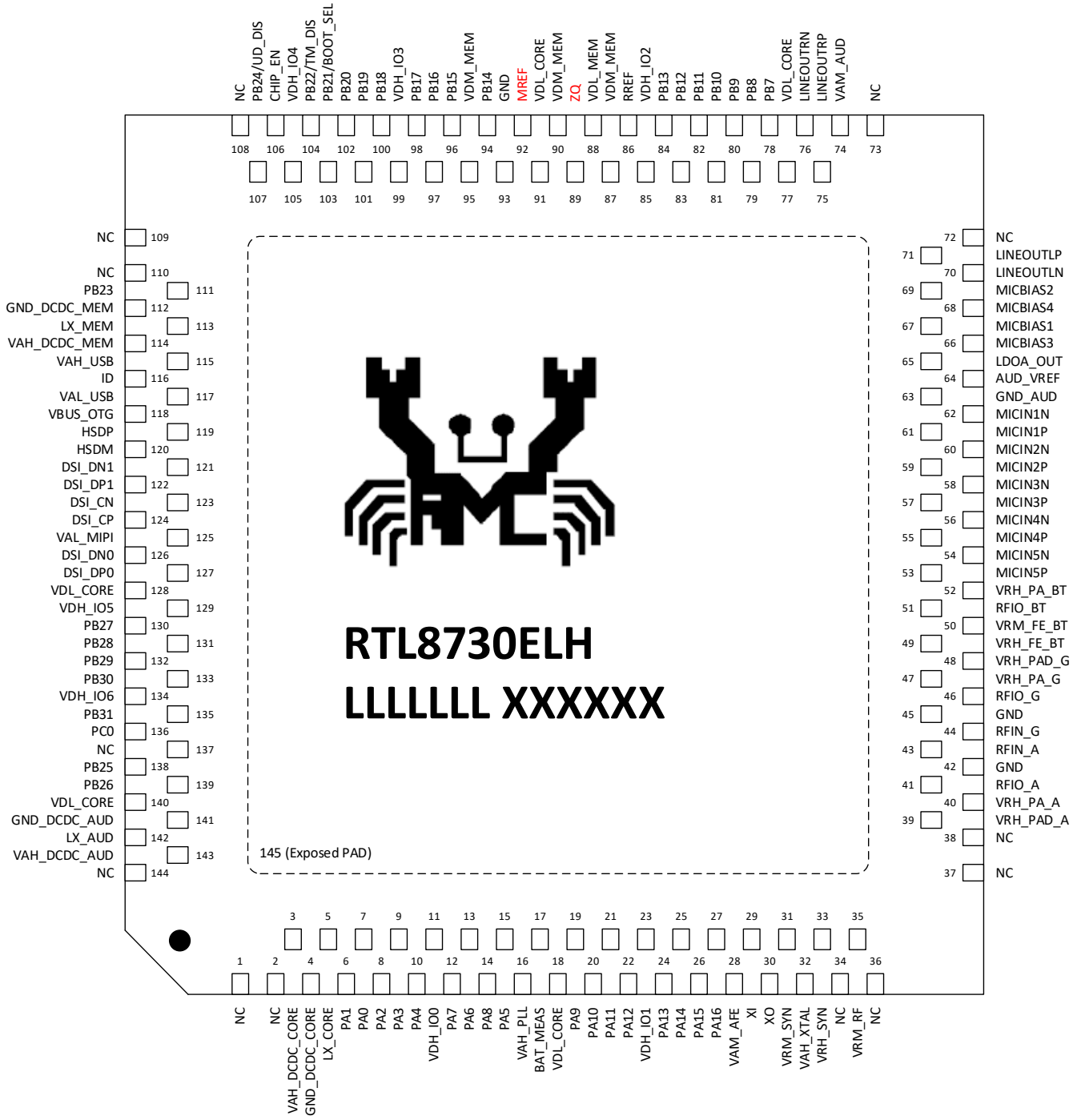


Figure 2-2 Pin assignments of RTL8730EAM series

2.1.2 DR-QFN144

The RTL8730ELH series and RTL8730ELM series are packaged with dual-row quad flat no-leads (DR-QFN) and 144-pin out.

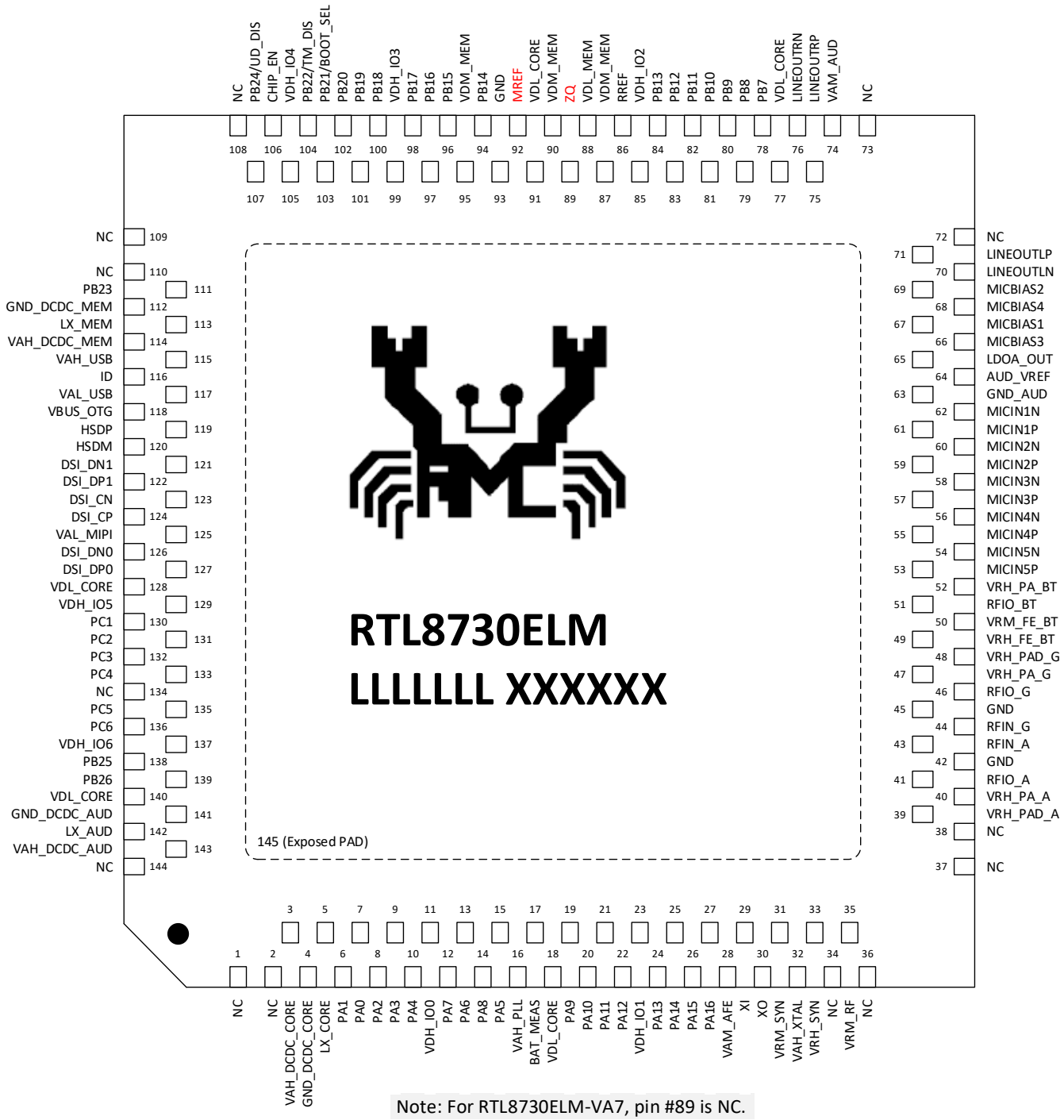
2.1.2.1 RTL8730ELH



Note:
· For other RTL8730ELH series, pin #89 is NC except RTL8730ELH-VA8.
· For RTL8730ELH-VA3, pin #92 is NC.

Figure 2-3 Pin assignments of RTL8730ELH series

2.1.2.2 RTL8730ELM



Note: For RTL8730ELM-VA7, pin #89 is NC.

Figure 2-4 Pin assignments of RTL8730ELM series

2.2 Pin Description

The definitions of pin type are listed below:

- I/O: Input/output pin
- A: Analog signal pin
- P: Power supply pin
- G: Ground pin
- RST: Reset pin

Pin number								Pin name	Pin type	Default function	Descriptions
RTL8730EAH-VD3	RTL8730EAH-VA3	RTL8730EAH-VH6	RTL8730EAM-VA6	RTL8730ELH-VA3	RTL8730ELH-VA7	RTL8730ELH-VA8	RTL8730ELM-VA7	RTL8730ELM-VA8			
1	1	1	1	143	143	143	143	143	VAH_DCDC_AUD	P	-	Power input for internal audio switching regulator
2	2	2	2	3	3	3	3	3	VAH_DCDC_CORE	P	-	Power input for internal digital core switching regulator
3	3	3	3	5	5	5	5	5	LX_CORE	P	-	Digital core switching regulator output
4	4	4	4	4	4	4	4	4	GND_DCDC_CORE	P	-	To be connected to ground
-	-	-	-	6	6	6	6	6	PA1	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	-	7	7	7	7	7	PA0	I/O	GPIO	
5	5	5	5	8	8	8	8	8	PA2	I/O	GPIO	
6	6	6	6	9	9	9	9	9	PA3	I/O	GPIO	
7	7	7	7	10	10	10	10	10	PA4	I/O	GPIO	
8	8	8	8	15	15	15	15	15	PA5	I/O	GPIO	
9	9	9	9	11	11	11	11	11	VDH_IO0	P	-	Power input for digital I/O power domain
-	-	-	-	12	12	12	12	12	PA7	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	-	13	13	13	13	13	PA6	I/O	GPIO	
-	-	-	-	14	14	14	14	14	PA8	I/O	GPIO	
-	-	-	-	16	16	16	16	16	VAH_PLL	P	-	Power input for AUX PLL circuit
10	10	10	10	17	17	17	17	17	BAT_MEAS	A	-	ADC input pin, 5V tolerance
11	11	11	11	18	18	18	18	18	VDL_CORE	P	-	Power input for digital core
12	12	12	12	19	19	19	19	19	PA9	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
13	13	13	13	20	20	20	20	20	PA10	I/O	GPIO	
-	-	-	-	21	21	21	21	21	PA11	I/O	GPIO	
-	-	-	-	22	22	22	22	22	PA12	I/O	GPIO	
14	14	14	14	23	23	23	23	23	VDH_IO1	P	-	Power input for digital I/O power domain
15	15	15	15	24	24	24	24	24	PA13	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
16	16	16	16	25	25	25	25	25	PA14	I/O	GPIO	
17	17	17	17	26	26	26	26	26	PA15	I/O	GPIO	
18	18	18	18	27	27	27	27	27	PA16	I/O	GPIO	
19	19	19	19	28	28	28	28	28	VAM_AFE	P	-	Power input for RF AFE circuit
20	20	20	20	32	32	32	32	32	VAH_XTAL	P	-	Power input for XTAL circuit
21	21	21	21	30	30	30	30	30	XO	A	-	Output of 40MHz crystal clock reference
22	22	22	22	29	29	29	29	29	XI	A	-	Input of 40MHz crystal clock reference
23	23	23	23	31	31	3	31	3	VRM_SYN	P	-	Power input for RF synthesizer circuit
24	24	24	24	33	33	33	33	33	VRH_SYN	P	-	Power input for RF synthesizer circuit
25	25	25	25	35	35	35	35	35	VRM_RF	P	-	Power input for RF circuit
26	26	26	26	39	39	39	39	39	VRH_PAD_A	P	-	Power input for RF 5G power amplifier driving circuit
27	27	27	27	40	40	40	40	40	VRH_PA_A	P	-	Power input for RF 5G power amplifier circuit
28	28	28	28	41	41	41	41	41	RFIO_A	A	-	WLAN 5GHz radio transmitter

											output and receiver input
29	29	29	43	43	43	43	43	RFIN_A	A	-	WLAN 5GHz RF AUX input signal
31	31	31	44	44	44	44	44	RFIN_G	A	-	WLAN 2.4GHz RF AUX input signal
32	32	32	46	46	46	46	46	RFIO_G	A	-	WLAN 2.4GHz & BT shared RF signal
33	33	33	47	47	47	47	47	VRH_PA_G	P	-	Power input for RF 2.4G power amplifier circuit
34	34	34	48	48	48	48	48	VRH_PAD_G	P	-	Power input for RF 2.4G power amplifier driving circuit
35	35	35	49	49	49	49	49	VRH_FE_BT	P	-	Power input for dedicated BT RF power
36	36	36	50	50	50	50	50	VRM_FE_BT	P	-	Power input for dedicated BT RF power
37	37	37	51	51	51	51	51	RFIO_BT	A	-	Bluetooth radio transmitter output and receiver input, dedicated for BT
38	38	38	52	52	52	52	52	VRH_PA_BT	P	-	Power input for Bluetooth
39	39	39	53	53	53	53	53	MICIN5P	A	Audio MICIN5P	The default function is audio MICIN5P, and it can be configured as other functions after IC boot.
40	40	40	54	54	54	54	54	MICIN5N	A	Audio MICIN5N	The default function is audio MICIN5N, and it can be configured as other functions after IC boot.
-	-	-	55	55	55	55	55	MICIN4P	A	Audio MICIN4P	The default function is audio MICIN4P, and it can be configured as other functions after IC boot.
-	-	-	56	56	56	56	56	MICIN4N	A	Audio MICIN4N	The default function is audio MICIN4N, and it can be configured as other functions after IC boot.
41	41	41	57	57	57	57	57	MICIN3P	A	Audio MICIN3P	The default function is audio MICIN3P, and it can be configured as other functions after IC boot.
42	42	42	58	58	58	58	58	MICIN3N	A	Audio MICIN3N	The default function is audio MICIN3N, and it can be configured as other functions after IC boot.
43	43	43	59	59	59	59	59	MICIN2P	A	Audio MICIN2P	The default function is audio MICIN2P, and it can be configured as other functions after IC boot.
44	44	44	60	60	60	60	60	MICIN2N	A	Audio MICIN2N	The default function is audio MICIN2N, and it can be configured as other functions after IC boot.
45	45	45	61	61	61	61	61	MICIN1P	A	Audio MICIN1P	The default function is audio MICIN1P, and it can be configured as other functions after IC boot.
46	46	46	62	62	62	62	62	MICIN1N	A	Audio MICIN1P	The default function is audio MICIN5P, and it can be configured as other functions after IC boot.
-	-	-	63	63	63	63	63	GND_AUD	G	-	To be connected to ground
47	47	47	64	64	64	64	64	AUD_VREF	P	-	Reference voltage output decoupling point (typical 0.5*LDOA_OUT)
48	48	48	65	65	65	65	65	LDOA_OUT	P	-	Audio reference voltage
-	-	-	66	66	66	66	66	MICBIAS3	A	Audio MICBIAS3	The default function is audio MICBIAS3, and it can be configured as other functions after IC boot.
49	49	49	67	67	67	67	67	MICBIAS1	A	Audio MICBIAS1	The default function is audio MICBIAS1, and it can be

											configured as other functions after IC boot.
-	-	-	68	68	68	68	68	MICBIAS4	A	Audio MICBIAS4	The default function is audio MICBIAS4, and it can be configured as other functions after IC boot.
50	50	50	69	69	69	69	69	MICBIAS2	A	Audio MICBIAS2	The default function is audio MICBIAS2, and it can be configured as other functions after IC boot.
51	51	51	70	70	70	70	70	LINEOUTLN	A	Audio LINEOUTLN	The default function is audio LINEOUTLN function, and it can be configured as other functions after IC boot.
52	52	52	71	71	71	71	71	LINEOUTLP	A	Audio LINEOUTLP	The default function is audio LINEOUTLP function, and it can be configured as other functions after IC boot.
53	53	53	74	74	74	74	74	VAM_AUD	P	-	Power input for audio codec
54	54	54	75	75	75	75	75	LINEOUTRP	A	Audio LINEOUTRN	The default function is audio LINEOUTRN function, and it can be configured as other functions after IC boot.
55	55	55	76	76	76	76	76	LINEOUTRN	A	Audio LINEOUTRP	The default function is audio LINEOUTRP function, and it can be configured as other functions after IC boot.
56	56	56	77	77	77	77	77	VDL_CORE	P	-	Power input for digital core
-	-	-	78	78	78	78	78	PB7	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	79	79	79	79	79	PB8	I/O	GPIO	
-	-	-	80	80	80	80	80	PB9	I/O	GPIO	
57	57	57	81	81	81	81	81	PB10	I/O	GPIO	
58	58	58	82	82	82	82	82	PB11	I/O	GPIO	
-	-	-	83	83	83	83	83	PB12	I/O	GPIO	
-	-	-	84	84	84	84	84	PB13	I/O	GPIO	
59	59	59	85	85	85	85	85	VDH_IO2	P	-	Power input for digital I/O power domain
60	60	60	86	86	86	86	86	RREF	A	-	External reference resistor 12kΩ for internal current source, 1% accuracy
61, 62, 65			87, 90, 95			87, 90, 95		VDM_MEM	P	-	Power input for memory controller
-	-	-	88	88	88	88	88	VDL_MEM	P	-	Power input for memory controller
-	-	-	-	-	89	-	89	ZQ	A	-	External reference resistor 240Ω for internal ZQ calibration, 1% accuracy
-	63	63	-	92	92	92	92	MREF	A	-	Optional reference voltage for memory
64	64	64	91	91	91	91	91	VDL_CORE	P	-	Power input for digital core
-	-	-	94	94	94	94	94	PB14	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
-	-	-	96	96	96	96	96	PB15	I/O	GPIO	
-	-	-	97	97	97	97	97	PB16	I/O	GPIO	
-	-	-	98	98	98	98	98	PB17	I/O	GPIO	
-	-	-	100	100	100	100	100	PB18	I/O	GPIO	
66	66	66	101	101	101	101	101	PB19	I/O	GPIO	
67	67	67	102	102	102	102	102	PB20	I/O	GPIO	
68	68	68	103	103	103	103	103	PB21/BOOT_SEL	I/O	GPIO	Wakeup pin, also the external Flash type trap pin. ● 1: NOR Flash ● 0: NAND Flash The default function is general-purpose input/output, and it can be configured as other functions.
69	69	69	104	104	104	104	104	PB22/TM_DIS	I/O	GPIO	Wakeup pin. The IC operating mode is determined by the level of trap pin PB22/TM_DIS during the

											process of power on. ● 1: Normal mode ● 0: Test mode The default function is general-purpose input/output, and it can be configured as other functions.
70	70	70	99	99	99	99	99	VDH_IO3	P	-	Power input for digital I/O power domain
-	-	-	105	105	105	105	105	VDH_IO4	P	-	Power input for digital I/O power domain
71	71	71	106	106	106	106	106	CHIP_EN	RST	-	Chip enable. ● 1: Enable chip ● 0: Shut down chip
72	72	72	111	111	111	111	111	PB23	I/O	LOGUART Rx	Wakeup pin. The default function is LOGUART Rx, and it can be configured as other functions after IC boot. If it is configured as a GPIO function, the LOGUART function becomes invalid.
73	73	73	107	107	107	107	107	PB24/UD_DIS	I/O	LOGUART Tx	Wakeup pin. The default function is LOGUART Tx, and it can be configured as other functions after IC boot. UART download disable, default internal pull up. ● 1: Enter into normal boot mode ● 0: Enter into UART download mode If it is configured as a GPIO function, the LOGUART function becomes invalid.
74	74	74	112	112	112	112	112	GND_DCDC_MEM	G	-	To be connected to ground
75	75	75	113	113	113	113	113	LX_MEM	P	-	Memory switching regulator output
76	76	76	114	114	114	114	114	VAH_DCDC_MEM	P	-	Power input for internal memory switching regulator
-	-	-	115	115	115	115	115	VAH_USB	P	-	Power input for USB analog
-	-	-	116	116	116	116	116	ID	A	-	This pin can be connected to the ID of the micro-USB or mini-USB interface. An USB OTG device can operate as either a host or a peripheral. The value of ID determines the initial roles, as input. ● 0: A-Device, initial host ● 1: B-Device, initial peripheral This pin can be floating when the USB OTG mode is disabled.
77	77	77	117	117	117	117	117	VAL_USB	P	-	Power input for USB analog
-	-	-	118	118	118	118	118	VBUS_OTG	P	-	This pin acts as an input, 5V tolerant. It is used to detect the VBUS voltage level. This pin can be floating when the USB OTG mode is disabled.
78	78	78	119	119	119	119	119	HSDP	I/O	-	USB positive differential signal
79	79	79	120	120	120	120	120	HSDM	I/O	-	USB negative differential signal
80	80	80	121	121	121	121	121	DSI_DN1	I/O	MIPI	MIPI DSI Data lane 1 differential negative signal, only supports HS Tx.
81	81	81	122	122	122	122	122	DSI_DP1	I/O	MIPI	MIPI DSI Data lane 1 differential positive signal, only supports HS Tx.
82	82	82	123	123	123	123	123	DSI_CN	I/O	MIPI	MIPI DSI Clock lane differential negative signal, supports HS Tx and LS Tx.
83	83	83	124	124	124	124	124	DSI_CP	I/O	MIPI	MIPI DSI Clock lane differential

											positive signal, supports HS Tx and LS Tx.
84	84	84	125	125	125	125	125	VAL_MIPI	P	-	Power input for MIPI
85	85	85	126	126	126	126	126	DSI_DN0	I/O	MIPI	MIPI DSI Data lane 0 differential negative signal, supports HS Tx, LS Tx, and LS Rx.
86	86	86	127	127	127	127	127	DSI_DP0	I/O	MIPI	MIPI DSI Data lane 0 differential positive signal, supports HS Tx, LS Tx, and LS Rx.
87	87	87	128	128	128	128	128	VDL_CORE	P	-	Power input for digital core
88	88	88	129	129	129	129	129	VDH_IO5	P	-	Power input for digital I/O power domain
89	89	-	130	130	130	-	-	PB27	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
90	90	-	131	131	131	-	-	PB28	I/O	GPIO	
91	91	-	132	132	132	-	-	PB29	I/O	GPIO	
92	92	-	133	133	133	-	-	PB30	I/O	GPIO	
-	-	89	-	-	-	130	130	PC1	I/O	GPIO	
-	-	90	-	-	-	131	131	PC2	I/O	GPIO	
-	-	91	-	-	-	132	132	PC3	I/O	GPIO	
-	-	92	-	-	-	133	133	PC4	I/O	GPIO	
-	-	94	-	-	-	135	135	PC5	I/O	GPIO	
-	-	95	-	-	-	136	136	PC6	I/O	GPIO	
93	93	93	134	134	134	137	137	VDH_IO6	P	-	Power input for digital I/O power domain
94	94	-	135	135	135	-	-	PB31	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
95	95	-	136	136	136	-	-	PC0	I/O	GPIO	
96	96	96	138	138	138	138	138	PB25	I/O	GPIO	
97	97	97	139	139	139	139	139	PB26	I/O	GPIO	
98	98	98	140	140	140	140	140	VDL_CORE	P	-	Power input for digital core
99	99	99	141	141	141	141	141	GND_DCDC_AUD	G	-	To be connected to ground
100	100	100	142	142	142	142	142	LX_AUD	P	-	Audio switching regulator output
30	30	30	45, 93			45, 93		GND	G	-	To be connected to ground
63	-	-	1 2 34 36 37 38 42 72 73 89 92 108 109 110 137 144	1 2 34 36 37 38 42 72 73 89 108 109 110 137 144	1 2 34 36 37 38 42 72 73 108 109 110 137 144	1 2 34 36 37 38 42 72 73 89 108 109 110 134 144	1 2 34 36 37 38 42 72 73 108 109 110 134 144	NC	-	-	No connection

2.3 Power Supply for Pins

Several GPIO pins belong to a specific power supply group. Each power pin may be supplied at different voltage levels as needed by the application, and can be powered by typical 1.8V or 3.3V according to different packages.

Refer to *UM0602_RTL8730E_pin_mux.xls* for more details on power supply pins.

3 Functional Description

3.1 Power Management

3.1.1 Power Structure

Only an external typical 3.3V power supply is required for the RTL8730E; all the other required voltages can be converted and output by embedded three DC-DC switching regulators. The recommended power on off sequence can be found in Section *4.4*.

The power structure diagrams are summarized in *Figure 3-1* and *Figure 3-2*.

- *Figure 3-1* applies for all series of RTL8730E.
  - The DCDC_CORE outputs typical 0.8V, 0.9V or 1.0V for low voltage circuits including digital system, USB and memory controller, etc., and 0.8V, 0.9V or 1.0V is controlled by the software based on application requirements.
  - The DCDC_MEM outputs typical 1.35V or 1.8V for embedded memory including PSRAM or DDR, and 1.35V or 1.8V is controlled by the software based on the type of embedded memory.
  - The DCDC_AUD outputs typical 1.8V for audio and radio frequency (RF) circuits.
- *Figure 3-2* only applies for RTL8730ELH-VA3 and RTL8730EAH-VA3/VD3.
  - The PSRAM, audio and RF circuits are powered by DCDC_MEM and the typical output voltage for DCDC_MEM is 1.8V.
  - The DCDC_AUD is not used and the related circuit components are not needed.

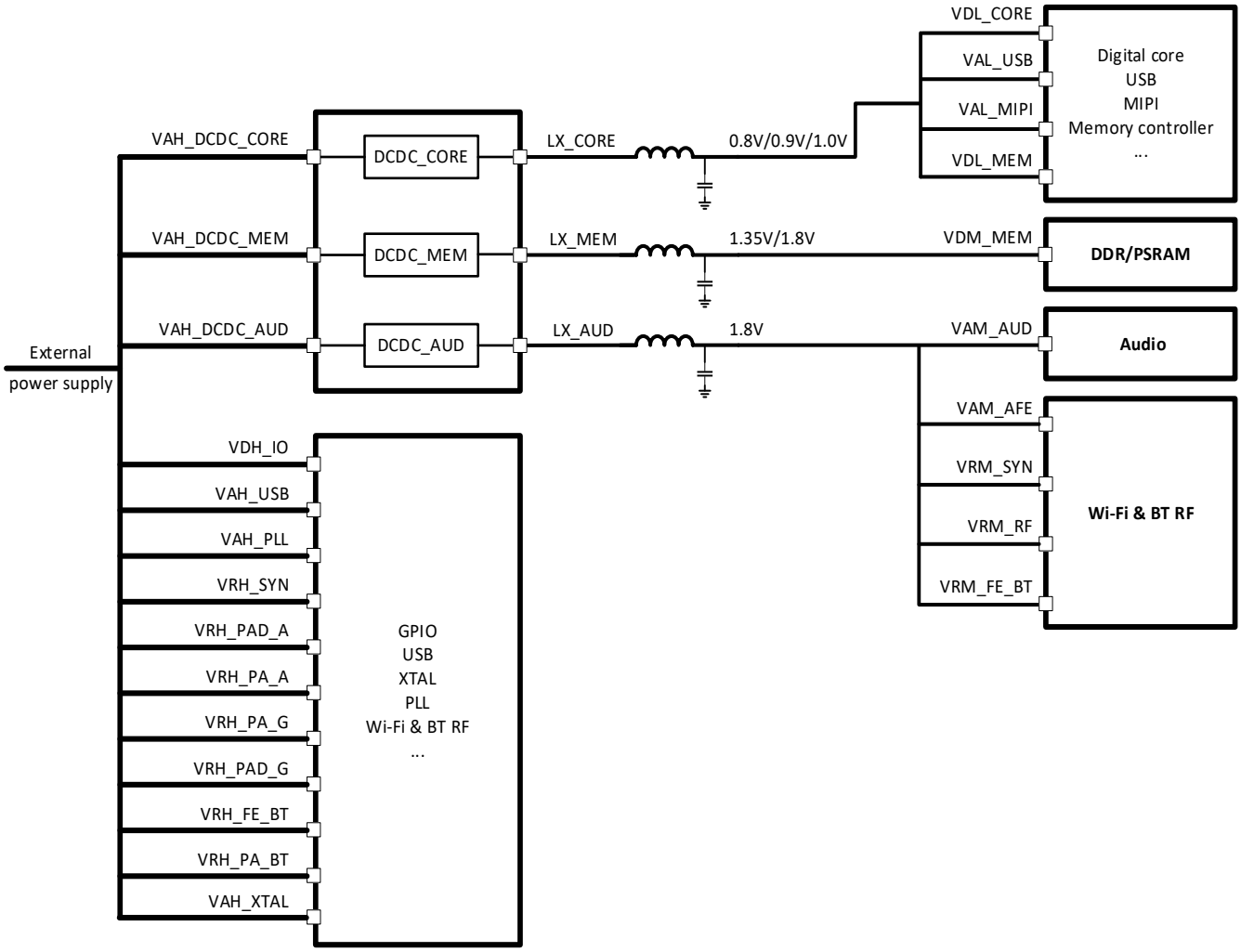


Figure 3-1 Power block diagram for all series of RTL8730E

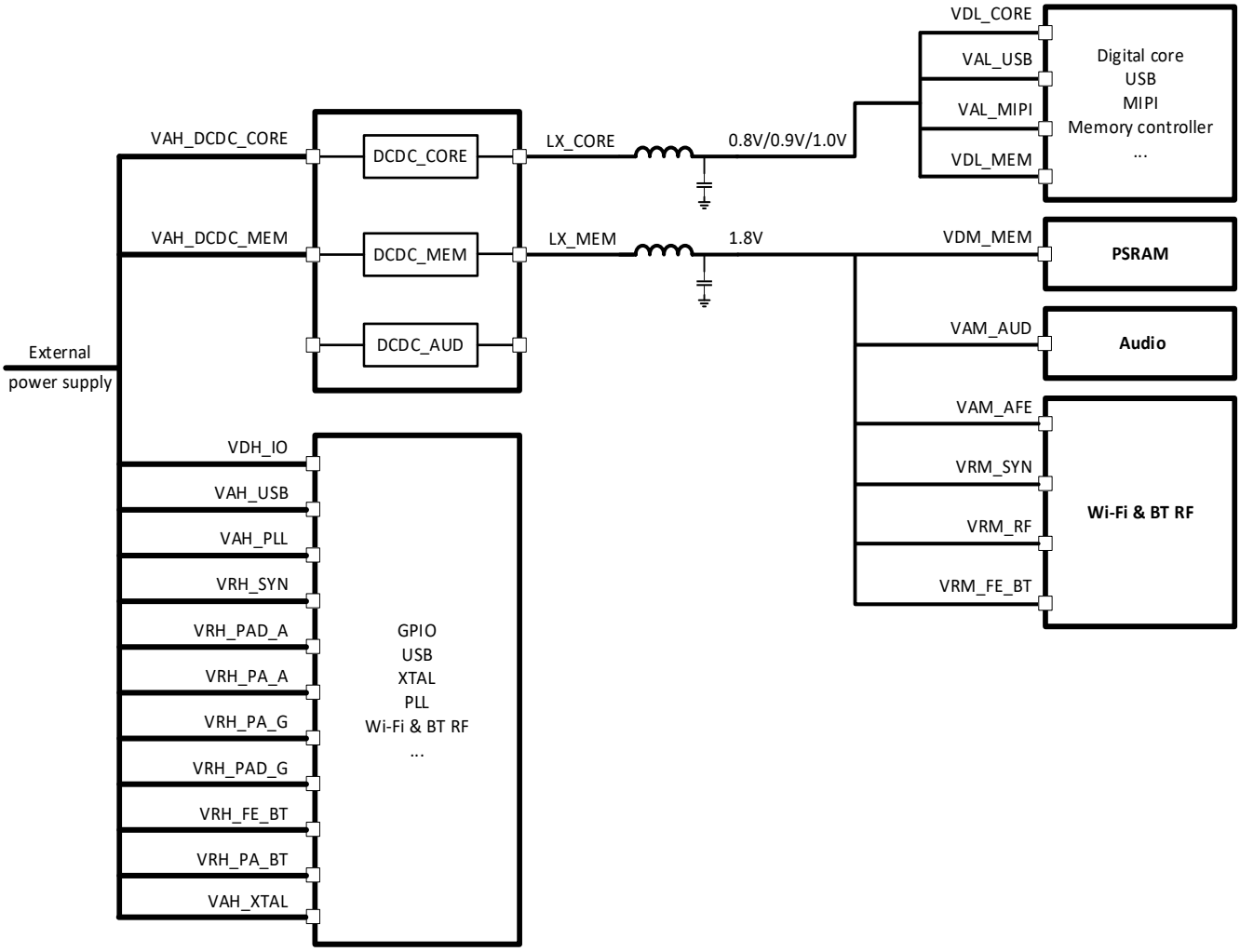


Figure 3-2 Power block diagram for RTL8730ELH-VA3 and RTL8730EAH-VA3/VD3

3.1.2 Power Supply Supervisor

The RTL8730E has integrated a power-on reset (POR) circuit and a brownout detect (BOD) circuit.

3.1.2.1 Power-on Reset (POR)

The POR supervisor monitors VDH_IO0 power supply input during power on and power off.

- When VDH_IO0 is higher than V_{POR_H}, the chip releases the internal reset.
- When VDH_IO0 is lower than V_{POR_L}, the chip remains in reset mode.

Refer to Section *Power Sequence* for more details.

3.1.2.2 Brownout Detect (BOD)

The BOD supervisor monitors VDH_IO0 power supply input. The BOD circuit is disabled by default and can be enabled by setting the register. The BOD circuit can work in reset mode or interrupt mode and has independent falling threshold V_{BOD_L} and rising threshold V_{BOD_H}.

- When VDH_IO0 drops below V_{BOD_L}, the BOD circuit will trigger an interrupt or a reset depending on the register configuration.
- When VDH_IO0 rises above V_{BOD_H}, the BOD circuit will release the internal reset. V_{BOD_L} and V_{BOD_H} can be chosen by setting the register, but V_{BOD_H} must be set higher than V_{BOD_L}.

Refer to Section *Power Sequence* for more details.

3.1.3 Power Domain

There are different power domains in the RTL8730E, and AON, SYSON, and SOC are three main power domains in the digital system. Users can flexibly power up different power domains to achieve the best balance between the performance and power consumption. Functions in different power domains will be turned off differently in different power-saving modes. More information about power domains and wakeup sources are depicted in *Figure 3-3*.

Some peripherals (such as UART, LOGUART, …) can only wake up the system under some special conditions, refer to *Table 3-2* for more details.

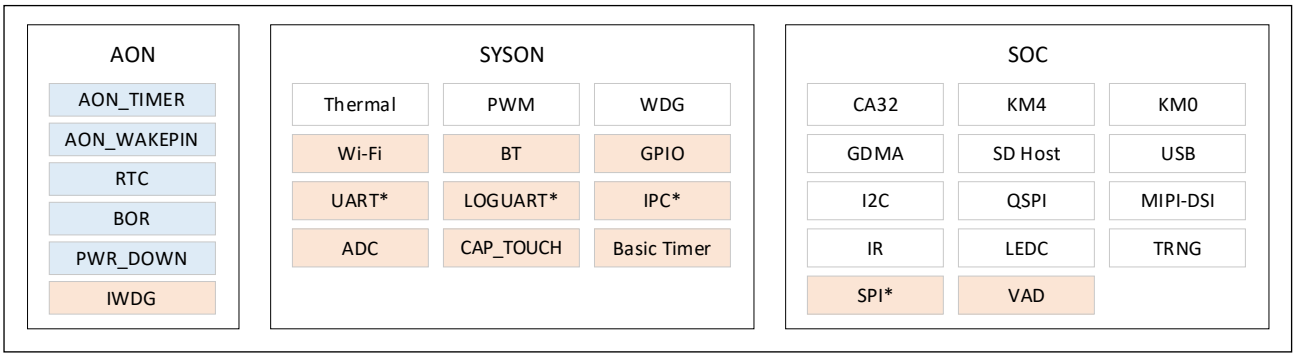


Figure 3-3 Power domains and wakeup sources

3.1.4 Power Mode

By controlling the power and clock of individual functions, the RTL8730E can support both active mode and power saving mode.

There are two special power-saving modes, sleep mode and deep-sleep mode, which are to achieve low power consumption with different peripherals running.

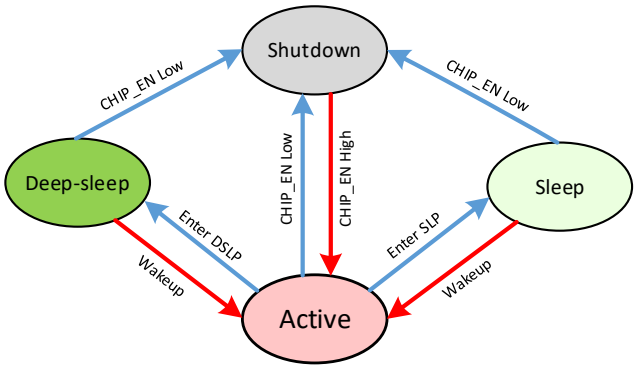


Figure 3-4 Switch among different power modes

3.1.4.1 Active Mode

In active mode, all the digital modules are powered on. Each of them can be configured as active or clock-gated, depending on the application requirement. In addition, there are individual power-down controls for some of the analog peripherals.

3.1.4.2 Sleep Mode

There are independent sleep modes for each of the three CPUs. In sleep mode, CPUs are stopped and cannot execute instructions until either a reset or an interrupt occurs. Meanwhile, most of the functions are powered off or clock-gated to save power. The processors' state and registers, SYSON and AON domains peripherals' registers, internal SRAM values, and PSRAM or DDR (if exist) values are maintained.

In sleep mode, two kinds of peripherals can be configured to continue operating.

- One kind is the peripherals which can be used as wakeup sources. Any interrupt/event can trigger the peripheral to wake up the system.
- The other kind is the peripherals which are needed to keep the wireless link alive. The system memory can be optionally set to retention mode, so that the system can wake up quickly without reloading content from Flash.

3.1.4.3 Deep-sleep Mode

In deep-sleep mode, all functions are powered off except the AON functions. This is to achieve ultra-lower power consumption. The processors' state and registers, SYSON domain peripherals' registers, internal SRAM values, and PSRAM or DDR (if exist) values are lost. Only AON registers and retention SRAM on AON domain are maintained. Only AON domain peripherals such as AON TIMER, AON GPIO, RTC and BOR can be left running.

The system can only be woken up by the interrupt/event generated from AON domain. When exiting from the deep-sleep mode, the system will go through normal boot flow.

3.1.4.4 Wakeup Source

Table 3-1 lists the peripheral/clock configuration in different power modes.

Table 3-1 Peripheral/clock configuration in different power modes

Peripheral/clock	**Power mode**				
	Active	Sleep		Deep-sleep	Shutdown
		Clock-gating	Power-gating		
PLL	ON	Software configurable	Software configurable	OFF	OFF
XTAL	ON	Software configurable	Software configurable	OFF	OFF
OSC4M	ON	Software configurable	Software configurable	OFF	OFF
SWR	ON	Software configurable	Software configurable	OFF	OFF
WLAN	Software configurable	Software configurable	Software configurable	OFF	OFF
BT	Software configurable	Software configurable	Software configurable	OFF	OFF
CPU + cache	ON	Clock-gated	Power off	OFF	OFF
SRAM	ON	Retention/shutdown	Retention/shutdown	OFF	OFF
Retention SRAM	ON	Retention	Retention	Retention	OFF
SYSON peripherals	Software configurable	Software configurable	Software configurable	OFF	OFF
AON peripherals	Software configurable	Software configurable	Software configurable	Software configurable	OFF

Table 3-2 lists the wakeup sources of power-saving mode.

Table 3-2 Wakeup sources of power-saving mode

Power-saving mode	**Wakeup source**	**Restriction**
Sleep mode	WLAN	
	BT	
	IWDG	
	Basic Timer	
	UART	● When using UART as a wakeup source: ■ If the Rx clock source is XTAL40M, do not turn off XTAL during sleep. ■ If the Rx clock source is OSC2M, do not turn off OSC4M during sleep. ● The portion of the command used to wake up that exceeds the FIFO depth (64B) will be lost.
	LOGUART	● When using LOGUART as a wakeup source: ■ If the Rx clock source is XTAL40M, do not turn off XTAL during sleep. ■ If the Rx clock source is OSC2M, do not turn off OSC4M during sleep. ● The portion of the command used to wake up that exceeds the FIFO depth (16B) will be lost.
	GPIO	
	CAP_TOUCH	
	ADC	
	IPC	The IPC can only wake up CA32 and KM4, but not KM0.
	SPI	When using SPI as a wakeup source, do not turn off HP platform and PLL.
	VAD	

Deep-sleep mode	RTC	
	AON_TIMER	
	AON_WAKEPIN	
	BOR	
	PWR_DOWN	

3.2 CPU Architecture

3.2.1 Dual-core CA32 Processor

The dual-core CA32 processor uses an efficient, 8-stage, in-order pipeline that has been extensively optimized to provide the 32-bit Armv8-A features in the smallest footprint and power. It delivers higher efficiency and higher performance than the Cortex-A7 and Cortex-A5 processors. It also benefits from an integrated L2 cache designed for low-power, with lower transaction latencies and improved OS support for cache maintenance.

The RTL8730E contains dual-core CA32 processors with the following features:

- Armv8-A architecture
- AArch32 for full backward compatibility with Armv7
- 8-stage pipeline to support high clock frequency
- Arm NEON advanced SIMD
- VFPv4 Floating point
- Arm TrustZone security technology
- Integrated generic interrupt controller (GIC) with 256 shared peripheral interrupts
- JTAG and Serial Wire Debug ports, up to 6 instruction breakpoints and 4 data watchpoints

The following interfaces are supported:

- RAM/ROM interface for instructions and data
- Local memory interface for fast peripheral register access
- External and internal interrupt sources
- JTAG for debugging

The CA32 is designed to run up to 900MHz at 0.9V and 1.2GHz at 1.0V.

3.2.2 KM4 Processor

The KM4 processor is a 3-staged pipelined 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, floating-point computation, Digital Signal Processing (DSP) extension and M-profile Vector Extension (MVE) instructions, TrustZone-M security for hardware-enforced isolation, and a high level of support block integration. It achieves an optimal blend between real-time determinism, energy efficiency, software productivity, and system security which opens the door for many new applications and opportunities across diverse markets.

The KM4 processor has the following features:

- Armv8.1-M architecture
- 3-stage pipeline to support the clock frequency of up to 333MHz
- Thumb/Thumb-2 technology
- TrustZone-M technology with Security Attribution Unit (SAU) of up to 8 regions
- 64K bytes I-Cache, 32K bytes D-Cache
- Single-precision floating-point unit (FPU)
- Memory Protection Unit (MPU) with up to 16 regions per security state
- Non-maskable Interrupt (NMI) and physical interrupts with 8 to 256 priority levels
- Waking up the processor from state retention power gating or when all clocks are stopped
- Integrated wait for event (WFE) and wait for interrupt (WFI) instructions
- JTAG and Serial Wire Debug ports, up to 8 instruction breakpoints and 1 data watchpoint

The KM4 is designed to run up to 250MHz at 0.9V and 333MHz at 1.0V.

3.3 Memory Mapping

The RTL8730E incorporates several distinct memory regions. Program memory, data memory, registers, and I/O ports are organized within the same linear 4Gbytes address space. The bytes are coded in memory in little-endian format.

The addressable memory space is divided into multiple main blocks, as shown in *Table 3-3*. All the memory areas that are not allocated to on-chip memories and peripherals are considered “RSVD” (reserved).

Table 3-3 Address space main blocks

Base address	End address	Size (bytes)	Function		TrustZone
0x0000_0000	0x0007_FFFF	512K	CA32 Bus ROM (Bus 1KB)	ROM Flash	-
			KM4 ITCM ROM (CPU internal)		
			KM0 ITCM ROM (CPU internal)		
0x0008_0000	0x000F_FFFF	512K	KM4 DTCM ROM (CPU internal)		
			KM0 DTCM ROM (CPU internal)		
0x0010_0000	0x07FF_FFFF	127M	RSVD		
0x0800_0000	0x0FFF_FFFF	128M	SPI NOR/NAND Flash		
0x1000_0000	0x1FFF_FFFF	256M	RSVD		-
0x2000_0000	0x20FF_FFFF	16M	HP SRAM (actually 256KB)	SRAM	-
0x2100_0000	0x21FF_FFFF	16M	RSVD		
0x2200_0000	0x22FF_FFFF	16M	Extension SRAM		
0x2300_0000	0x23FF_FFFF	16M	LS SRAM (actually 128KB)		
0x2400_0000	0x2FFF_FFFF	192	RSVD		
0x3000_0000	0x3FFF_FFFF	256M	TrustZone secure address (SRAM)		Secure
0x4000_0000	0x41FF_FFFF	32M	HP peripherals group	Peripherals	-
0x4200_0000	0x42FF_FFFF	16M	LS peripherals group		
0x4300_0000	0x43FF_FFFF	16M	WLAN firmware		
0x4400_0000	0x440F_FFFF	1M	SPI Flash Controller		
0x4410_0000	0x4FFF_FFFF	191M	RSVD		
0x5000_0000	0x5FFF_FFFF	256M	TrustZone secure address (Peripherals)		Secure
0x6000_0000	0x6FFF_FFFF	256M	External PSRAM/DDR (selectable)	DRAM	-
0x7000_0000	0x7FFF_FFFF	256M	TrustZone secure address (DRAM)		Secure
0x8000_0000	0x8003_FFFF	256K	CA32 internal debug register		-
0x8004_0000	0x9FFF_FFFF	511.75M	RSVD		-
0xA000_0000	0xA00F_FFFF	1M	CA32 debug register	CA32	-
0xA010_0000	0xA010_7FFF	32K	CA32 GIC		
0xA010_8000	0xAFFF_FFFF	254.96875M	RSVD		
0xB000_0000	0xB000_1FFF	8K	RSVD		Secure
0xB000_2000	0xB000_2FFF	4K	CA32 timestamp/system counter		
0xB000_3000	0xBFFF_FFFF	255.98828125M	RSVD		
0xC000_0000	0xDFFF_FFFF	512M	RSVD		-
0xE000_0000	0xE0FF_FFFF	16M	System PPB Device (RAM predefined)		-
0xE100_0000	0xFFFF_FFFF	496M	RSVD		

NOTE

The security attribution of one address space is determined by the bit[28] of this address.

3.4 Memory Subsystem

The RTL8730E incorporates high-speed memories with on-chip SRAM and stacked selectable DRAM (either DDR or PSRAM). A dedicated SPI Flash controller provides a flexible and efficient way to access NOR/NAND Flash (e.g. byte and block access). A multi-layer AXI interconnect support internal and external memories access.

3.4.1 ROM/Cache

- CA32:
  - 32K bytes L1 instruction cache (I-Cache) for each core
  - 32K bytes L1 data cache (D-Cache) for each core
  - 256K bytes L2 cache
- KM4:
  - I-Cache: 64K bytes
  - D-Cache: 32K bytes
  - IROM: 256K bytes
  - DROM: 96K bytes

3.4.2 On-chip SRAM

The on-chip SRAM in HP platform consists of two blocks:

- A general purposed on-chip 256KB contiguous SRAM for system heap and application, whose clock is configurable but cannot exceed 333MHz.
- A dedicated connectivity 296KB SRAM shared with Wi-Fi and BT (low protocol stack). If user's application applies Wi-Fi function or BT function, the corresponding SRAM would be occupied and cannot be used as general SRAM anymore.

LS platform features 128KB contiguous SRAM.

All the SRAMs can be accessed as bytes (8 bits), half-words (16 bits), or full words (32 bits) by processors, DMA engine, and other AXI/AHB masters.

The SRAMs can be disabled or enabled in the Power Management Unit (PMU) block to save power, and can also keep power for quickly resuming from sleep mode when the system enters sleep mode.

3.4.3 Retention SRAM

LS platform also features another 512B retention SRAM next to the 128KB SRAM, in order to allow saving data with minimal power usage during deep-sleep mode.

This SRAM can be accessed by all CPUs and DMA engine.

3.4.4 Flash Memory

The Flash memory consists of a SPI Flash controller and a Flash memory array module. The SPI Flash controller acts as an interface between the system bus and the flash memory device. It implements the erase and program Flash memory operations, and the read/write protection mechanisms. It accelerates code execution with a system of instruction prefetch and cache lines.

The SPI Flash controller of RTL8730E supports SPI NAND/NOR Flash with Single/Dual/Quad I/O pins. The I/O voltage is 3.3V. It can run up to 100MHz Single-Data-Rate (SDR) speed.

3.4.5 PSRAM/DDR

The RTL8730E incorporates high-speed memories with stacked selectable DRAM (either DDR or PSRAM).

3.4.5.1 PSRAM

The Random Access Memory (RAM) array uses dynamic cells that require periodic refresh. Refresh control logic within the device manages the refresh operations on the RAM array when the memory is not being actively read or written by the HyperBus interface master (host). Since the host is not required to manage any refresh operations, the DRAM array appears to the host as though the memory uses static cells that retain data without refresh. Hence, the memory can also be described as Pseudo-Static RAM (PSRAM).

The PSRAM has the following features:

- Clock rate: up to 250MHz
- Double data rate

- 8-bit I/O
- Supports half-sleep and deep power-down mode

3.4.5.2 DDR

The HyperBus is a low-signal-count, Double Data Rate (DDR) interface that achieves high-speed read and write throughput. The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals.

The DDR has the following features:
- Supports DDR2/DDR3/DDR3L
- Clock rate: up to 533MHz
- Double data rate
- 16-bit I/O

3.5 Security

The RTL8730E is designed to safely hold security-related data such as cryptographic keys and general purpose security information with the following security techniques.
- Secure boot
- Arm TrustZone and TrustZone-M
- True Random Number Generator (TRNG)
- Hardware crypto engines
- ECDSA/EdDSA/RSA engines
- Whole or partial Flash encryption
- Read Protection (RDP)
- Secure JTAG/SWD
- 2K bytes OTP fuses, up to 2K bits for users

3.5.1 Secure Boot

Secure boot aims at firmware protection, which prevents attackers from modifying or replacing firmware maliciously. When the chip is power on, the secure boot ROM executes to check the validation of the image signature.

The RTL8730E supports the following algorithms of secure boot:
- Signing/Authentication algorithm:
  - Ed25519
  - ECDSA
- Hash algorithm:
  - SHA
  - HMAC

3.5.2 Elliptic Curve Signature Algorithm (ECDSA)

The ECDSA implements a complete asymmetric (public/private) key cryptographic signature solution based upon Elliptic Curve Cryptography and the ECDSA signature protocol. The device features hardware acceleration for the NIST standard SECP256K1 and P256 prime curve includes ECDSA signature generation, ECDH key agreement, and ECDSA public-key signature verification. The processing of it is faster than software.

It has the following features:
- Support the following Elliptic Curves and all other Elliptic Curves with N no more than 256 bits:
  - ECDSA_ECP_SECP192R1
  - ECDSA_ECP_SECP224R1
  - ECDSA_ECP_SECP256R1
  - ECDSA_ECP_BP256R1
  - ECDSA_ECP_CURVE25519
  - ECDSA_ECP_SECP192K1
  - ECDSA_ECP_SECP224K1
  - ECDSA_ECP_SECP256K1
- Two private keys in OTP which can only be accessed by hardware engine.
- Performance: about 3.5ms for signature verification which is much faster than software

3.5.3 Edwards-curve Digital Signature Algorithm (EdDSA)

The EdDSA is a variant of Schnorr's signature system with (possibly twisted) Edwards curves. The hardware EdDSA engine supports ED25519 curve and accelerates applications that need EdDSA signature verification or some EdDSA basic core functions. Hardware EdDSA engine executing these functions can not only reduce software overhead but also save CPU and memory resources. The processing of it is faster than software.

Programmers majorly use this engine to do signature verification platform for trusted boot and update. For the trusted boot and trusted firmware update process, a minimum key size of EdDSA public key requirement is 256 bits (32 bytes) (ARM PSA suggestion).

3.5.4 RSA Engine

RSA is an asymmetric encryption algorithm widely used in the field of information security, especially for encryption and digital signatures. RSA engine is an encryption engine specifically designed to perform RSA encryption and decryption.

Realtek's RSA engine supports operations below:

- RSA encryption:
  - Key: 1024 bits
  - Key: 2048 bits
  - Key: 3072 bits
- RSA decryption:
  - Key: 1024 bits
  - Key: 2048 bits
  - Key: 3072 bits

3.5.5 Hardware Crypto Engine (IPsec)

The RTL8730E integrates two hardware crypto engines: SHA engine and AES engine, which can accelerate applications that need cryptographic functions, such as authentication, encryption and decryption. Hardware crypto engine executing these functions cannot only reduce software overhead but also save CPU and memory resources, and the processing is more secure and faster than software.

Realtek's IPsec provides the basic cryptographic features:

- Authentication algorithms
  - General cryptographic hash function
    - MD5 (weak, not recommended)
    - SHA1 (weak, not recommended)
    - SHA2-224
    - SHA2-256
    - SHA2-384
    - SHA2-512
  - HMAC (Hash-based message authentication code)
    - HMAC_MD5 (weak, not recommended)
    - HMAC_SHA1 (weak, not recommended)
    - HMAC_SHA2-224
    - HMAC_SHA2-256
    - HMAC_SHA2-384
    - HMAC_SHA2-512
- Cipher (Encryption/Decryption) algorithms
  - AES-128/192/256
    - ECB (Electronic Codebook) mode (weak, not recommended)
    - CBC (Cipher Block Chaining) mode
    - OFB (Output Feedback) mode
    - CFB (Cipher Feedback) mode
    - CTR (Counter) mode (weak, not recommended)
    - GCM (Galois/Counter Mode) mode
- Secure mode: 4 keys in OTP, two for secure mode and two for non-secure mode, which can only be accessed by hardware engine.

3.5.6 Secure Image Protection (RSIP)

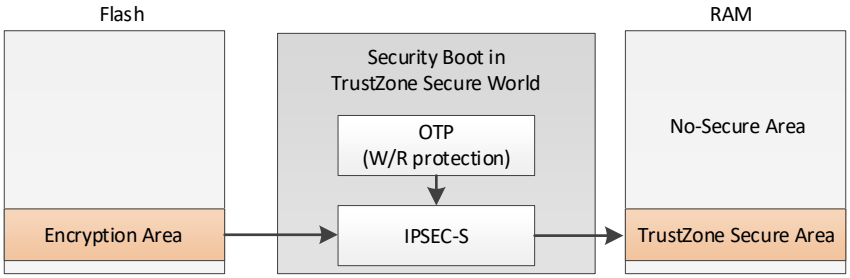
Generally, both firmware and some data are stored in Flash memory. The SPI Flash controller is used to transmit/receive data from/to SPI Flash memory. In order to protect firmware, the code and data in Flash can be encrypted with Advanced Encryption Standard (AES) algorithm. The RSIP is mainly used for MMU and image decryption.

The RSIP consists of two parts:
- RSIP-AES: performs Flash decryption on the fly.
- RSIP-MMU: used for virtual-to-physical memory address translation.

The RSIP-AES has the following features:
- The whole or part of Flash can be encrypted.
- Encrypted Flash data is decrypted by hardware engine on the fly.
- Optional crypto algorithm: AES-256 CTR mode and XTS mode.
- Key length is 256 bits, which should be programmed into OTP, and can be set to Read Protection and Write Protection.
- IV length is 128 bits, the higher 64 bits can be defined by user, and the lower 64 bits are decided by the address.
- Keys are auto-loaded to hardware engine; software cannot access them after read protection is enabled.
- Keeps 8 IVs in the engine.
- 8 entries to enable decryption for specific areas, and every entry can choose a different IV and mode independently.

3.5.1 Read Protection (RDP)

Read Protection (RDP) is used to protect security-critical code, which is implemented with Arm TrustZone technology. The security-critical code is stored in the Flash with encrypted form, and would be decrypted in secure bootloader and loaded into secure SRAM protected by TrustZone.



3.5.2 True Random Number Generator (TRNG)

The TRNG integrated in RTL8730E is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

It has the following features:
- Delivers 32-bit true random numbers, produced by an analog entropy source
- Embeds with a health test unit and an error management unit
- Two independent FIFOs, the secure one has a higher priority.
- Throughput of the TRNG is up to about 2Mbps.

The clock of TRNG will be enabled in ROM code. It has a dedicated ROSC, and can generate a random clock with 4MHz ~ 7MHz.

3.6 Radio Subsystem

The RTL8730E includes an integrated dual-band direct conversion radio that supports WLAN & Bluetooth 2.4GHz band and WLAN 5GHz bands.

3.6.1 RF Block Diagram

The radio frequency (RF) block diagram of RTL8730E, including WLAN and BT modem, is given in *Figure 3-5*.

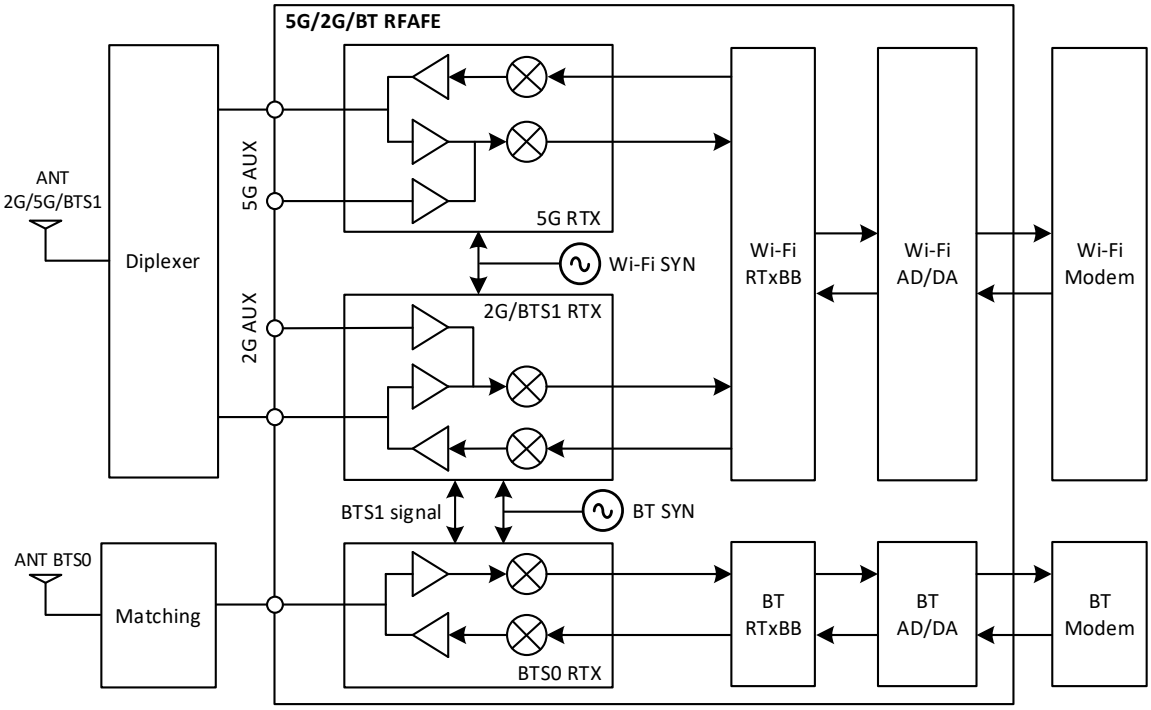


Figure 3-5 RF block diagram

3.6.2 WLAN

The RTL8730E includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4GHz and 5GHz Wireless LAN systems. It is designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4GHz unlicensed ISM or 5GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing and gain control functions. The integrated on-chip baluns convert the fully differential transmit and receive paths to single-ended signal pins.

The radio subsystem of RTL8730E consists of the following modules:

- Receiver
- Transmitter
- Real-time calibration

3.6.2.1 WLAN Receiver

The RTL8730E has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4GHz ISM band or the entire 5GHz U-NII band. At port RFIO_G, an on-chip low-noise amplifier (LNA) in the 2.4GHz path is shared between the Bluetooth S1 and WLAN 2.4GHz receivers, while the 5GHz at port RFIO_A receiver path has a dedicated on-chip LNA. Because the NF of receiver path is lower enough, external LNA is not necessary, which can increase the receive sensitivity no more than 1dB.

3.6.2.2 WLAN Transmitter

The baseband data is modulated and up-converted to the 2.4GHz ISM or 5GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11 b/g/n/ac/ax specifications without the need for

external PAs. But if you do want high Tx power, external PA can be added. When using the internal PAs, closed-loop output power control is completely integrated.

3.6.2.3 Real-time Calibration

The RTL8730E adopts real-time and automatic on-chip calibration mechanisms to ensure that normal radio system can operate perfectly, and users do not need to do extra operations to enhance Tx/Rx performance. These calibration mechanisms which are merged into software or hardware continually compensate for temperature and process variations across components. Examples of some of these algorithms are digital correction, such as:

- I-Q compensation calibration
- Digital pre-distortion calibration for good EVM performance of the transmitter
- LO calibration for carrier leakage reduction

3.6.3 Bluetooth

3.6.3.1 Bluetooth Transceiver

Fully integrated radio transceiver is compliant with Bluetooth SIG test specification, and designed for low power consumption, excellent transmit and receive performance in the ISM band.

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

3.6.3.2 Bluetooth Transmitter

The modulator translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

3.6.3.3 Bluetooth Receiver

The LNA amplifies a low energy RF signal to the desired level without significantly increasing the noise power. When input power is high, the designed limits non-linearity. The Receive mixer is a device whose input is an RF signal, and the output is an IF signal. The IF signal is then passed along the IF path to the demodulator.

3.7 WLAN Subsystem

3.7.1 WLAN Baseband

The RTL8730E is designed to support 802.11 a/b/g/n/ac/ax single-stream WLAN. The PHY has implied efficient algorithms to provide high throughput and enhanced sensitivity, including advanced algorithms for DC, frequency and timing offset estimation, adaptive frequency domain equalizer, and a Viterbi decoder.

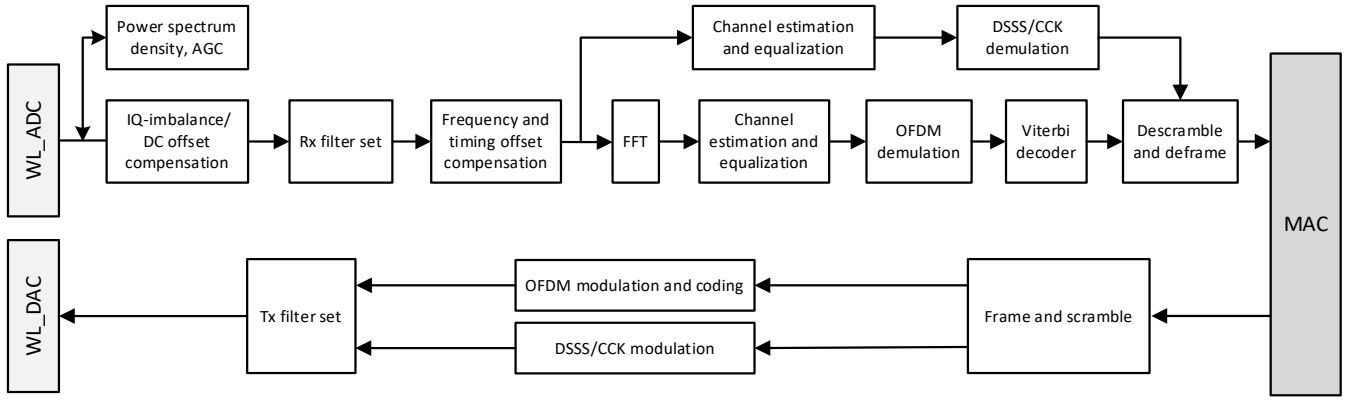


Figure 3-6 PHY block diagram

The WLAN baseband of RTL8730E supports the following features:

- 802.11 a/b/g/n/ac/ax
- 802.11n MCS0-7, 20MHz bandwidth, up to 72.2Mbps of data rate
- 802.11ac MCS0-8, 20MHz bandwidth, up to 86.7Mbps of data rate
- 802.11ax MCS0-9, 20MHz bandwidth, up to 114.7Mbps of data rate
- Integrated 2.4GHz/5GHz PA and LNA, and T/R switch
- Integrated 2.4GHz and 5GHz balun
- Support both internal and external PA
- Adjustable transmitting power
- Supports Channel State Info (CSI)
- Supports Dynamic Frequency Selection (DFS)
- Supports Tx Low-Density Parity Check (LDPC), Tx Binary Convolutional Code (BCC), and Rx BCC
- Supports Rx STBC 2x1
- Supports SU/MU Beamformee
- Supports Rx DL-OFDMA, Tx UL-OFDMA
- Supports 802.11ax Dual Carrier Modulation (DCM)/ER Tx/Rx
- Supports Spatial Reuse to maximize parallel transmissions
- Short guard interval (0.8ns)
- Supports digital pre-distortion to enhance PA performance
- Smoothing for channel estimation
- Antenna diversity

The RTL8730E supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and select the best antenna to minimize the effects of channel fading.

3.7.2 WLAN MAC

The WLAN MAC of RTL8730E applies low-level protocol functions automatically. It supports the following features:

- Frame aggregation for increased MAC efficiency (A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Supports Target Wake Time (TWT) function for power saving
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- Supports Enhanced Distribution Channel Access (EDCA) and MU EDCA
- Transmitting beamforming as beamformee
- Supports 2 Network Allocation Vector (NAV)
- Supports Basic Service Set (BSS) color
- Supports Time Synchronization Function (TSF) auto-sync
- IEEE 802.11i (WPA, WPA2, WPA3), open, shared key, and pair-wise key authentication services
- Rx trigger frame (except GCR MU-BAR and NFRP)
- Supports AP/STA/Concurrent mode (802.11ax AP not supported)
- Supports Multi Channel Concurrent (MCC) mode by software TDMA

3.8 Bluetooth Subsystem

The RTL8730E integrates a hardware link layer controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

3.8.1 Bluetooth Baseband

The Bluetooth baseband of RTL8730E supports the following features:

- Compliant with Bluetooth Core Specification including BR/EDR/LE-1M/LE-2M/LE-Coded (long range).
- Fully integrated balun and synthesizer minimize external components.
- RF circuit design minimizes power consumption while keeping excellent performance.
- 40MHz main clock
- Supports serial Flash for firmware storage and parameter upgrade
- Adaptive Frequency hopping (AFH)

3.8.2 Bluetooth Link Controller

- Bluetooth 5.3 specification compliant, dual mode
  - Bluetooth Basic Rate/Enhanced Data Rate (BR/EDR)
  - Bluetooth Low Energy (BLE)
- Supports all packet types in BR/EDR
- High-speed UART interface for Bluetooth data transmission
- Integrated MCU to execute Bluetooth protocol stack
- Supports Secure Simple Pairing
- Enhanced Bluetooth/WLAN Co-existence Control to improve transmission quality in different profiles
- Supports BLE Connection Isochronous Channel
- Supports multiple Low Energy states

3.9 Timers and Watchdogs

The RTL8730E includes twelve basic timers, one pulse timer, one PWM timer, also a RTC timer, a debug timer and five watchdog timers.

Table 3-4 Timer feature comparison

Type	Number	Counter resolution	Counter mode	Prescaler	INT generation	Sleep mode	Secure mode
Basic timer	12	32-bit	Up	×	✓	✓ (TIM0 ~ TIM7)	✓
Capture timer	1	16-bit	Up	16-bit	✓	×	✓
PWM timer	1	16-bit	Up	16-bit	✓	×	✓

3.9.1 Basic Timer (TIM0 ~ TIM7, TIM10 ~ TIM13)

The RTL8730E has twelve basic timers.
- LS platform: TIM0, TIM1, TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, whose clock source is SDM32kHz.
- HP platform: TIM10, TIM11, TIM12, TIM13, whose clock source is XTAL 1MHz, divided by XTAL40M.

The basic timers may be used as generic timers for time-based generation.

All the basic timers support:
- Resolution: 32-bit
- Counter mode: up
- Interrupt generation
- Secure mode

Otherwise, the basic timers in LS platform supports wakeup from sleep mode.

3.9.2 Capture Timer (TIM9)

The RTL8730E has one capture timer (TIM9) in HP platform.

The capture timer can be used for a variety of purposes, including measuring the pulse lengths or numbers of input signals.

The pulse timer supports:
- Clock source: XTAL40MHz
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- Statistic pulse width
- Statistic pulse number
- Secure mode

3.9.3 PWM Timer (TIM8)

The RTL8730E has one PWM timer (TIM8) in HP platform.

The PWM timer can be used for a variety of purposes, including measuring the pulse frequency of input signals (input capture) or generating

output waveforms (PWM) continuously or only once in response to a stimulus. Pulse lengths and waveform periods can be modulated from a few microseconds to several seconds using the timer prescaler.

The PWM timer supports:
- Channel: 6
- Clock source: XTAL40MHz
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- One pulse mode with configurable default level and trigger edge
- PWM mode with polarity selection
- Interrupt generation
- Duty cycle: 0% ~ 100%
- Phase shift
- Secure mode

3.9.4 Real-time Clock (RTC) Timer

The RTC timer is an independent binary coded decimal (BCD) timer/counter.
- One 32-bit register: contains the seconds, minutes, hours (12- or 24-hour format) expressed in BCD format.
- One 32-bit register: contains the days expressed in binary format.
- One 8-bit register: contains the years expressed in binary format.

The RTC timer provides a set of continuously running counters in AON domain to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or watchdog reset, or when the device wakes up from sleep or deep-sleep mode.

The RTC timer supports:
- Prescaler: 9-bit asynchronous prescaler and 9-bit synchronous prescaler
- Time with seconds, minutes, hours (12- or 24-hour format) days and years
- Daylight saving compensation programmable by software
- One programmable alarm with interrupt function. The alarm can be triggered by any combination of the time fields.
- Maskable interrupt/event:
  - Alarm
  - Day threshold
  - Wakeup timer
- Digital calibration circuit
- Register write protection
- Periodic auto-wakeup
- A digital calibration to compensate for some deviation
- External clock source
- Keep running as long as the supply voltage remains in the operating range

When the system boots up, the clock source of RTC timer is from SDM32K. After calibrating the internal XTAL, the RTC module's deviation is less than 2s per 24 hours (typical value).

3.9.5 Generic timers (CA32)

The generic timers embedded inside CA32 are fed by value from system timing generation (STGEN). The CA32 processor provides a set of four timers for each processor:
- Physical timer for use in secure and non-secure modes. The registers for the physical timer are banked to provide secure and non-secure copies.
- Virtual timer for use in non-secure modes.
- Physical timer for use in hypervisor mode.

Generic timers are not memory-mapped peripherals. They are accessible only by specific CA32 coprocessor instructions.

Timestamp generator memory-mapped registers are located in two memory frames, identified by different base addresses:
- The locations of the RO copies of CNTCV are defined relative to the PSELCTRL base address.
- The locations of all the other registers are defined relative to the PSELREAD base address.

The PSELCTRL is implemented only in the secure memory space, whose address is 0xB0002000; a status frame, with base address PSELREAD located in 0xA0002000.

3.9.6 Debug Timer

The debug timer is a common timestamp for all debug messages originating from all on-die processors and processor execution domains (application, kernel and firmware). It also includes a lock-free increment counter. It features:

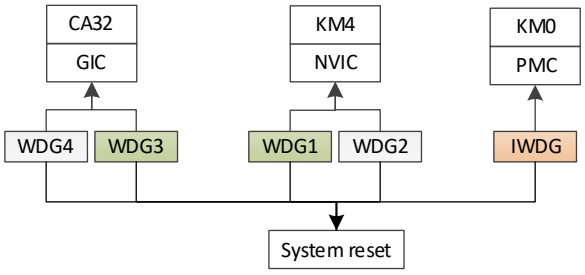
- A simple 32-bit wrap timer
- A lock-free counter

The counter is enabled by default. The counter wraps around to zero and continues to count once it reaches 32'hFFFFFFFF. A write to the timestamp will set the current value of it, however, it must continue to increment at the base of the new setting value if the writing happens when the counter is active.

The debug timer has two types of clock sources: XTAL and internal 32K. The XTAL clock may be gated in sleep mode. If you select XTAL as the clock source in sleep mode, the debug timer will stop counting, and all the registers will be maintained. The counter will resume the increment immediately after XTAL resumes. You can select 32K as the clock source in sleep mode; however, the counter itself needs 220us to switch the clock before continuing counting. In this period, writing to this IP is not allowed. All the registers will be reset to the initial values after wakeup from deep-sleep mode.

3.9.7 Watchdog Timers

The RTL8730E includes five watchdog timers: one independent watchdog timer (IWDG) and four system watchdog timers (WDG). The four system watchdog timers are divided into two groups, and each group has a secure watchdog timer and a non-secure watchdog timer.



These watchdog timers are intended to recover from an unforeseen fault causing the application program to abandon its normal sequence. A system reset will be triggered if the watchdog is not fed or fed out the proper fed window. All the five watchdogs can reset the whole system if a watchdog barks or an unexpected error happens. After reset, a flag can tell which watchdog is fired.

Once enabled, the watchdogs cannot be disabled.

3.9.7.1 Independent Watchdog (IWDG)

The IWDG is based on a 12-bit down-counter and 8-bit prescaler. It is dedicated to KM0. The IWDG is powered by always-on power and clocked from always-on OSC100K, meaning that it can stay active even if the main power or crystal fails. Also, IWDG can be configured to start by hardware at the very beginning of reset.

In sleep mode, the IWDG can keep running or gating; while in deep-sleep mode, IWDG will be disabled by hardware.

3.9.7.2 System Watchdog (WDG1, WDG2, WDG3, WDG4)

The WDG can work as a window watchdog by setting the appropriate window in the WDG_WIN.

The WDG1 and WDG3 are secure.

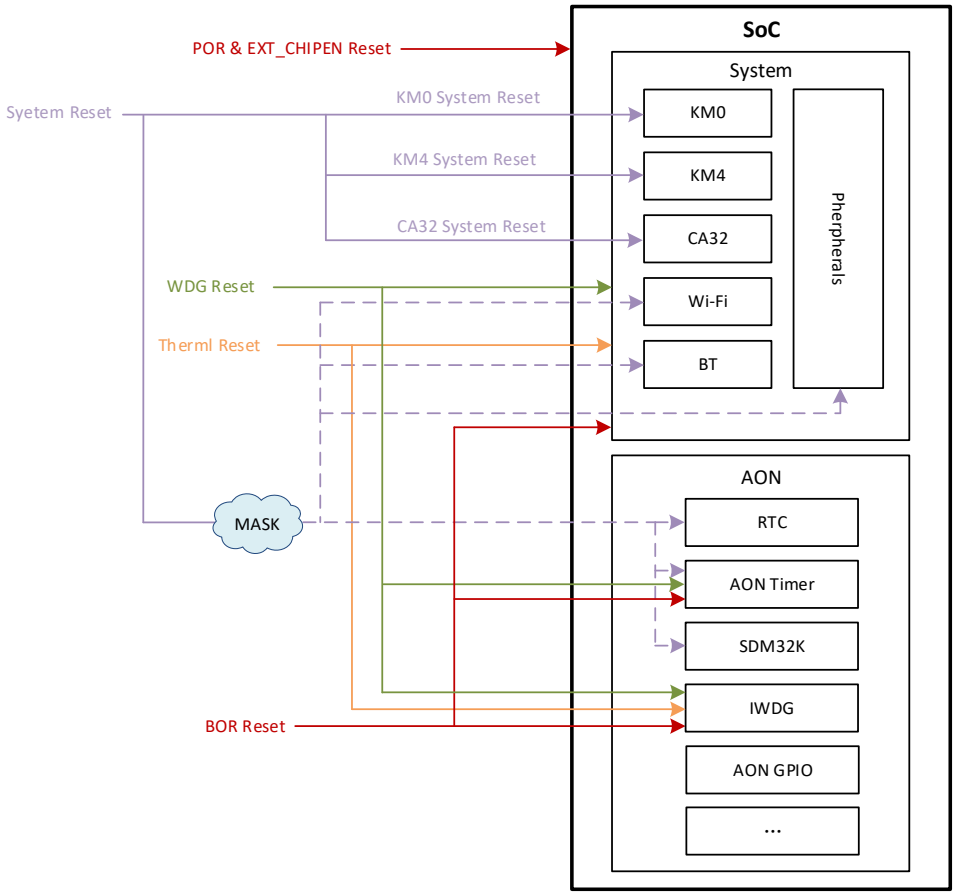
In sleep mode, each of WDGs can maintain its register but keep freezing, counting down will resume after the CPU leaves from sleep; while in deep-sleep mode, WDGs will be powered off.

3.10 Reset and Clock Control (RCC)

The RCC module manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides high flexibility in the choice of clock sources and allows the application of clock ratios to improve power consumption.

3.10.1 Reset Control

3.10.1.1 Reset Diagram



3.10.1.2 Reset Types

The following reset sources or events are able to generate a reset.

Reset type	Description
POR	A regulator power-on reset is generated when power on
BOR	A regulator brownout reset is generated when BOR detected
EXT_POR	A external power on reset is generated when external power on
WDG	A watchdog reset is generated when watchdog timeout
THM	A thermal reset is generated when abnormal temperature detected
SYSRST	Generated when CPU controls NVIC reset register

3.10.1.3 Reset Domains

Different reset types reset different domains.

- Regulator Power-on reset (POR) and External CHIP_EN reset (EXT_POR) can reset the whole chip.
- System reset is triggered by software.
- A watchdog reset is generated when watchdog timeout. Watchdog reset can reset most of the system.
- A thermal reset is generated when abnormal temperature detected. Thermal reset can reset the system and IWDG of AON domain.

3.10.2 Clock Control

The clock sources of RTL8730E are listed below. Different clock sources can drive different functions.

- One external oscillator:
  - XTAL40M: used for peripherals directly or after frequency division.
- Three internal oscillators:
  - OSC4M: provides 4MHz clock for KM0 CPU, or 2MHz clock for peripherals after frequency division.
  - OSC131K: used for input of SDM and other peripherals.
  - OSC100K: resides in the AON domain and used to drive the IWDG and OTPC.
- Six separate PLLs: each of them can be configured with integer or fractional ratios.
  - AP PLL: 1.2GHz, provides clock for CA32 CPU.
  - NP PLL: 920MHz/1GHz, provides clock for KM4 CPU, and for peripherals after frequency division.
  - Two Audio PLLs dedicated to Audio subsystem, can be enabled or disabled by software.
    - PLL1: 90.304MHz
    - PLL2: 45.1584MHz
  - One PLL dedicated for Wi-Fi: 320MHz
  - One PLL dedicated for DDR: 533MHz
- USB PHY: 480MHz, dedicated to USB
- MIPI PHY: 80MHz ~ 1GHz, dedicated to MIPI

3.11 General Direct Memory Access (GDMA)

The RTL8730E has a GDMA, which allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory transactions without the participation of CPU. Each DMA stream provides unidirectional DMA transfers for a single source and destination. It features:

- Up to eight independent channels with programmable priority
- FIFO per channel for source and destination
- Programmable flow control at block transfer level (source, destination or DMAC)
- Transaction: supports single and burst transaction mode
- DMA transfer: supports single-block and multi-block transfer
- Secure transfer mode

3.12 Audio

The audio module is divided into four parts: VAD, Audio ADC, Audio DAC and I2S. The functions of the four parts are described below.

3.12.1 Built-in VAD

The Voice Activity Detection (VAD) is to accurately locate the beginning and end of the actual audio from the original data with noise, which is to remove the mute and noise as interference signals from original data. It features:

- Support MIC data from Analog MIC or PDM digital MIC
- Support single MIC human voice detection
- Support Multi-MIC array data store before/after voice detection event
- Work in 16kHz

3.12.2 Audio ADC

- Built-in five channels audio ADC
- Support vary sampling rate from 8kHz to 96kHz
- SNR > 98dB A-weighted and THD+N < -80dB
- Support differential microphone input and can also be configured as single-ended
- Support programmable input analog gains
- Support five programmable microphone bias. The maximum programmable voltage can reach 1.8V.
- Support zero-crossing detection
- Digital volume control
- DC remove function
- Configurable 0~5 band equalizer (EQ)
- Support up to 8 channels DMIC interface

3.12.3 Audio DAC

- Built-in stereo audio DAC with earphone driver or line-out
- Support vary sampling rate from 8kHz to 192kHz
- SNR > 98dB, THD+N < -85dB (AVDD=1.8V, load=10kΩ, dual differential output)
- Dual differential output or single-ended output
- De-pop function in stereo headphone amplifiers
- -80dB crosstalk between channels
- Digital volume control, zero-crossing detection
- DC remove function
- PDM interface function for external speaker AMP
- 10-band flexible EQ

3.12.4 Inter-IC Sound (I2S)

The Audio module integrates two I2S interfaces.

- Support I2S normal, left-justified mode, etc.
- Support up to 8-channel I2S transmitter and receiver by TDM or PCM mode
- Audio data word length: 16/20/24/32 bits
- Channel length: 16/20/24/32 bits
- Work in master and slave mode
- In 2 channels mode, fs supports up to 192kHz.

3.13 Inter-Processor Communication (IPC)

The inter-processor communication (IPC) hardware is designed to make any two CPUs communicate with each other. The IPC provides a set of registers for each processor that facilitates inter-processor communication via interrupts. Interrupts may be independently masked by each processor to allow polled-mode operation.

The IPC communication data must be located in a common memory, which is not part of the IPC block. It features:

- Status signaling for the 32 channels (16 channels for Tx and 16 channels for Rx)
  - Channel empty/full flag, also used as a lock
- Four sets interrupt lines per processor
  - Two sets for Rx channel full (communication data posted by sending processors)
  - Two sets for Tx channel empty (communication data retrieved by receiving processors)
- Interrupt masking per channel
  - Channel Tx empty mask
  - Channel Rx full mask

3.14 General-Purpose Input/Outputs (GPIOs)

The RTL8730E provides GPIO ports with a total of up to 72 GPIO pins. All GPIOs are located in LS platform.

The GPIO supports the following features:

- Clock source:
  - 10MHz
  - SDM32kHz
- Separate data register and data direction register for each signal
- Read back the data on external pads using memory-mapped registers.
- Independently controllable signal by bits
- Interrupt mode for each pin
  - Level sensitive: active-high level or active-low level interrupt
  - Edge trigger: rising edge, falling edge or both edges
- Option to generate single or multiple interrupts
- Configurable de-bounce time up to 8ms to de-bounce interrupts
- Level interrupt synchronization

Each of the GPIO pins can be dynamically configured by software as output or input. GPIO pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Most of the GPIO pins are shared with digital or analog alternate functions.

3.15 Inter-integrated Circuit Interface (I2C)

The RTL8730E embeds three I2C interfaces (I2C0, I2C1, I2C2).

The I2C bus interface handles communications between the RTL8730E and the serial I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing. The design of I2C aims at sensor-hub application in low-power or battery-powered productions. Essential features of I2C bus protocol should be provided for acquiring or controlling external sensor data.

The I2C peripheral supports:

- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three speed modes
  - Standard Speed, up to 100kbps
  - Fast Speed, up to 400kbps
  - High Speed, up to 3.4Mbps
- I2C interfaces: 3
  - I2C0 on LS platform (LS_APB_CLK, 10MHz), only supports Standard Speed and Fast Speed modes.
  - I2C1 and I2C2 on HP platform (HP_AHB_CLK, 100MHz), support all speed modes.
- Master or Slave I2C operation
- Transmitter or Receiver
- Transmit and receive buffers with depth of 16
- Multi-master ability including bus arbitration scheme
- Clock stretch in master/slave mode
- 7-bit or 10-bit addressing mode, 7-bit or 10-bit combined format transfer
- Manual START/RESTART/STOP bit control
- Support General Call, NULL DATA, START BYTE transfer protocol
- Component parameters for configurable software driver support (programmable SDA hold time, slave address, SCL duty cycle, etc.)
- Filter to eliminate the glitches on signals of SDA and SCL, programmable digital noise filter
- Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)
- Slave Mode Dual Own Address
  - Slave 1 supports 7-bit or 10-bit address mode
  - Slave 2 only supports 7-bit address mode
- Operation mode
  - Polling mode
  - Interrupt mode

3.16 Universal Asynchronous Receiver/Transmitter (UART, LOGUART)

3.16.1 UART0 ~ UART2

The RTL8730E has embedded three general UART interfaces (UART0, UART1, UART2).

The UART offers a flexible means of full-duplex data exchange with external equipment, requiring an industry-standard NRZ asynchronous serial data format. It provides a very wide range of baud rates using a fractional baud rate generator. Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

The UART supports the following features:

- All UARTs locate in HP platform (HP_APB_CLK) with clock source XTAL40MHz or OSC2MHz
- Various UART formats: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Fractional baud rate
  - Up to 8Mbps within high-speed mode (40MHz)
  - 115.2kbps within low-power mode (2MHz)
- Separated clocks for Tx path and Rx path
  - Tx path: XTAL 40MHz
  - Rx path: XTAL 40MHz, XTAL 2MHz, OSC 2MHz
- 11 bits * 16 asynchronous Transmit/Receive FIFO
- Hardware Interface auto-flow control
- Interrupt control and error detection
- IrDA (SIR mode) encoder and decoder module
- Loop-back mode for self-test
- Low power mode for Rx path

- Monitor and elimination of Rx baud rate error and own frequency drift automatically for Rx path
- UART Rx timeout mechanism
- DMA interface for DMA transfer
  - DMA as DMA TRx flow controller
  - UART as DMA Rx flow controller
- Operation mode
  - Polling mode
  - Interrupt mode

3.16.2 LOGUART

The RTL8730E has one LOGUART.

The LOGUART is responsible for printing logs. It can print logs from five sources at the same time without disordered logs, also it can receive commands for CPU to process.

The LOGUART supports:
- Clock source: XTAL40M, OSC2M and XTAL2M
- Follow UART protocol
- Various UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Up to 3Mbps baud rate for fast log printing
- Fractional baud rate
- Monitor function to eliminate Rx baud rate error and own frequency drift automatically for Rx path
- Five Tx ports for multi-core or multi-function to print log, which are KM0 CPU, KM4 CPU, CA32 CPU, Bluetooth and Bluetooth firmware
- Supports UART relay function, Bluetooth firmware log of UART protocol from other SoC can be relayed by this IP to print out through one Tx port
- Hardware arbitration for Tx ports so that all Tx ports can print log concurrently without disordered log
- Independent open and close for five Tx ports
- Tx AGG supported, hardware adds AGG header automatically so that console can separate logs from different Tx ports
- Wake up the system when clock source is open during sleep mode.

3.17 Serial Peripheral Interface (SPI)

The RTL8730E features two SPIs (SPI0, SPI1) that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex and simplex modes. All SPI interfaces support hardware CRC calculation and 64x16-bit embedded Rx and Tx FIFOs with DMA capability.

The SPI has the following features:
- Both SPI0 and SPI1 locate in HP platform (HP_AHB_CLK) with 100MHz
- Two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps
- Master and slave operation mode
- DMA interface for DMA transfer
- Independent masking of interrupts
- The Transmit and Receive FIFOs are 64 words in depth, and the width is fixed at 16 bits.
- Hardware/Software slave-select
  - Dedicated hardware slave-select lines
  - Software control to select target serial-slave device
- Programmable features
  - Clock bit-rate – Dynamic control of the serial bit rate of the data transfer, only when configured in Master Mode.
  - Data frame size (4 to 16 bits) – Frame size of each data transfer under the control of the programmer.
  - Configurable clock polarity and phase
  - Programmable delay sample time of the received serial data bit (rxd), when configured in Master Mode
- Transfer mode
  - Transmit and receive
  - Transmit only
  - Receive only
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

3.18 Universal Serial Bus (USB) Interface

The USB of RTL8730E supports communication between a host and a device. It is fully compliant with USB 2.0 specifications. The USB of RTL8730E can operate as USB host, USB device and USB OTG.

3.18.1 USB Host

The USB host enables data exchange with USB device attached to the bus. It supports high speed, full speed and low speed. All transactions are initiated by the host controller. USB host sends commands and sends/receives setup packets through message pipe, and it transmits data through stream pipe. Also, USB host does not support hub-insert detection.

It has the following features:

- Software configurable to OTG1.3 mode of operation
- Support three speed modes:
  - High-Speed (HS, 480Mbps) mode
  - Full-Speed (FS, 12Mbps) mode
  - Low-Speed (LS, 1.5Mbps) mode
- Support internal DMA mode and non-DMA mode
- Support up to 8 host channels
- Support up to 1016 data FIFO depth
- Includes automatic ping capabilities
- Support the keep-alive in Low-Speed mode and SOFs in High-/Full-Speed modes
- Use UTMI 16-bit MAC-PHY interface
- Support dynamic FIFO sizing, software can configure periodic and non-periodic host Tx FIFO size and host Rx FIFO size flexibly.

3.18.2 USB Device

The USB device enables data exchange with a USB host. It supports high speed and full speed. USB device allows customization of descriptors via software configuration. USB device has a bidirectional control endpoint, it can receive host commands and send/receive USB data. Also, it supports multiple IN and OUT endpoints.

It has the following features:

- Software configurable to OTG1.3 mode of operation
- Support two speed modes:
  - High-Speed (HS, 480Mbps) mode
  - Full-Speed (FS, 12Mbps) mode
- Support internal DMA mode and non-DMA mode
- Support up to 6 endpoints, including two bidirectional endpoints for endpoint 0 (dedicated for control transfer) and endpoint 5, two IN endpoints for endpoint1 and endpoint3, two OUT endpoints for endpoint2 and endpoint4
- Support one Device Mode Periodic IN endpoint among the 6 endpoints
- Support dynamic FIFO sizing, software can configure periodic and device non-periodic Tx FIFO size and device Rx FIFO size flexibly with total data FIFO depth 1016.

3.18.3 USB OTG

The USB OTG integrates the host and device controller. USB OTG is a 5-wire bus that supports dynamic host-peripheral switch of role. Host or peripheral (the default) role is assumed depending on the ID input pin. The ID line status is determined by plugging in the USB, depending on which side of the USB cable is connected to the micro-AB receptacle.

It has the following features:

- Software configurable to OTG1.3 mode of operation
- Support two speed modes:
  - High-Speed (HS, 480Mbps) mode
  - Full-Speed (FS, 12Mbps) mode
- Support internal DMA mode and non-DMA mode
- Support Session Request Protocol (SRP)
- Support Host Negotiation Protocol (HNP)

3.19 Serial Data (SD) Host Controller

The Serial data (SD) host controller is responsible for accessing SD memory card and eMMC device. It features:

- Compliance with SD memory card specifications version 2.0 and Multi-Media Card (MMC) system specification version 4.5.
- SD
  - 1-bit and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
  - Card detect with debounce function
- eMMC
  - 1-bit and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
- Internal DMA supported
- 3.3V operating voltage
- For eMMC, 1.8V is supported.

NOTE

If the eMMC device powered by 1.8V is used to transmit data, an independent 1.8V power supply is needed to ensure sufficient power for eMMC chip. Refer to the datasheet of eMMC chip for specific power design specification.

3.20 Light Emitting Diode Controller (LEDC)

The RTL8730E embeds a LEDC. LEDC is used to control external LED lamps, a common light-emitting device. It can efficiently convert electrical energy into light energy, which has a wide range of applications in modern society.

The LEDC supports the following features:

- Clock source: XTAL40MHz
- Configurable LED output high/low level time from 0 to 6.4us
- Configurable LED refresh time period up to 400us
- DMA interface with LEDC as DMA flow controller
- Configurable RGB888 display mode
- Maximum 1024 LED serial connection
- Transmit FIFO is 32*24bits
- Configurable IDLE state output level
- Operation mode
  - DMA mode
  - Interrupt mode

3.21 Liquid Crystal Display Controller (LCDC)

The LCD-TFT (Liquid Crystal Display-Thin Film Transistor) display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to internal VO interface, which is only used by MIPI Display Serial Interface directly to a broad range of LCD and TFT panels up to XGA (1024×768) @60 fps resolution with the following features:

- 3 display layers with dedicated FIFO 256×32 bits
- Up to 7 input color formats selectable per layer
- Color keying (transparency color)
- Flexible programmable parameters for each layer
- Flexible blending between layers using alpha value (per pixel or constant)
- Programmable background-color
- AXI master interface @200MHz

NOTE

The LCDC is dedicated to MIPI and there is not any pin out, so users cannot use it directly.

3.22 MIPI Display Serial Interface (MIPI-DSI)

The Display Serial Interface (DSI) standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards. The MIPI DSI Host Controller provides an interface between the system and the MIPI D-PHY, allowing communication with a DSI-compliant display.

The MIPI-DSI has the following features:

- 1 clock and 1 or 2 data lane pairs
- Support up to two D-PHY Data Lanes and max. bit rate of 1Gbps per lane
- Bidirectional Communication and Escape Mode support through Data Lane 0
- Ultra-low-power mode
- End of Transmission Packet (EoTp)
- ECC and checksum capabilities
- Video mode with dedicated FIFO 480×64 bits
- Command mode with dedicated FIFO 480×64 bits

3.23 Infrared Radiation (IR)

The RTL8730E embeds an infrared radiation (IR).

The IR is mainly designed to process IR signals with carrier frequency under 500kHz. The hardware IP supports hardware modulation which can be used on the IR Tx transmission. It also can detect the period of a continuous high/low level signal, and record in Rx FIFO, and then the software can recognize a received IR signal serial and process it. IR module works in Half-duplex mode.

It supports the following features:
- Clock source: 100MHz
- Half-duplex mode
  - Tx mode: carrier frequency range is from 25kHz to 500KHz
  - Rx mode: maximum sample frequency is 100MHz
- 32*4 bytes FIFO depth
  - Tx FIFO: Tx carrier symbol count and Tx data state
  - Rx FIFO: Rx data Level and Rx data count
- Customizable carrier duty by users
- Tx Compensation Mechanism
- Optional to modulate space symbol to carrier symbol
- IR receiver front can be IR receiver module or IR diode
- IR Rx glitch filter from 10ns to 90ns
- Operation mode:
  - Interrupt mode
  - Polling mode

3.24 General Analog-to-digital Converter (ADC)

The RTL8730E integrates a 12-bit successive-approximation register (SAR) ADC, which provides a solution for collecting analog sensor and system power-consumption data with a low-power requirement. Various operation modes, for instance, auto mode, timer-trigger mode, and software-trigger mode, are adopted according to different using strategies.

It has the following features:
- Resolution: 12-bit SAR
- Single-ended input
- Available channel number
  - 6 external channels and 1 BAT_MEAS channel
  - 2 internal channels
- Built-in calibration
- Wide input voltage range: 0 ~ 1.8V
- Configurable ADC clock source
- Configurable channel switch order and channel number
- Individual channel compare mode
- Multi-sampling trigger sources
  - Software
  - Timer
- Manual and auto mode conversion
  - Manual mode for software-controllable conversion
  - Auto mode for hardware continuous conversion

3.25 Thermal Sensor

The RTL8730E has integrated a thermal sensor, which can be used to detect and monitor the real-time temperature inside the chip. It has the following features:

- Measurement range: -40°C ~ 125°C
- Variation: ±1°C (typical), ±3°C (worst)
- Provides low- temperature warning, high-temperature warning and over-temperature protection
- Provides thermal enable and over-temperature protection enable write access control

The temperature protection mechanism is an important feature provided by the thermal sensor, and is implemented as follows:

- When the temperature exceeds the limit high-temperature threshold, an interrupt is sent to the CPU, and the CPU will reduce the frequency and speed.
- When the temperature exceeds the limit low-temperature threshold, an interrupt is sent to the CPU, and the CPU will increase the frequency and speed.
- When the temperature exceeds the limit over-temperature protection threshold, the hardware will be powered down automatically for over-temperature protection.

By default, Realtek's SDK does not automatically adjust the CPU frequency and speed based on the temperature detected by thermal meter. If users need to use this function, please call the thermal related APIs to configure the temperature threshold according to the actual application and heat dissipation conditions.

3.26 Cap-Touch Controller (CTC)

Self-capacitance touch controller measures the capacitance between the capacitive sensor pin and ground. The capacitive touch controller detects the presence of a finger through capacitance changes.

It has the following features:

- 9 capacitive sensor channels:
  - Detection of finger touch
  - Programmable enable/disable for each channel
  - Adjustable sensitivity for each channel
  - Adjustable touch threshold for each channel
- Automatic channel scan: hardware scans each enabled channel automatically in sequence
- Programmable scan period: sample number and scan interval
- Active noise immunity:
  - Supports SNR information monitor
  - Adjustable environmental noise threshold for each channel
- Automatic environment tracking and calibration (ETC)
  - Automatic hardware baseline initialization
  - Automatic baseline and threshold update for different noise environments
  - Programmable ETC update step and factor
- Programmable button debounce function
- Interrupt control
  - Programmable interrupt enabled for each interrupt source
  - Software readable interrupt status and raw status register

4 Electrical Characteristics

4.1 Parameters Definitions

4.1.1 Maximum and Minimum Values

Unless otherwise specified, all data are guaranteed by design, simulation and samples test to be applicable to all declared temperature, voltage ranges and processes, but and are not tested in production.

4.1.2 Typical Values

Unless otherwise specified, the typical values are reference results when the IC is at an ambient temperature of 25°C and an operating voltage of 3.3V. This value is for reference design only and not actually tested.

4.1.3 Pin Status

4.1.3.1 Loading Capacitor

Unless otherwise specified, the load refers to the equivalent capacitance mounted on the chip pin. Schematic diagrams used for loading capacitor measurements is illustrated in *Figure 4-1*.

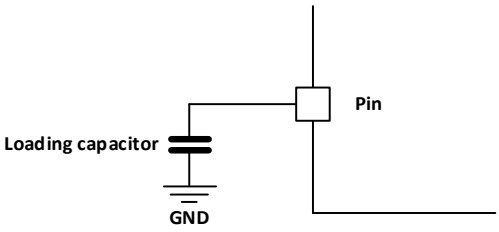


Figure 4-1 Loading capacitor diagram of pin

4.1.3.2 Input Voltage

Unless otherwise specified, the input voltage of the chip pin refers to the voltage difference between the pin and ground. The schematic diagram is illustrated in *Figure 4-2*.

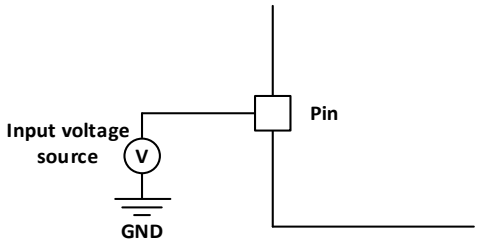


Figure 4-2 Input voltage diagram of pin

4.2 Absolute Maximum Ratings

Stresses beyond absolute maximum ratings may cause permanent damage to the device. These are emphasized ratings only and do not imply functional operation of the device.

Table 4-1 Absolute maximum ratings

Symbol	Parameter	Condition	Min.	Max.	Unit
VAH_DCDC_CORE, VDH_IO0, VDH_IO1, VAH_PLL, VRH_SYN, VAH_XTAL, VRH_PAD_A, VRH_PA_A, VRH_PAD_G, VRH_PA_G, VRH_FE_BT, VRH_PA_BT, VDH_IO2, VDH_IO3, VDH_IO4, VDH_IO5, VDH_IO6, VAH_DCDC_MEM, VAH_DCDC_AUD, VAH_USB	The voltage difference between the power pin and GND	Input voltage at power pin	-0.3	3.63	V
VBUS_OTG	The voltage difference between the power pin and GND	Input voltage at VBUS_OTG pin		5.5	V
BAT_MEAS	The voltage difference between the BAT_MES pin and GND	Input voltage at BAT_MEAS pin	TBD	6.4	V
V_{IN}	The difference between the input voltage on the PAx/PBx/PCx pins and GND	Input DC voltage at digital I/O pin, VDH_IOx≤3.63V	-0.3	VDH_IOx+0.3	V
	The difference between the input voltage on the MICx/LINEx pins and GND	Input DC voltage at analog pin, VAM_AUD≤1.98V	-0.3	VAM_AUD+0.3	
P_ANT	Maximum power at receiver	Input RF power at antenna pin		0	dBm
T_{STORE}	Storage temperature		-65	+150	°C
MSL	Moisture Sensitivity Level			MSL3	
HBM	ESD Human Body Model	T_A=25°C, conforming to JESD22-A114F		Class 2	
CDM	ESD Charged Device Model	T_A=25°C, conforming to JESD22-C101F		Class C2	

4.3 Operation Conditions

Table 4-2 Recommended operation conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
VAH_DCDC_CORE, VDH_IO0, VAH_PLL, VRH_SYN, VAH_XTAL, VRH_PAD_A, VRH_PA_A, VRH_PAD_G, VRH_PA_G, VRH_FE_BT, VRH_PA_BT, VDH_IO2, VDH_IO3, VDH_IO4, VDH_IO5, VAH_DCDC_MEM, VAH_DCDC_AUD, VAH_USB[1]	Power pin voltage		2.97	3.3	3.63	V
VDH_IO1, VDH_IO6	Power pin voltage (3.3V)		2.97	3.3	3.63	V
	Power pin voltage (1.8V)		1.71	1.8	1.98	V
VBUS_OTG	Power pin voltage		4.75	5	5.25	V
VAM_AFE, VRM_SYN, VRM_RF, VRM_FE_BT, VAM_AUD	Power pin voltage		1.71	1.8	1.98	V
VDL_CORE, VDL_MEM, VAL_USB, VAL_MIPI	Power pin voltage	SoC in burst mode[2]	0.95	1.0	1.05	V
		SoC in normal mode[2]	0.855	0.9	0.945	V
		SoC in sleep mode	0.72	0.8	0.88	V
VDM_MEM	Power pin voltage	Embedded DDR3L memory type	1.283	1.35	1.45	V
		Embedded DDR2 or PSRAM memory type	1.7	1.8	1.9	V
T_A	Ambient operating temperature		-40	-	+105	°C
T_J max.	Maximum Junction temperature[3][4]		-	-	+125	°C

CAUTION

[1] All these power pins must be powered by the same voltage. For IC's stable performance, the voltage ripple on these pins is suggested to be under +/-100mV.

[2] The normal mode and burst mode are subdivisions of active mode, while the burst mode has a higher core power and operation frequency.

[3] The junction temperature must not exceed T_J max. in all T_A ranges. When T_A is high and the power consumption of device is also high, a well-designed thermal management should be implemented to the board system to guarantee proper T_J. Refer to Section Thermal Characteristics to estimate T_J.

[4] The IC must not operate at junction temperature of 125°C for extended periods of time.

4.4 Power Sequence

The recommended power-on and power-off sequences are depicted in the following sections. The VDH_*x*/VAH_*x*/VRH_*x* and CHIP_EN are powered and controlled by external power sources. Other used voltages are recommended to be powered by the embedded regulator or LDO.

NOTE

The VDH_x/VAH_x/VRH_x refers to typical 3.3V power supply including VAH_DCDC_CORE, VDH_IO0, VAH_PLL, VRH_SYN, VAH_XTAL, VRH_PAD_A, VRH_PA_A, VRH_PAD_G, VRH_PA_G, VRH_FE_BT, VRH_PA_BT, VDH_IO2, VDH_IO3, VDH_IO4, VAH_DCDC_MEM, VAH_USB, VDH_IO5 and VAH_DCDC_AUD. The VDH_IO1 and VDH_IO6 can be powered by typical 3.3V or 1.8V, and should be stable before the corresponding GPIOs normal operation.

The parameter specification of power sequence is listed in *Table 4-3*.

Table 4-3 Power sequence specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{NORMAL}	VDH_*x*/VAH_*x*/VRH_*x* normal operation voltage	2.97	3.3	3.63	V
V_{POR_H}	Power on reset high level	1.9	2.1	2.7	V
V_{POR_L}	Power on reset low level	0.5			V
V_{IL}	CHIP_EN input low voltage	0	0	0.8	V
V_{IH}	CHIP_EN input high voltage	2.0	3.3	3.63	V
T_0	VDH_*x*/VAH_*x*/VRH_*x* rising time	0.05			ms
T_1	VDH_*x*/VAH_*x*/VRH_*x* ready time			4.2	ms
T_2	VDH_*x*/VAH_*x*/VRH_*x* falling time	0.05			ms
T_{CORE}	Core power on time		6[1]		ms
T_{TM}	Test mode trap time	0		5	ms
T_{UD}	UART download mode trap time	0		5	ms
T_{BS}[2]	Boot selection from NOR or NAND Flash trap time	0		5	ms
T_3	VDH_*x*/VAH_*x*/VRH_*x* low voltage last time	0.3			ms
Debounce time	CHIP_EN debounce time, set by registers				
T_4	CHIP_EN low voltage last time	0.1			ms

NOTE

[1] T_{CORE} is characterized under 3.3V power supply and 25°C.

[2] T_{BS} is only valid for RTL8730EAM and RTL8730ELM series which need external Flashes.

4.4.1 Power-on Sequence

During power on, the VDH_*x*/VAH_*x*/VRH_*x* needs to rise monotonously. When the VDH_*x*/VAH_*x*/VRH_*x* is over V_{POR_H} and CHIP_EN is high, the chip releases internal reset, and the VDH_*x*/VAH_*x*/VRH_*x* needs to rise up to V_{NORMAL} within T_1. There is no restriction that CHIP_EN is pulled up earlier or later than VDH_*x*/VAH_*x*/VRH_*x* or at the same time with VDH_*x*/VAH_*x*/VRH_*x*.

- T_{CORE} after IC release internal reset, embedded DCDC and LDO will start to output core power for VDL_CORE.
- T_{TM} after IC release internal reset, the IC will get the state of PB22/TM_DIS.
  - When the state of PB22/TM_DIS is high, the IC will enter normal mode.
  - When the state of PB22/TM_DIS is low, the IC will enter test mode.
- T_{UD} after IC release internal reset, the IC will get the state of PB24/UD_DIS.
  - When the state of PB24/UD_DIS is high, the IC will enter normal boot mode.
  - When the state of PB5/UD_DIS is low, the IC will enter UART download mode.
- T_{BS} after IC release internal reset, the IC will get the state of PB21/BOOT_SEL. PB21/BOOT_SEL is only valid for RTL8730EAM and RTL8730ELM series which need external Flashes.
  - When the state of PB21/BOOT_SEL is high, it indicates that the external Flash type is NOR Flash.
  - When the state of PB21/BOOT_SEL is low, it indicates that the external Flash type is NAND Flash.

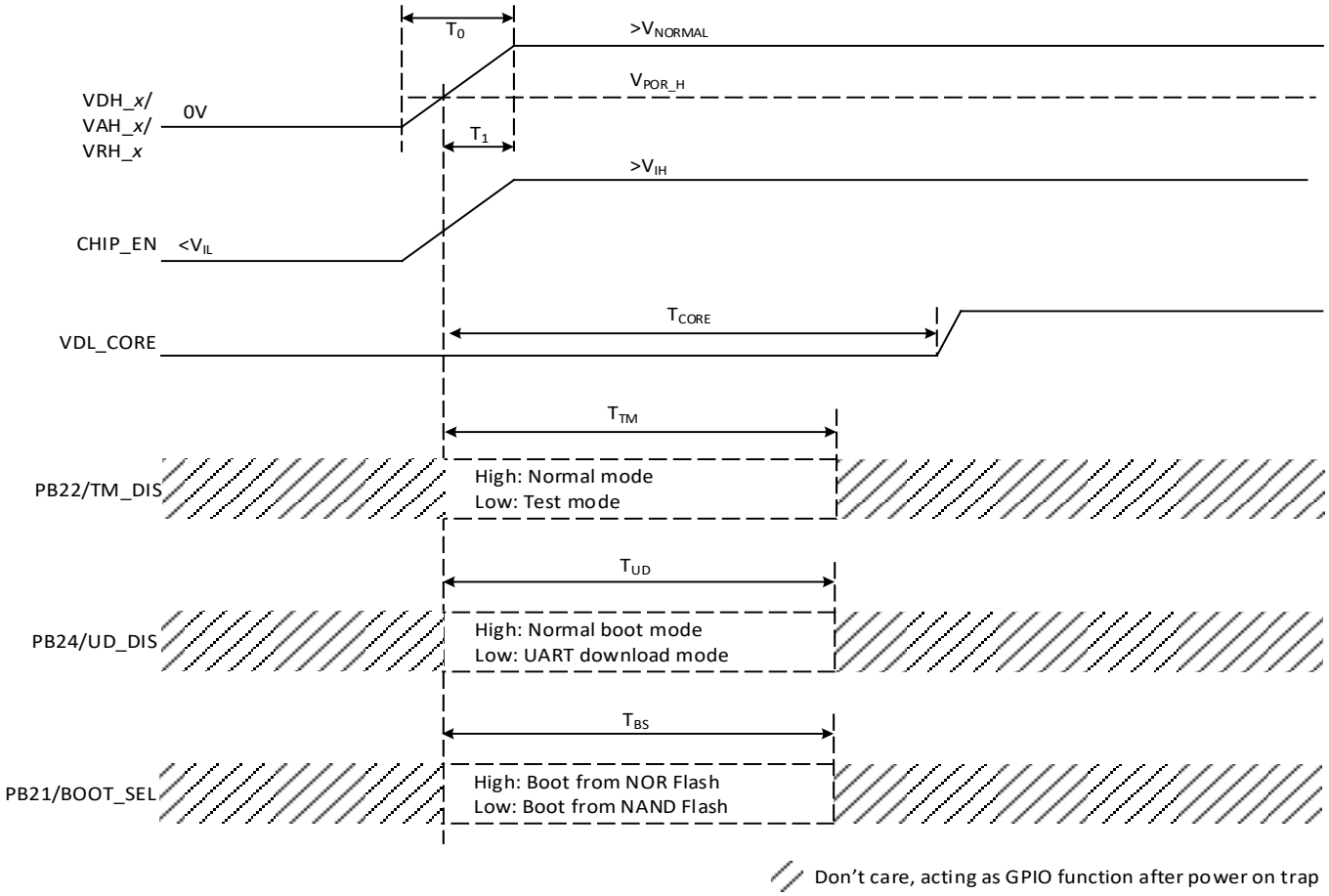


Figure 4-3 Power-on sequence

4.4.2 Power-off Sequence

In the process of power-off, the VDH_*x*/VAH_*x*/VRH_*x* needs to drop down below V_{POR_L} and lasts for at least T_3 before it can be boosted and the IC can be powered on again. Any voltage between V_{NORMAL} and V_{POR_L} may not trigger a reset, and it may cause the chip to work abnormally.

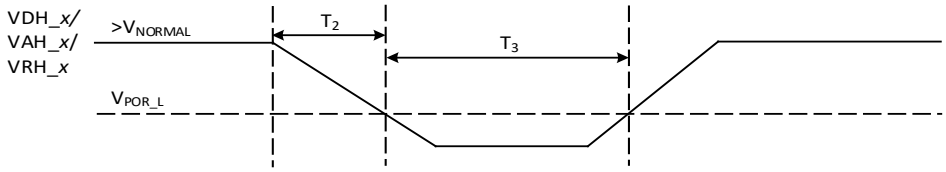


Figure 4-4 Power-off sequence

4.4.3 CHIP_EN Reset Sequence

When using the CHIP_EN as normal reset function, you can set the expected debounce time, ranging from 0us to 16ms. This time may have max. ±50% variation under different conditions, such as different voltage, temperature, etc. When reset, the pull down time must be T_4 more than debounce time, and the variation of debounce time needs to be taken into consideration.

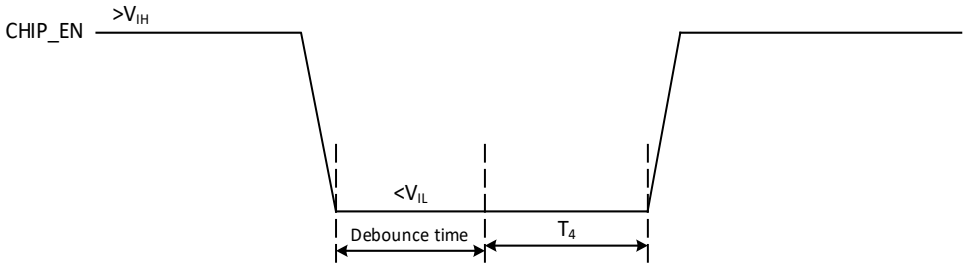


Figure 4-5 CHIP_EN reset sequence

4.5 Reset Detection

The parameters given in *Table 4-4* are derived from test under ambient operating temperature.

Table 4-4 Embedded power supply supervisor characteristics

Symbol	Parameter	Configuration	Min.	Typ.	Max.	Unit
V_{BOD_L}	Brownout detect falling threshold	BOD_THRESHOLD10		2.90		V
		BOD_THRESHOLD11		2.86		V
		BOD_THRESHOLD12		2.81		V
		BOD_THRESHOLD13		2.76		V
		BOD_THRESHOLD14		2.72		V
		BOD_THRESHOLD15		2.67		V
		BOD_THRESHOLD16		2.63		V
V_{BOD_H}	Brownout detect rising threshold	BOD_THRESHOLD8		2.98		V
		BOD_THRESHOLD9		2.92		V
		BOD_THRESHOLD10		2.87		V
		BOD_THRESHOLD11		2.83		V
		BOD_THRESHOLD12		2.78		V
		BOD_THRESHOLD13		2.74		V
		BOD_THRESHOLD14		2.69		V

NOTE

V_{BOD_L} and V_{BOD_H} can be set independently. V_{BOD_H} needs to be set higher than V_{BOD_L}. It is recommended to reserve about 200mV or higher hysteresis window between V_{BOD_H} and V_{BOD_L}.

4.6 Embedded Regulators Characteristics

The characteristics of embedded regulators including DCDC_CORE, DCDC_MEM and DCDC_AUD are guaranteed by design.

Table 4-5 Embedded regulators characteristics

Regulators	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DCDC_CORE	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		0.72	0.8/0.9/1.0	1.05	V
	I_{LOAD}	Load current[1]	PWM mode			540	mA
	F	Switching frequency	PWM mode		2		MHz
DCDC_MEM	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		1.283	1.35/1.8	1.98	V
	I_{LOAD}	Load current[1]	PWM mode			500	mA
	F	Switching frequency	PWM mode		2		MHz
DCDC_AUD	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		1.62	1.8	1.98	V
	I_{LOAD}	Load curren[1]	PWM mode			250	mA
	F	Switching frequency	PWM mode		2		MHz

NOTE

[1] No additional external load is accepted unless mentioned.

4.7 Crystal Characteristics

The RTL8730E has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned. The characteristic requirements of external crystal are listed in *Table 4-6*.

Table 4-6 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

4.8 I/O Pin Characteristics

This section applies when a GPIO is used as a digital function, but not when it is used as an analog function.

Table 4-7 Digital I/O pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	V_{IO}[1]=1.8V±10%	-0.3	-	0.35 * V_{IO}	V
		V_{IO}=3.3V±10%	-0.3	-	0.8	
V_{IH}	I/O input high level voltage	V_{IO}=1.8V±10%	0.65 * V_{IO}	-	-	
		V_{IO}=3.3V±10%	2	-	-	
V_{OL}[2]	I/O output low level voltage	V_{IO}=1.8V±10%, I_{OL} Max.[2]	-	-	0.15 * V_{IO}	
		V_{IO}=3.3V±10%, I_{OL} Max.	-	-	0.15 * V_{IO}	
V_{OH}[2]	I/O output high level voltage	V_{IO}=1.8V±10%, I_{OH} Max.	0.85 * V_{IO}	-	-	
		V_{IO}=3.3V±10%, I_{OH} Max.	0.85 * V_{IO}	-	-	

NOTE

[1] V_{IO} is the power supply for I/O pin.
[2] Refer to Table 4-8 for driving strength.

All I/Os are listed in *Table 4-8*.

Table 4-8 I/O types

Pin name	I/O power pin	Driving (mA)[1]		Internal pull resistor (kΩ)[2]			Resistor available in deep-sleep mode[3]?
		1.8V (±10%)	3.3V (±10%)	Min.	Typ.	Max.	
PA0~PA8[4]	VDH_IO0	-	4/8	40	80	120	√
PA9~PA16[5]	VDH_IO1	4/8	8/16	2.3/5	4.7/10	7.1/15	√
PA17[5]	VDH_IO1	2/4	4/8	40	80	120	√
PA18~PB6[6]	VAM_AUD	1/3	-	PU: 185 PD: 52	PU:3 00 PD: 100	PU: 431 PD: 165	x
PB7~PB9[4]	VDH_IO2	-	4/8	40	80	120	√
PB10~PB13[4]	VDH_IO2	-	8/16	2.3/5	4.7/10	7.1/15	√
PB14~PB20	VDH_IO3	-	4/8	40	80	120	√
PB21~PB22[4]	VDH_IO3/VDH_IO4[7]	-	8/16	2.3/40	4.7/80	7.1/120	√
PB23~PB24[4]	VDH_IO3/VDH_IO4[7]	-	8/16	40	80	120	√
PB25~PC0[5]	VDH_IO6	2/4/8/10/12	4/8/16/20/24	12.5/25	25/50	37.5/75	√
PC1~PC7[4]	VDH_IO5	-	8/16	40	80	120	√

NOTE

[1] The I/O powers supported by different I/Os are different, and the driving capability is related to the I/O powers. Refer to Table 4-7 for VOH and VOL. Different drive capabilities can be controlled by registers. For example, 4/8 refers to the driving capability of 4mA or 8mA, which can be adjusted through registers.
[2] Except for PA18~PB6, the pull-up and pull-down values of other I/Os are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The range is ±50%. Different resistor can be controlled by registers. For example, 4.7/10 refers to the internal pull resistor of 4.7kΩ or 10kΩ, which can be adjusted through registers.
[3] In deep-sleep mode, PA18~PB6 are in FLOATING state, and the internal resistors of these pins are NOT available. If the circuit

connected with these GPIOs needs to be pulled high or low state, external resistor on PCB is needed. In other mode except deep-sleep, internal resistors of all GPIOs are available.

[4] The pins of this group only support 3.3V I/O power.

[5] The pins of this group support 1.8V/3.3V I/O power.

[6] The pins of this group only support 1.8V I/O power.

[7] The I/O power pin of RTL8730ELH is VDH_IO4, and the I/O power pin of RTL8730EAH is VDH_IO3.

4.9 Power Consumption Characteristics

For the current data provided in the following sections, the typical current is the average current of multiple typical process chips, and the maximum current is the worst case caused by process deviations. The power consumption of chip is affected by voltage, temperature and process deviations.

The power consumption data given in the following sections is the result of the IC powered by 3.3V and different ambient temperatures.

4.9.1 Power-Saving Mode Power Consumption

The MCU is under the following working conditions:

- Except for UART_LOG TXD/RXD (PB24/PB23), other I/O pins are in input mode.
- All peripherals except GPIO are disabled.

Table 4-9 Power-saving mode

Operating mode	KM0 mode	KM4 mode	CA32 mode	SWR_AUD mode	SWR_MEM mode	Wi-Fi & BT state	SRAM state
Sleep mode 1	CG[1]	CG	CG	OFF	PFM	OFF	Retention
Sleep mode 2	PG[2]	PG	PG	OFF	PFM	OFF	Retention
Deep-sleep mode[3]	OFF	OFF	OFF	OFF	OFF	OFF	Shut down

NOTE

[1] CG: Clock Gating

[2] PG: Power Gating

[3] In deep-sleep mode, only some circuits in the AON domain are still working.

4.9.1.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (LP1)	Sleep mode 1	1.72	14.2	mA
I_{VDD} (LP2)	Sleep mode 2	0.345	3.09	mA
I_{VDD} (LP3)	Deep-sleep mode	23.1	194	µA

4.9.1.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (LP1)	Sleep mode 1	3.51	19.7	mA
I_{VDD} (LP2)	Sleep mode 2	1.77	5.7	mA
I_{VDD} (LP3)	Deep-sleep mode	27.6	239	µA

4.9.1.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (LP1)	Sleep mode 1	3.11	16.4	mA
I_{VDD} (LP2)	Sleep mode 2	1.86	5.25	mA
I_{VDD} (LP3)	Deep-sleep mode	25.6	208	µA

4.9.1.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (LP1)	Sleep mode 1	4.02	17.7	mA
I_{VDD} (LP2)	Sleep mode 2	2.78	6.4	mA
I_{VDD} (LP3)	Deep-sleep mode	20.7	200	µA

4.9.2 MCU Operating Mode Power Consumption

The MCU is under the following working conditions:

- Except for UART_LOG TXD/RXD (PB24/PB23), other I/O pins are in input mode.
- All peripherals except GPIO are disabled.

For different application scenarios, the required CPU operating frequency is different, and the corresponding power consumption will also be different.

Table 4-10 MCU operating mode

MCU operating mode	Dual core/single core (CA32)	KM0	KM4	CA32	VDL_CORE voltage
MCU operating mode 1-1	Single core	40MHz	333MHz	1.2GHz	1.0V
MCU operating mode 1-2	Dual core				
MCU operating mode 2-1	Single core	40MHz	333MHz	1GHz	1.0V
MCU operating mode 2-2	Dual core				
MCU operating mode 3-1	Single core	40MHz	230MHz	920MHz	0.9V
MCU operating mode 3-2	Dual core				
MCU operating mode 4-1	Single core	40MHz	230MHz	460MHz	0.9V
MCU operating mode 4-2	Dual core				

In the case of the same operating mode, the CPU will be in different modes at different times.

Table 4-11 IC status in operation mode

Operating mode	KM0 mode	KM4 mode	CA32 mode	SWR_AUD mode	SWR_MEM mode[1]	Wi-Fi/BT state	SRAM state
Active mode 1	WFI[2]	WFI	WFI	OFF	PWM	OFF	Standby
Active mode 2	WFI	WFI	NOP[3]	OFF	PWM	OFF	Standby
Active mode 3	NOP	NOP	NOP	OFF	PWM	OFF	Standby
Active mode 4	NOP	NOP	RW RAM[4]	OFF	PWM	OFF	Standby

NOTE

[1] For RTL8730EAH-VA3, SWR_MEM is always in PFM mode.

[2] WFI (Wait for interrupt): Arm instruction

[3] NOP (NO Operation): Arm instruction

[4] RW RAM:

- *For RTL8730ELH-VA7/-VA8 and RTL8730EAH-VH6, DDR SDRAM is in active mode, and CA32 reads and writes DDR SDRAM continuously.*
- *For RTL8730EAH-VA3/VD3 and RTL8730ELH-VA3, PSRAM is in active mode, and CA32 reads and writes PSRAM continuously.*

4.9.2.1 MCU Operating Mode 1-1

4.9.2.1.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	26.2	56.6	mA
I_{VDD} (Active 2)	Active mode 2	52.9	88.1	
I_{VDD} (Active 3)	Active mode 3	62.7	100	
I_{VDD} (Active 4)	Active mode 4	82.0	123	

4.9.2.1.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	37.6	79.6	mA
I_{VDD} (Active 2)	Active mode 2	63.8	112	
I_{VDD} (Active 3)	Active mode 3	73.8	124	
I_{VDD} (Active 4)	Active mode 4	289	362	

4.9.2.1.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	36.3	71.6	mA
I_{VDD} (Active 2)	Active mode 2	62.6	104	
I_{VDD} (Active 3)	Active mode 3	73.0	117	
I_{VDD} (Active 4)	Active mode 4	291	362	

4.9.2.1.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	37.2	73.0	mA
I_{VDD} (Active 2)	Active mode 2	64.1	107	
I_{VDD} (Active 3)	Active mode 3	74.1	119	
I_{VDD} (Active 4)	Active mode 4	268	328	

4.9.2.2 MCU Operating Mode 1-2

4.9.2.2.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	26.7	60.9	mA
I_{VDD} (Active 2)	Active mode 2	81.3	126	
I_{VDD} (Active 3)	Active mode 3	92.0	140	
I_{VDD} (Active 4)	Active mode 4	104	153	

4.9.2.2.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	38.1	80.0	mA
I_{VDD} (Active 2)	Active mode 2	91.0	143	
I_{VDD} (Active 3)	Active mode 3	102	156	
I_{VDD} (Active 4)	Active mode 4	327	407	

4.9.2.2.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	37.1	76.3	mA
I_{VDD} (Active 2)	Active mode 2	90.9	144	
I_{VDD} (Active 3)	Active mode 3	102	158	
I_{VDD} (Active 4)	Active mode 4	333	425	

4.9.2.2.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	38.0	79.3	mA
I_{VDD} (Active 2)	Active mode 2	92.4	148	
I_{VDD} (Active 3)	Active mode 3	104	162	
I_{VDD} (Active 4)	Active mode 4	320	390	

4.9.2.3 MCU Operating Mode 2-1

4.9.2.3.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	24.0	53.8	mA
I_{VDD} (Active 2)	Active mode 2	45.8	79.9	
I_{VDD} (Active 3)	Active mode 3	55.8	91.5	
I_{VDD} (Active 4)	Active mode 4	76.3	116	

4.9.2.3.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	36.1	76.8	mA
I_{VDD} (Active 2)	Active mode 2	57.1	104	
I_{VDD} (Active 3)	Active mode 3	66.6	116	
I_{VDD} (Active 4)	Active mode 4	282	354	

4.9.2.3.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	34.7	69.1	mA
I_{VDD} (Active 2)	Active mode 2	55.9	95.6	
I_{VDD} (Active 3)	Active mode 3	65.8	108	
I_{VDD} (Active 4)	Active mode 4	285	353	

4.9.2.3.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	35.5	70.1	mA
I_{VDD} (Active 2)	Active mode 2	57.2	97.6	
I_{VDD} (Active 3)	Active mode 3	66.9	110	
I_{VDD} (Active 4)	Active mode 4	259	319	

4.9.2.4 MCU Operating Mode 2-2

4.9.2.4.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	24.4	58.1	mA
I_{VDD} (Active 2)	Active mode 2	68.9	112	
I_{VDD} (Active 3)	Active mode 3	79.7	124	
I_{VDD} (Active 4)	Active mode 4	94.0	141	

4.9.2.4.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	36.9	77.3	mA
I_{VDD} (Active 2)	Active mode 2	80.6	129	
I_{VDD} (Active 3)	Active mode 3	90.5	142	
I_{VDD} (Active 4)	Active mode 4	317	394	

4.9.2.4.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	35.7	74.5	mA
I_{VDD} (Active 2)	Active mode 2	79.8	130	
I_{VDD} (Active 3)	Active mode 3	90.3	143	
I_{VDD} (Active 4)	Active mode 4	323	411	

4.9.2.4.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	36.6	75.9	mA
I_{VDD} (Active 2)	Active mode 2	81.6	133	
I_{VDD} (Active 3)	Active mode 3	91.8	146	
I_{VDD} (Active 4)	Active mode 4	300	374	

4.9.2.5 MCU Operating Mode 3-1

4.9.2.5.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	19.3	40.5	mA
I_{VDD} (Active 2)	Active mode 2	35.4	59.1	
I_{VDD} (Active 3)	Active mode 3	40.8	65.6	
I_{VDD} (Active 4)	Active mode 4	60.4	88.0	

4.9.2.5.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	30.8	60.9	mA
I_{VDD} (Active 2)	Active mode 2	46.6	80.5	
I_{VDD} (Active 3)	Active mode 3	52.1	87.2	
I_{VDD} (Active 4)	Active mode 4	256	307	

4.9.2.5.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.2	53.5	mA
I_{VDD} (Active 2)	Active mode 2	44.7	72.2	
I_{VDD} (Active 3)	Active mode 3	50.3	78.7	
I_{VDD} (Active 4)	Active mode 4	256	302	

4.9.2.5.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.8	54.4	mA
I_{VDD} (Active 2)	Active mode 2	45.7	73.9	
I_{VDD} (Active 3)	Active mode 3	51.3	80.5	
I_{VDD} (Active 4)	Active mode 4	231	271	

4.9.2.6 MCU Operating Mode 3-2

4.9.2.6.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	19.6	43.2	mA
I_{VDD} (Active 2)	Active mode 2	52.5	81.6	
I_{VDD} (Active 3)	Active mode 3	58.1	88.6	
I_{VDD} (Active 4)	Active mode 4	73.6	106	

4.9.2.6.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	30.9	61.3	mA
I_{VDD} (Active 2)	Active mode 2	63.7	100	
I_{VDD} (Active 3)	Active mode 3	70.2	107	
I_{VDD} (Active 4)	Active mode 4	288	344	

4.9.2.6.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.9	56.9	mA
I_{VDD} (Active 2)	Active mode 2	62.3	96.0	
I_{VDD} (Active 3)	Active mode 3	68.1	103	
I_{VDD} (Active 4)	Active mode 4	291	348	

4.9.2.6.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	30.8	57.9	mA
I_{VDD} (Active 2)	Active mode 2	63.5	98.1	
I_{VDD} (Active 3)	Active mode 3	69.4	105	
I_{VDD} (Active 4)	Active mode 4	265	313	

4.9.2.7 MCU Operating Mode 4-1

4.9.2.7.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	17.6	38.6	mA
I_{VDD} (Active 2)	Active mode 2	25.6	47.8	
I_{VDD} (Active 3)	Active mode 3	30.8	53.9	
I_{VDD} (Active 4)	Active mode 4	52.9	79.1	

4.9.2.7.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.0	59.0	mA
I_{VDD} (Active 2)	Active mode 2	36.7	68.5	
I_{VDD} (Active 3)	Active mode 3	42.0	75.0	
I_{VDD} (Active 4)	Active mode 4	238	286	

4.9.2.7.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	27.5	51.5	mA
I_{VDD} (Active 2)	Active mode 2	35.2	60.6	
I_{VDD} (Active 3)	Active mode 3	40.3	66.9	
I_{VDD} (Active 4)	Active mode 4	238	281	

4.9.2.7.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	28.1	52.4	mA
I_{VDD} (Active 2)	Active mode 2	36.0	62.0	
I_{VDD} (Active 3)	Active mode 3	41.3	68.4	
I_{VDD} (Active 4)	Active mode 4	211	248	

4.9.2.8 MCU Operating Mode 4-2

4.9.2.8.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	18.0	41.4	mA
I_{VDD} (Active 2)	Active mode 2	33.9	60.0	
I_{VDD} (Active 3)	Active mode 3	39.2	66.5	
I_{VDD} (Active 4)	Active mode 4	59.6	89.6	

4.9.2.8.2 RTL8730EAH-VH6

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.8	59.5	mA
I_{VDD} (Active 2)	Active mode 2	45.7	78.4	
I_{VDD} (Active 3)	Active mode 3	51.1	84.6	
I_{VDD} (Active 4)	Active mode 4	270	324	

4.9.2.8.3 RTL8730ELH-VA7

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	28.3	54.9	mA
I_{VDD} (Active 2)	Active mode 2	43.9	73.8	
I_{VDD} (Active 3)	Active mode 3	49.3	80.3	
I_{VDD} (Active 4)	Active mode 4	273	327	

4.9.2.8.4 RTL8730ELH-VA8

Symbol	Operating mode	Typ.		Unit
		25°C	85°C	
I_{VDD} (Active 1)	Active mode 1	29.1	55.8	mA
I_{VDD} (Active 2)	Active mode 2	45.0	75.4	
I_{VDD} (Active 3)	Active mode 3	50.4	82.1	
I_{VDD} (Active 4)	Active mode 4	247	291	

4.9.3 RF Power Consumption

RF power consumption refers to the static power consumption of the IC in Tx/Rx states as well as Idle/Standby states under MP mode.

The RF power consumption data is based on the EVB of Realtek EV730EL0_5V0. The operating voltage is 3.3V, and all emission data are measured based on 100% duty cycle.

All measurements are tested under the following working conditions:

- CPU working mode:
  - CPU frequency: KM0 40MHz, KM4 333MHz, CA32 1.2GHz.
  - All CPUs are in WFI working state.
- Operation mode:
  - Active (RF works):
    - Continuous Tx (Duty 100%)
    - Packet Rx
  - RF Standby: In this mode, only CBC&SYN circuits work.
  - RF Shutdown: In this mode, all RF circuits are off.
- Channel:
  - CH4 @2.4G 20M
  - CH36 @5G 20M

4.9.3.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3 & RTL8730EAH-VH6 & RTL8730ELH-VA7 & RTL8730ELH-VA8

Frequency band	Condition	Typ. (25°C)	Unit
2.4G	1T-11ax MCS9/BW20M (16dBm)	303	mA
	1T-11ax MCS0/BW20M (20dBm)	381	
	1T-11ac MCS8/BW20M (17dBm)	320	
	1T-11ac MCS0/BW20M (20dBm)	381	
	1T-11n MCS7/BW20M (18dBm)	341	
	1T-11n MCS0/BW20M (20dBm)	382	
	1T-OFDM54M (19dBm)	361	
	1T-OFDM6M (20dBm)	381	
	1T-CCK11M (20dBm)	375	
	1T-CCK1M (20dBm)	375	
	1R (Pin idle)	67	
	1R-11ax MCS9/BW20M (Pin= -60dBm)	73	
	1R-11ac MCS8/BW20M (Pin= -60dBm)	73	
	1R-11n MCS7/BW20M (Pin= -60dBm)	73	
	1R-OFDM54M (Pin= -60dBm)	73	
	1R-CCK11M (Pin= -60dBm)	67	
	1R Beacon (Pin idle)	45	
	1R Beacon CCK1M (Pin= -60dBm)	45	
	RF Standby	50	
	RF Shutdown	33	
5G	1T-11ax MCS9/BW20M (15dBm)	367	mA
	1T-11ax MCS0/BW20M (20dBm)	436	
	1T-11ac MCS8/BW20M (16dBm)	376	
	1T-11ac MCS0/BW20M (20dBm)	439	
	1T-11n MCS7/BW20M (17dBm)	387	
	1T-11n MCS0/BW20M (20dBm)	437	
	1T-OFDM54M (18dBm)	400	
	1T-OFDM6M (20dBm)	436	
	1R (Pin idle)	70	
	1R-11ax MCS9/BW20M (Pin= -60dBm)	78	
	1R-11ac MCS8/BW20M (Pin= -60dBm)	78	
	1R-11n MCS7/BW20M (Pin= -60dBm)	78	
	1R-OFDM54M (Pin= -60dBm)	78	
	1R Beacon (Pin idle)	59	
	1R Beacon OFDM6M (Pin= -60dBm)	66	
	RF Standby	50	
	RF Shutdown	33	

NOTE

For descriptions and definitions of other RF states, refer to the RFC table.

4.9.4 WoWLAN Power Consumption

This section provides power consumption data in Wake on Wireless Lan (WoWLAN) state. The power consumption data in the following sections are the results of the IC operating at 25°C with a 3.3V power supply.

All measurements are tested under the following conditions:

- MCU working conditions:
  - Except for UART_LOG TXD/RXD (PB24/PB23), other I/O pins are in input mode.
  - All peripherals except GPIOs are disabled.
  - The CPU is in PG mode outside the wake-up state.
- WoWLAN power consumption test conditions:
  - Test environment: shielded room
  - AP: Tenda AX3000
  - Wi-Fi frequency bands 2.4G and 5G are measured separately.
  - The power consumption when Delivery Traffic Indication Message (DTIM) is 1/3/10 is measured separately.
  - Take the average current value within 20 minutes as the test value.

4.9.4.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

DTIM	Wi-Fi frequency band	Typ.	Unit
DTIM=1	2.4G	1.32	mA
	5G	1.24	
DTIM=3	2.4G	0.691	
	5G	0.663	
DTIM=10	2.4G	0.470	
	5G	0.436	

4.9.4.2 RTL8730EAH-VH6

DTIM	Wi-Fi frequency band	Typ.	Unit
DTIM=1	2.4G	2.80	mA
	5G	2.65	
DTIM=3	2.4G	2.13	
	5G	2.07	
DTIM=10	2.4G	1.90	
	5G	1.86	

4.9.4.3 RTL8730ELH-VA7

DTIM	Wi-Fi frequency band	Typ.	Unit
DTIM=1	2.4G	2.84	mA
	5G	2.77	
DTIM=3	2.4G	2.23	
	5G	2.18	
DTIM=10	2.4G	2.03	
	5G	1.99	

4.9.4.4 RTL8730ELH-VA8

DTIM	Wi-Fi frequency band	Typ.	Unit
DTIM=1	2.4G	3.77	mA
	5G	3.67	
DTIM=3	2.4G	3.17	
	5G	3.13	
DTIM=10	2.4G	2.97	
	5G	2.94	

4.9.5 Maximum Power Consumption

The maximum power consumption scenario will cause the IC temperature to rise significantly, so the heat dissipation of the circuit board will have a great impact on the temperature rise and current data.

This section provides current data in the maximum power consumption scenario when the operating voltage is 3.3V, which is measured on Realtek's EVB.

The maximum power consumption scenario is as follows:

- KM0: 40MHz
- KM4: 333MHz, continuously accesses RAM
- CA32: 1.2GHz, dual-core continuously reads and writes DDR SDAM or PSRAM
- Audio: MIC continuous to record (power consumption includes microphone), and audio lineout continuous playback (power consumption does not include speaker device)
- USB: turned on, but no device is connected to the USB port
- MIPI: continues to transmit data through High-Speed mode (the frequency of the two data lanes is 363MHz), but there is no external display screen

- Wi-Fi: continuously Tx at 20dbm power on 2.4G CH1
- BT: S0 channel continues to transmit according to the power of 8dbm

4.9.5.1 RTL8730EAH-VA3/VD3 & RTL8730ELH-VA3

Symbol	Parameter	Condition	Maximum power consumption (mA)
I_{VDD33}	Absolute maximum power consumption at 3.3V DC power supply	Ambient temperature = 25°C	543
		Junction temperature = 125°C	612

4.9.5.2 RTL8730EAH-VH6

Symbol	Parameter	Condition	Maximum power consumption (mA)
I_{VDD33}	Absolute maximum power consumption at 3.3V DC power supply	Ambient temperature = 25°C	844
		Junction temperature = 125°C	932

4.9.5.3 RTL8730ELH-VA7

Symbol	Parameter	Condition	Maximum power consumption (mA)
I_{VDD33}	Absolute maximum power consumption at 3.3V DC power supply	Ambient temperature = 25°C	859
		Junction temperature = 125°C	938

4.9.5.4 RTL8730ELH-VA8

Symbol	Parameter	Condition	Maximum power consumption (mA)
I_{VDD33}	Absolute maximum power consumption at 3.3V DC power supply	Ambient temperature = 25°C	762
		Junction temperature = 125°C	855

4.10 RF Characteristics

4.10.1 WLAN Radio Specifications

This section describes the RF characteristics of WLAN 2.4GHz and 5GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

NOTE

The WLAN radio performance values listed in this section are based on 25°C, 3.3V, 50ohm@Lab environment & Realtek EVB.

4.10.1.1 WLAN 2.4GHz Band Receiver Performance

Table 4-12 WLAN 2.4GHz band receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Rx Sensitivity 802.11b	1Mbps CCK		-100		dBm
	2Mbps CCK		-96.5		dBm
	5.5Mbps CCK		-94.5		dBm
	11Mbps CCK		-90		dBm
Rx Sensitivity 802.11g	BPSK rate 1/2, 6Mbps OFDM		-95		dBm
	BPSK rate 3/4, 9Mbps OFDM		-94		dBm
	QPSK rate 1/2, 12Mbps OFDM		-92		dBm
	QPSK rate 3/4, 18Mbps OFDM		-89.5		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-86		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-83		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-79		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-77		dBm

Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-95		dBm
	MCS 1, QPSK rate 1/2		-92		dBm
	MCS 2, QPSK rate 3/4		-89.5		dBm
	MCS 3, 16-QAM rate 1/2		-86		dBm
	MCS 4, 16-QAM rate 3/4		-82.5		dBm
	MCS 5, 64-QAM rate 2/3		-78.5		dBm
	MCS 6, 64-QAM rate 3/4		-77		dBm
	MCS 7, 64-QAM rate 5/6		-75.5		dBm
Rx Sensitivity 802.11ax BW = 20MHz	MCS 0, BPSK rate 1/2		-93.5		dBm
	MCS 1, QPSK rate 1/2		-90.5		dBm
	MCS 2, QPSK rate 3/4		-88		dBm
	MCS 3, 16-QAM rate 1/2		-85		dBm
	MCS 4, 16-QAM rate 3/4		-82		dBm
	MCS 5, 64-QAM rate 2/3		-77.5		dBm
	MCS 6, 64-QAM rate 3/4		-76		dBm
	MCS 7, 64-QAM rate 5/6		-75		dBm
	MCS 8, 256-QAM rate 3/4		-71		dBm
	MCS 9, 256-QAM rate 5/6		-69		dBm
Max. Receive Level	6Mbps OFDM		0		dBm
	54Mbps OFDM		0		dBm
	11n MCS 0 HT20		0		dBm
	11n MCS 7 HT20		0		dBm
	11ax MCS 0 HE20		0		dBm
	11ax MCS 8 HE20		0		dBm
Adjacent Channel Rejection	11Mbps CCK		48		dB
	BPSK rate 1/2, 6Mbps OFDM		40		dB
	64-QAM rate 3/4, 54Mbps OFDM		26		dB
	HT20, MCS 0, BPSK rate 1/2		39		dB
	HT20, MCS 7, 64-QAM rate 5/6		24		dB
	HE20, MCS 0, BPSK rate 1/2		39		dB
	HE20, MCS 8, 256-QAM rate 3/4		21		dB
	HE20, MCS 9, 256-QAM rate 5/6		19		dB

4.10.1.2 WLAN 2.4GHz Band Transmitter Performance

Table 4-13 WLAN 2.4GHz band transmitter performance

Parameter	**Condition**	**Performance**			**Unit**
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK		20		dBm
	11Mbps CCK		20		dBm
	BPSK rate 1/2, 6Mbps OFDM		20		dBm
	64-QAM rate 3/4, 54Mbps OFDM		20		dBm
	HT20,MCS 0, BPSK rate 1/2		20		dBm
	HT20, MCS 7, 64-QAM rate 5/6		20		dBm
	HE20, MCS 8, 256-QAM rate 3/4		19		dBm
	HE20, MCS 9, 256-QAM rate 5/6		17		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM			-5	dB
	64-QAM rate 3/4, 54Mbps OFDM			-25	dB
	HT20, MCS 0, BPSK rate 1/2			-5	dB
	HT20, MCS 7, 64-QAM rate 5/6			-27	dB
	HE20, MCS 8, 256-QAM rate 3/4			-30	dB
	HE20, MCS 9, 256-QAM rate 5/6			-32	dB
Output power variation	TSSI on across operating temperature range, all channels and VSWR≤1.5:1 at RFIO port	-1.5		1.5	dB
Carrier suppression				-32	dBc
Harmonic output power[2]	2nd harmonic		-18		dBm/MHz

	3rd harmonic		-24		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable. The output power is measured at antenna port on Realtek EVB and the EVB loss of 2.4G is approximately 1.6dB. The actual Tx power will be different from suggested power level according to PCB losses and national regulatory restrictions. The MP (massive production) power may be lower than power level mentioned above. Please refer to MP Flow document for further data.

[2] Harmonic output power is tested at IC port.

[3] Harmonic output power is measured at RF connector with diplexer (DP1608-R2455DBR1) and appropriate matching.

4.10.1.3 WLAN 5GHz Band Receiver Performance

Table 4-14 WLAN 5GHz band receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5885	MHz
Rx Sensitivity 802.11a	BPSK rate 1/2, 6Mbps OFDM		-94.5		dBm
	BPSK rate 3/4, 9Mbps OFDM		-93.5		dBm
	QPSK rate 1/2, 12Mbps OFDM		-92		dBm
	QPSK rate 3/4, 18Mbps OFDM		-89.5		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-86		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-83		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-79		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-77		dBm
Rx Sensitivity 802.11n/ac BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-94		dBm
	MCS 1, QPSK rate 1/2		-91.5		dBm
	MCS 2, QPSK rate 3/4		-89		dBm
	MCS 3, 16-QAM rate 1/2		-86		dBm
	MCS 4, 16-QAM rate 3/4		-82.5		dBm
	MCS 5, 64-QAM rate 2/3		-78.5		dBm
	MCS 6, 64-QAM rate 3/4		-77		dBm
	MCS 7, 64-QAM rate 5/6		-75.5		dBm
Rx Sensitivity 802.11ac	MCS 8, 256-QAM rate 3/4		-71		dBm
Rx Sensitivity 802.11ax BW = 20MHz	MCS 0, BPSK rate 1/2		-94		dBm
	MCS 1, QPSK rate 1/2		-90.5		dBm
	MCS 2, QPSK rate 3/4		-88.5		dBm
	MCS 3, 16-QAM rate 1/2		-85		dBm
	MCS 4, 16-QAM rate 3/4		-82		dBm
	MCS 5, 64-QAM rate 2/3		-78		dBm
	MCS 6, 64-QAM rate 3/4		-76.5		dBm
	MCS 7, 64-QAM rate 5/6		-75		dBm
	MCS 8, 256-QAM rate 3/4		-71		dBm
	MCS 9, 256-QAM rate 5/6		-69.5		dBm
Max. Receive Level	6Mbps OFDM		0		dBm
	54Mbps OFDM		0		dBm
	11n MCS 0 HT20		0		dBm
	11n MCS 7 HT20		0		dBm
	11ax MCS 0 HE20		0		dBm
	11ax MCS 8 HE20		0		dBm
Adjacent Channel Rejection	BPSK rate 1/2, 6Mbps OFDM		30		dB
	64-QAM rate 3/4, 54Mbps OFDM		12		dB
	HT20, MCS 0, BPSK rate 1/2		28		dB
	HT20, MCS 7, 64-QAM rate 5/6		8		dB
	HE20, MCS 0, BPSK rate 1/2		28		dB
	HE20, MCS 8, 256-QAM rate 3/4		3		dB
	HE20, MCS 9, 256-QAM rate 5/6		1		dB

4.10.1.4 WLAN 5GHz Band Transmitter Performance

Table 4-15 WLAN 5GHz band transmitter performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5885	MHz
Output power with spectral mask and EVM compliance[1]	BPSK rate 1/2, 6Mbps OFDM		19		dBm
	64-QAM rate 3/4, 54Mbps OFDM		19		dBm
	HT20, MCS 0, BPSK rate 1/2		19		dBm
	HT20, MCS 7, 64-QAM rate 5/6		19		dBm
	HE20, MCS 8, 256-QAM rate 3/4		19		dBm
	HE20, MCS 9, 256-QAM rate 5/6		17		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM			-5	dB
	64-QAM rate 3/4, 54Mbps OFDM			-25	dB
	HT20, MCS 0, BPSK rate 1/2			-5	dB
	HT20, MCS 7, 64-QAM rate 5/6			-27	dB
	HE20, MCS 8, 256-QAM rate 3/4			-30	dB
	HE20, MCS 9, 256Q-AM rate 5/6			-32	dB
Output power variation	TSSI on across operating temperature range, all channels and VSWR≤1.5:1 at RFIO port	-1.5		1.5	dB
Carrier suppression				-32	dBc
Harmonic output power[2]	2nd harmonic		-40		dBm/MHz
	3rd harmonic		-40		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable. The output power is measured at antenna port on Realtek EVB and the EVB loss of 5G is approximately 1.5dB. The actual Tx power will be different from suggested power level according to PCB losses and national regulatory restrictions. The MP (massive production) power may be lower than power level mentioned above. Please refer to MP Flow document for further data.

[2] Harmonic output power is tested at IC port.

[3] Harmonic output power is measured at RF connector with diplexer (DP1608-R2455DBR1) and appropriate matching.

4.10.2 Bluetooth Radio Specifications

This section describes the RF characteristics of Bluetooth 2.4GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

NOTE

- *The Bluetooth radio performance values listed in this section are based on 25°C, 3.3V, 50ohm@Lab environment & Realtek EVB.*
- *S0 is dedicated for Bluetooth, and S1 is shared with Wi-Fi.*

4.10.2.1 Basic Rate (BR) Receiver Performance

Table 4-16 BR receiver performance

Parameter	Condition	Performance (S0)			Performance (S1)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Receiver Sensitivity	BER<0.1%		-93[1]			-93[1]		dBm
Max. Usable Signal	BER<0.1%		0			0		dBm
C/I co-channel (BER<0.1%)	Co-channel sensitivity		11			11		dB
C/I 1MHz (BER<0.1%)	Adjacent channel selectivity		-14			-13		dB
C/I 2MHz (BER<0.1%)	2nd adjacent channel selectivity		-44			-41		dB
C/I 3MHz (BER<0.1%)	3rd adjacent channel selectivity		-50			-50		dB
C/I Image Channel (BER<0.1%)	Image channel selectivity		-22			-23		dB
C/I Image 1MHz (BER<0.1%)	1MHz adjacent to image channel selectivity		-32			-34		dB
Inter-modulation			-31			-33.5		dBm

Out-of-band blocking[2]	30MHz to 2000MHz	-10			-10			dBm
	2000MHz to 2400MHz	-27			-27			dBm
	2500MHz to 3000MHz	-27			-27			dBm
	3000MHz to 12.75GHz	-10			-10			dBm

NOTE

[1] The receiver sensitivity is measured at the chip output, and channels 2440MHz and 2480MHz may have extra degradation due to spurious interference.

[2] Frequencies where the requirements are not met are called "spurious response frequencies". The number of spurs must not exceed 24 if blocking signal power level is as specified above, and must not exceed 5 if it is reduced to -50dBm.

4.10.2.2 Basic Rate (BR) Transmitter Performance

Table 4-17 BR transmitter performance

Parameter	Condition	Performance (S0)			Performance (S1)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Max. Transmit Power	At max. power output level		7			8		dBm
Gain step			4			4		dB
Modulation characteristics	Δf1 avg.		160			160		kHz
	Δf2 max. (for at least 99.9% of all Δf2 max.)	115			115			kHz
	Δf1 avg./Δf2 avg.		0.9			0.9		
ICFT[1]	Initial carrier frequency tolerance		±15			±15		kHz
Carrier Frequency Drift	One slot packet (DH1)		±10			±10		kHz
	Two slot packet (DH3)		±10			±10		kHz
	Five slot packet (DH5)		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Tx Output Spectrum	20dB bandwidth			1000			1000	kHz
In-Band Spurious Emission	±2MHz offset		-47			-44		dBm
	±3MHz offset		-50			-47		dBm
	>±3MHz offset		-50			-47		dBm

NOTE

[1] Initial carrier frequency offset should be calibrated in MP process in the customer side.

4.10.2.3 Enhanced Data Rate (EDR) Receiver Performance

Table 4-18 EDR receiver performance

Parameter	Condition	Performance (S0)			Performance (S1)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Receiver Sensitivity (BER<0.1%)	π/4 DQPSK		-93[1]			-93[1]		dBm
	8PSK		-86[1]			-86[1]		dBm
Max. Usable Signal (BER<0.1%)	π/4 DQPSK		0			0		dBm
	8PSK		0			0		dBm
C/I co-channel (BER<0.1%)	π/4 DQPSK		11			11		dB
	8PSK		17			17		dB
C/I 1MHz (BER<0.1%)	π/4 DQPSK		-13			-13		dB
	8PSK		-5			-5		dB
C/I 2MHz (BER<0.1%)	π/4 DQPSK		-44			-41		dB
	8PSK		-37			-40		dB
C/I 3MHz (BER<0.1%)	π/4 DQPSK		-50			-50		dB
	8PSK		-45			-46		dB
C/I Image Channel (BER<0.1%)	π/4 DQPSK		-22			-23		dB
	8PSK		-16			-17		dB
C/I Image 1MHz (BER<0.1%)	π/4 DQPSK		-32			-35		dB
	8PSK		-24			-30		dB

NOTE

[1] The receiver sensitivity is measured at the chip output, and channels 2440MHz and 2480MHz may have extra degradation due to spurious interference.

4.10.2.4 Enhanced Data Rate (EDR) Transmitter Performance

Table 4-19 EDR transmitter performance

Parameter	Condition		Performance (S0)			Performance (S1)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency		2402		2480	2402		2480	MHz
Maximum Transmit Power	π/4 DQPSK			7			8		dBm
	8PSK			7			8		dBm
Relative Transmit Power	π/4 DQPSK			-1			-1		dB
	8PSK			-1			-1		dB
Frequency Stability	Max. carrier frequency stability, ωo	π/4 DQPSK		±10			±10		kHz
		8PSK		±10			±10		kHz
	Max. carrier frequency stability, ωi	π/4 DQPSK		±15			±15		kHz
		8PSK		±15			±15		kHz
	Max. carrier frequency stability, |ωo + ωi|	π/4 DQPSK		±15			±15		kHz
		8PSK		±15			±15		kHz
Modulation Accuracy	RMS DEVM	π/4 DQPSK			20			20	%
		8PSK			13			13	%
	99% DEVM	π/4 DQPSK			30			30	%
		8PSK			20			20	%
	Peak DEVM	π/4 DQPSK			35			35	%
		8PSK			25			25	%
In-Band	±1MHz offset	π/4 DQPSK		40			34		dB
	±1MHz offset	8PSK		40			33		dB
Spurious Emission	±2MHz offset	π/4 DQPSK		-34			-28		dBm
	±2MHz offset	8PSK		-33			-28		dBm
	±3MHz offset	π/4 DQPSK		-42			-41		dBm
	±3MHz offset	8PSK		-42			-41		dBm

4.10.2.5 Bluetooth Low Energy (BLE) Receiver Performance

Table 4-20 BLE receiver performance

Parameter	Condition	Performance (S0)			Performance (S1)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Bluetooth LE 1Mbps								
Receiver Sensitivity	PER<30.8%		-96.5[1]			-96.5[1]		dBm
Max. Usable Signal	PER<30.8%		0			0		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		7			7		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-4			-4		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-44			-47		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-52			-53		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-28			-27		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-26			-30		dB
Inter-modulation			-30			-32.5		dBm
Out-of-band blocking[2]	30MHz to 2000MHz	-30			-30			dBm
	2003MHz to 2399MHz	-35			-35			dBm
	2484MHz to 2997MHz	-35			-35			dBm
	3000MHz to 12.75GHz	-30			-30			dBm
Bluetooth LE 2Mbps								
Receiver Sensitivity	PER<30.8%		-93.5[1]			-93.5[1]		dBm
Max. Usable Signal	PER<30.8%		0			0		dBm

C/I co-channel (PER<30.8%)	Co-channel sensitivity		7			7		dB
C/I 2MHz (PER<30.8%)	Adjacent channel selectivity		-2			-2		dB
C/I 4MHz (PER<30.8%)	2nd adjacent channel selectivity		-42			-43		dB
C/I >= 6MHz (PER<30.8%)	3rd adjacent channel selectivity		-51			-53		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-27			-27		dB
C/I Image 2MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-23			-27		dB
Inter-modulation			-30			-32.5		dBm
Out-of-band blocking[2]	30MHz to 2000MHz	-30			-30			dBm
	2003MHz to 2399MHz	-35			-35			dBm
	2484MHz to 2997MHz	-35			-35			dBm
	3000MHz to 12.75GHz	-30			-30			dBm
Bluetooth LE 125kbps								
Receiver Sensitivity	PER<30.8%		-106[1]			-106[1]		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		4			5		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-15			-14		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-52			-53		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-52			-62		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-33			-32		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-35			-39		dB
Bluetooth LE 500kbps								
Receiver Sensitivity	PER<30.8%		-100[1]			-100[1]		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		5			5		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-9			-9		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-45			-49		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-49			-56		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-31			-34		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-29			-30		dB

NOTE

[1] The receiver sensitivity is measured at the chip output, and channels 2440MHz and 2480MHz may have extra degradation due to spurious interference.

[2] Frequencies where the requirements are not met are called "spurious response frequencies". The number of spurs must not exceed 10 if blocking signal power level is as specified above, and must not exceed 3 if it is reduced to -50dBm.

4.10.2.6 Bluetooth Low Energy (BLE) Transmitter Performance

Table 4-21 BLE transmitter performance

Parameter	Condition	Performance (S0)			Performance (S1)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Output Power	At max. power output level		7			8		dBm
Bluetooth LE 1Mbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±15			±15		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		250			250		kHz
	Δf2 max.	185			185			kHz
	Δf1 avg./Δf2 avg.		0.9			0.9		
In-Band Spurious Emission	±2MHz offset		-44			-42		dBm
	>±3MHz offset		-48			-46		dBm
Bluetooth LE 2Mbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±30			±30		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		500			500		kHz
	Δf2 max.	370			370			kHz

	Δf1 avg./Δf2 avg.		0.9			0.9		
In-Band Spurious Emission	±4MHz offset		-43			-46		dBm
	±5MHz offset		-49			-46		dBm
	>±6MHz offset		-50			-46		dBm
Bluetooth LE 125kbps								
Carrier Frequency Offset and Drift	Frequency offset[1]		±15			±15		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz/50us
Modulation characteristics	Δf1 avg.		250			250		kHz
	Δf1 max.	185			185			kHz

NOTE

[1] Initial carrier frequency offset should be calibrated in MP process in the customer side.

4.11 Audio Characteristics

4.11.1 Audio ADC

Table 4-22 Analog performance of recording path

Parameter	Conditions		Min.	Typ.	Max.	Unit
Sample rate	8/16/32/44.1/48/88.2/96		8	48	96	kHz
Bit width	Configured by I2S interface data length		8	16	24	Bits
Analog supply voltage (VAM_AUD)	Powered by system power source		1.71	1.8	1.98	V
Reference voltage (LDOA_OUT)	From reference generator LDO			1.8		V
MICBIAS	LDO for analog microphone			1.8		V
MIC boost gain	0/5/10/15/20/25/30/35/40		0	20	40	dB
ADC channel variation	Measured at -10dBV@1kHz input			±0.2		dB
MICBIAS noise floor	MICBIAS=1.8V, load=3mA			-100		dBV
SNR	B/W=20Hz~20kHz, A-weighted, 0dB gain, VAM_AUD = 1.8V	Single-ended mode		98		dBA
		Differential mode		98		dBA
THD+N @-3dBFS output	VAM_AUD = 1.8V, 0dB gain	Single-ended mode		-80		dB
	VAM_AUD = 1.8V, 0dB gain	Differential mode		-80		dB

4.11.2 Audio DAC

Table 4-23 Analog performance of playback path

Parameter	Conditions		Min.	Typ.	Max.	Unit
Sample rate	8/16/22.05/32/44.1/48/88.2/96/192		8	48	192	kHz
Bit width	Configured by I2S interface data length		8	16	24	Bits
Analog supply voltage (VAM_AUD)	Powered by system power source		1.71	1.8	1.98	V
Reference voltage (LDOA_OUT)	From reference generator LDO			1.8		V
Output amplitude	Single-ended mode			0.5		Vrms
	Differential mode			1		Vrms
Crosstalk between channels	L vs. R, 1kHz@-10dBFS input, load=32Ω, VAM_AUD = 1.8V, single-ended mode			-80		dB
SNR	B/W=20Hz~20kHz, A-weighted, load=10k/32Ω, VAM_AUD = 1.8V	Single-ended mode		98		dBA
		Differential mode		98		dBA
Noise Floor	B/W=20Hz~20kHz, A-weighted, load=10k/32Ω, VAM_AUD = 1.8V	Single-ended mode		-100		dBV
		Differential mode		-100		dBV
THD+N @-3dBFS output	10kΩ load, VAM_AUD = 1.8V, single-ended mode			-85		dB
	32Ω load, VAM_AUD = 1.8V, single-ended mode			-85		dB

4.12 General ADC Characteristics

Table 4-24 ADC characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
VAH_PLL	Analog power supply	-		2.97	3.3	3.63	V
fs	ADC sample frequency	-		31.25	166.67	250	kHz
V_{in}[1]	Conversion input voltage range	External channel (CH0 ~ CH5)		0	-	1.8	V
		BAT_MEAS channel		0	-	5	
R_{in}	Input impedance (to GND)	External channel (CH0 ~ CH5)		412	491	574	kΩ
		BAT_MEAS channel		142	160	179	
t_{STAB}	ADC total power-up time	Including internal LDO power-up time		-	-	190	µs
I_{DDA}	ADC power consumption	T_A = 25°C, fs = 166.67kHz, including internal Band Gap		-	263	-	µA
Resolution	-	-		-	12	-	bits
EO	Offset error	fs = 166.67kHz, VAH_PLL = 3.3V, T_A = 25°C	External channel	-	±10	-	LSB
			BAT_MEAS channel	-	±12	-	
EG	Gain error		External channel	-	±10	-	
			BAT_MEAS channel	-	±12	-	
INL[2]	Integral linearity error		External channel	-	-	7	
DNL[2]	Differential linearity error		External channel	-	-	3	
SFDR[2]	Spurious free dynamic range		External channel	-	56	-	dB
THD[2]	Total harmonic distortion		External channel	-	-50	-	
SNDR[2]	Signal-to-noise and distortion ratio		External channel	-	52	-	
ENOB[2]	Effective number of bits		External channel	-	8.5	-	bits

NOTE

[1] The ADC conversion voltage range is fixed at 0 ~ 1.8V.

[2] There is the ADC performance with calibration. Nonlinearity will be partially corrected after calibration.

4.13 QSPI Flash Controller Characteristics

This section describes the timing characteristics of the Quad Serial Peripheral Interface (QSPI) for Flash controller.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high or weak driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V.
- The process includes all corners.

NOTE

All timing is shown with respect to 30% V_{IO} and 70% V_{IO} thresholds. Refer to Section 4.8 for definitions of V_{IO}.

Table 4-25 Timing data of QSPI Flash controller

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SCL}	Clock period	Master	10	-	ns
t_{LOW}	Clock Low time	Master	45%*T_{SCL}	55%*T_{SCL}	ns
t_{HIGH}	Clock High time	Master	45%*T_{SCL}	55%*T_{SCL}	ns
t_r	Data/Clock raise time	Master	-	1	ns
t_f	Data/Clock fall time	Master	-	1	ns
$t_{SU;DAT(I)}$	Data input setup time	Master	2	-	ns
$t_{HD;DAT(I)}$	Data input hold time	Master	1	-	ns
$t_{SU;DAT(O)}$	Data output setup time	Master	(T_{SCL}/2) − 2	-	ns
$t_{HD;DAT(O)}$	Data output hold time	Master	(T_{SCL}/2) − 2	-	ns
$t_{VD;DAT(O)}$	Data output valid time	Master	-1	1	ns
$t_{SU;CS(A)}$	CS active setup time relative to CLK	Master	(T_{SCL}/2) − 2	-	ns
$t_{HD;CS(A)}$	CS active hold time relative to CLK	Master	T_{SCL}-2	-	ns

NOTE

- *The timing data of $t_{SU;DAT(I)}$ is only applicable to clock frequency of 20MHz or below. When QSPI needs a faster clock frequency, the RTL8730E would activate a special sampling mechanism internally.*
- *The timing data of $t_{SU;CS(A)}$ and $t_{HD;CS(A)}$ can be adjusted by configuring registers, and the adjustment unit is TSCL/2.*

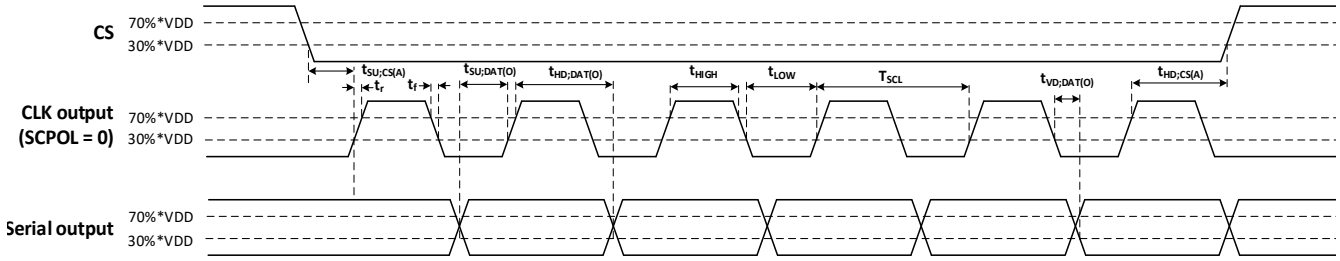


Figure 4-6 Output timing diagram (SCPH = 0)

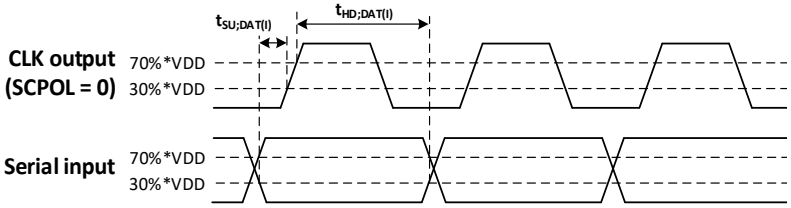


Figure 4-7 Input timing diagram (SCPH = 0)

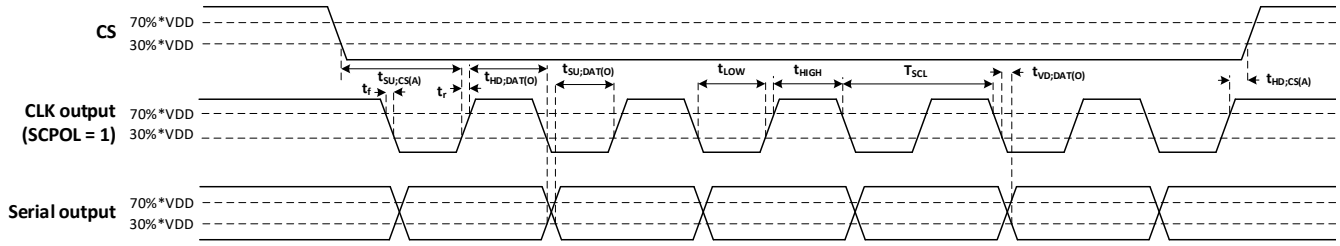


Figure 4-8 Output timing diagram (SCPH = 1)

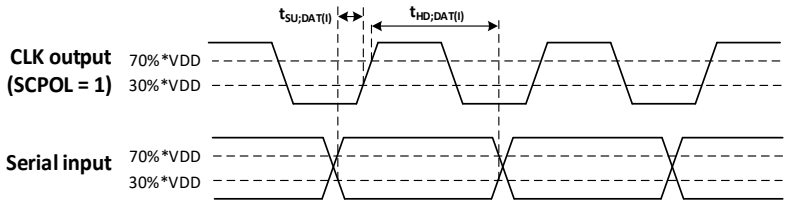


Figure 4-9 Input timing diagram (SCPH = 1)

4.14 SPI Characteristics

Only the specified pins configured as function ID3 can be used as SPI in combination:

- Group 1: PA2, PA3, PA4, PA5
- Group 2: PA9, PA10, PA11, PA12
- Group 3: PA13, PA14, PA15, PA16
- Group 4: PA26, PA27, PA28, PA29
- Group 5: PB3, PB4, PB5, PB6
- Group 6: PB10, PB11, PB12, PB13
- Group 7: PB17, PB18, PB19, PB20
- Group 8: PB25, PB26, PB27, PB28
- Group 9: PB29, PB30, PB31, PC0

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.

- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

- *Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.*
- *When the pins of Group 4 or Group 5 are used as SPI, the I/O power can only be fixed at 1.8V (typical).*

Table 1-3 Timing data of SPI

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	20	-	20	-	ns
		Slave	40	-	40	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	$1.5*T_{SCL} - 3$	-	$1.5*T_{SCL} - 3$	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	$T_{SCL} - 2$	-	$T_{SCL} - 2$	-	ns
		Slave	-	12	-	16	ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-2	2	-2	2	ns
		Slave	-	12	-	16	ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	3	-	3	-	ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	3	-	3	-	ns

NOTE

- *The maximum value of $t_{VD;DAT(SO)}$ is already greater than half of a 50MHz clock cycle, so when used as a slave, the maximum speed supported by SPI is 25MHz. But if the connected master supports sampling with a delay of at least 10ns, it could support up to max. 50MHz.*
- *The timing data of $t_{SU;DAT(MI)}$ is only applicable to speeds of 25MHz or below. When the RTL8730E is used as a master running at 50MHz, due to the sample delay function of IC, the accepted minimum value of $t_{SU;DAT(MI)}$ can be -3ns for 1.8V I/O and -5ns for 3.3V I/O.*

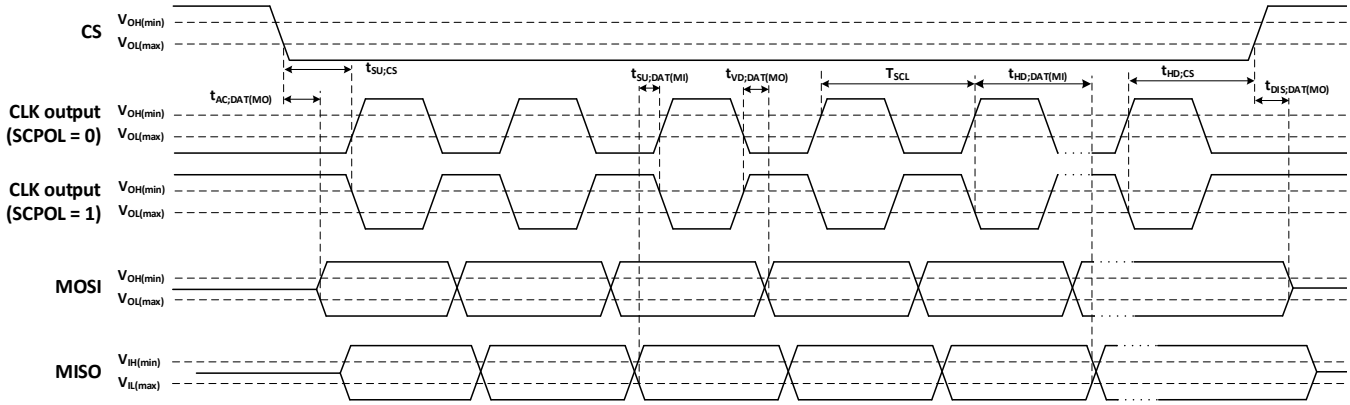


Figure 1-3 Timing diagram for master (SCPH = 0)

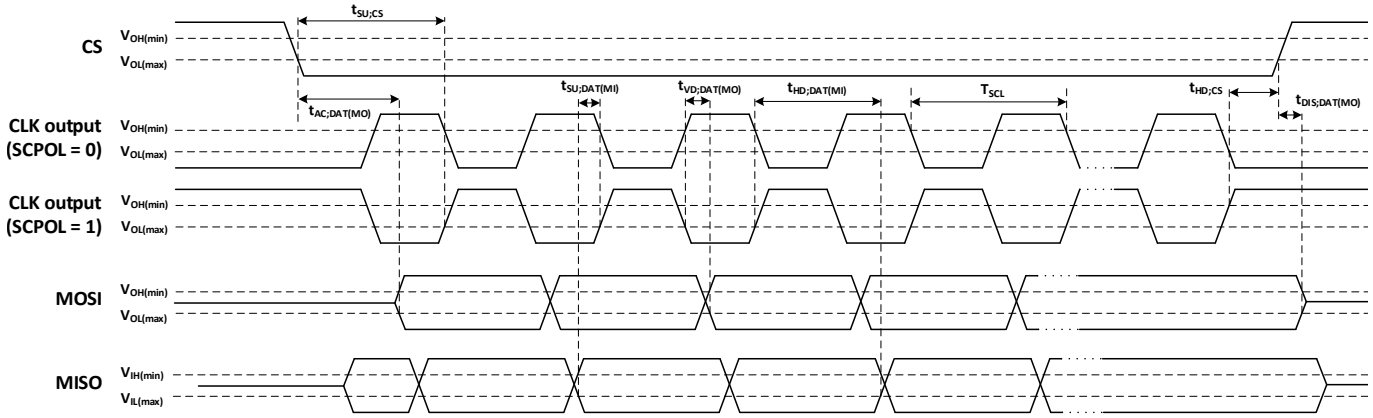


Figure 1-4 Timing diagram for master (SCPH = 1)

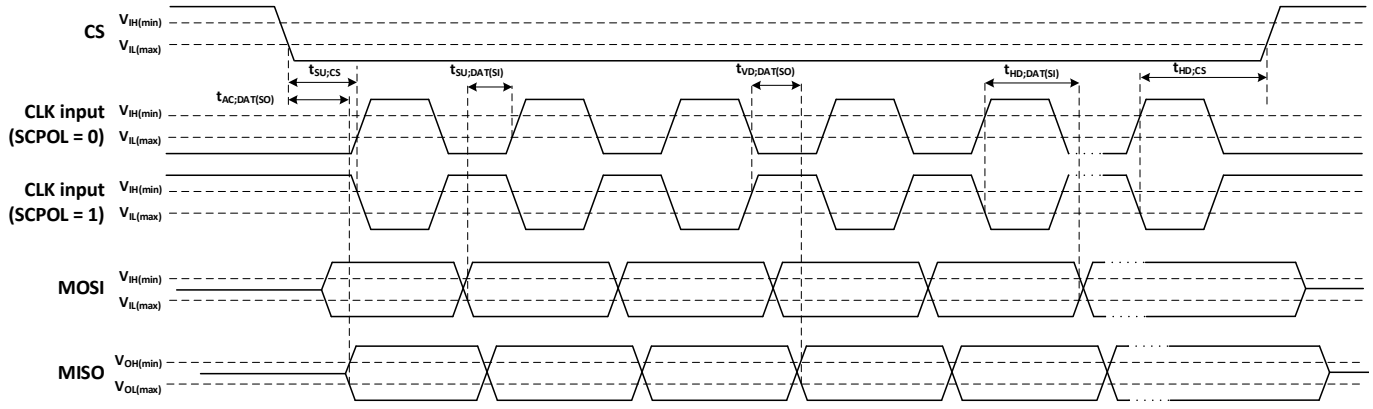


Figure 1-5 Timing diagram for slave (SCPH = 0)

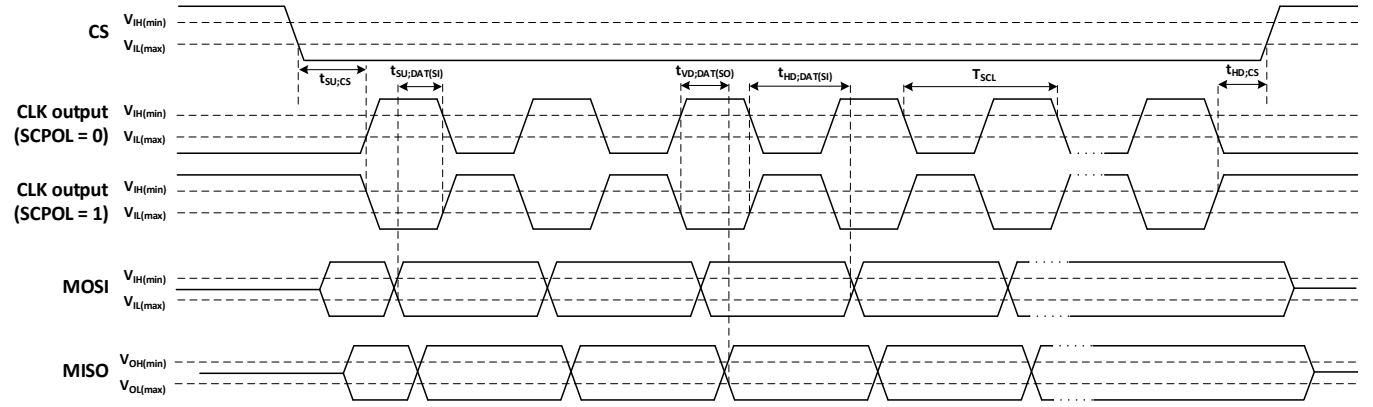


Figure 1-5 Timing diagram for slave (SCPH = 1)

4.15 I2C Characteristics

All measurements are tested under the following conditions:

- The maximum loading is 400pF (SS mode, 1.7M FS mode), 100pF (3.4M HS mode).
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The process includes all corners.

NOTE

All timing is shown with respect to 30% V_{IO} and 70% V_{IO} thresholds. Refer to Section 4.8 for definitions of V_{IO}.

Table 1-1 Timing data of I2C (FS/SS mode)

Symbol	Parameter	Standard mode (Cb=400pF max.)		Fast mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	-	100	-	400	kHz
$t_{HD;STA}$	Hold time START condition	4	-	0.6	-	µs
t_{LOW}	Low period of the SCL clock	Programmable		Programmable		µs
t_{High}	High period of the SCL clock					µs
t_r	Raise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	-	300	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	us
$t_{SU;DAT}$	Data set-up time	0.25	-	0.1	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4	-	0.6	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs

NOTE

- *Cb is the capacitive load for each bus line.*
- *The resistance value of the pull-up resistor needs to be calculated and determined according to the loading on the bus.*

Table 1-2 Timing data of I2C (HS mode)

Symbol	Parameter	High-Speed mode (Cb=100pF max.)		High-Speed mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	-	3.4	-	1.7	MHz
$t_{HD;STA}$	Hold time START condition	160	-	160	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	160	-	160	-	ns
$t_{HD;DAT}$	Data hold time	0	70	0	150	ns
$t_{SU;DAT}$	Data set-up time	10	-	10	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	160	-	160	-	ns
t_{high}	High period of the SCL clock	Programmable		Programmable		ns
t_{low}	Low period of the SCL clock					ns
t_{rCL}	Rise time of SCLH signal	-	40	-	80	ns
t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	20	160	ns
t_{rDA}	Rise time of SDAH signal	10	80	20	160	ns
t_{fCL}	Fall time of SCLH signal	-	40	-	80	ns
t_{fDA}	Fall time of SDAH signal	-	80	-	160	ns

NOTE

- *Cb is the capacitive load for each bus line.*
- *The resistance value of the pull-up resistor needs to be calculated and determined according to the loading on the bus.*

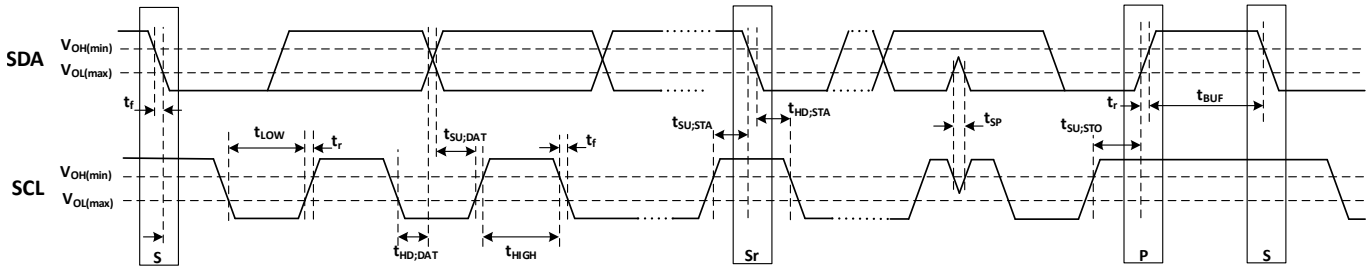


Figure 1-4-10 Timing diagram of I2C (FS/SS mode)

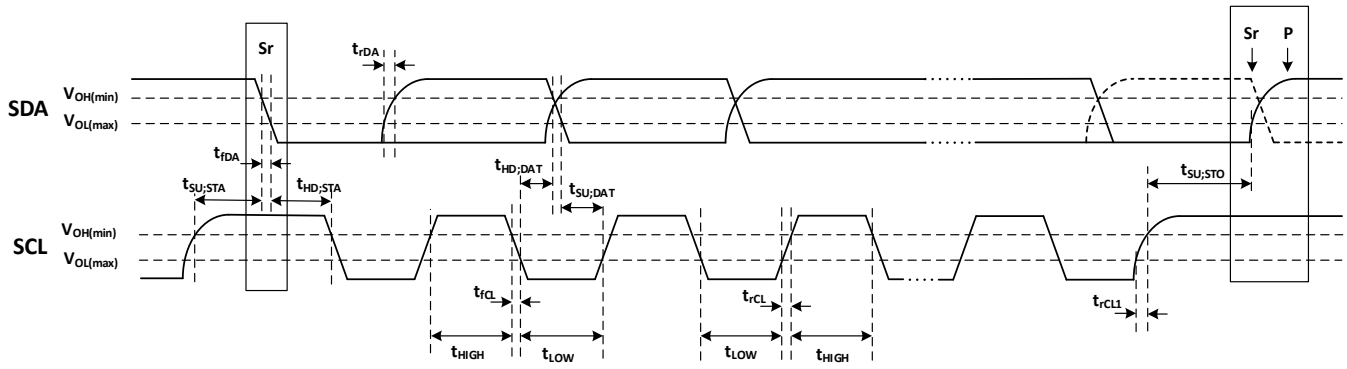


Figure 1-2 Timing diagram of I2C (HS mode)

NOTE

In HS mode, the first rising edge of SCLH signal after a repeated start condition is push-pull output instead of open-drain output.

4.16 UART Characteristics

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-26 Timing data of UART

Item	Conditions	Min.	Typ.	Max.	Unit
Transfer rate	TXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 2MHz OSC			115200	bps

NOTE

Total baud rate error shall be less than 3% in order to communicate correctly, which includes three parts: the error of real baud rate of Tx device and expected communication baud rate, the frequency drift of Rx IP clock, and the calculation baud error of Rx device. Users can enable the function of monitoring baud rate of Rx data to decrease the baud rate error.

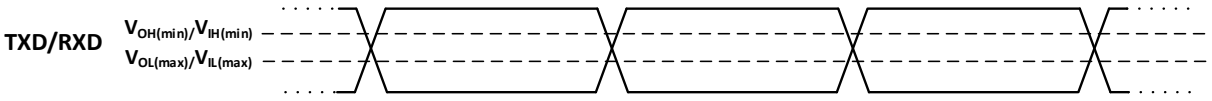


Figure 4-11 Timing diagram of UART

4.17 LEDC Characteristics

The LEDC is used to control external intelligent LED lamp.

Table 4-27 Timing data of LEDC

Symbol	Description	Default value	Value range	Unit
T_{0H}	Digital 0 code, high-level time	300	25 ~ 6375	ns
T_{0L}	Digital 0 code, low-level time	800	25 ~ 6375	ns
T_{1H}	Digital 1 code, high-level time	800	25 ~ 6375	ns
T_{1L}	Digital 1 code, low-level time	300	25 ~ 6375	ns
RESET	Frame unit, low-level time	300	25 ~ 409575	ns
wait_time0	Low-Level time between two pixels' data.	-	25 ~ 12775	ns
wait_time1	Low-Level time after RESET except for the 1th frame	-	25 ~ 5.3e10	ns

NOTE

- *The adjustable unit of the symbol value is 25ns.*
- *Wait_time0 and Wait_time1 are optional, default disable.*

The sequence of logic "1" code, logic "0" code and refresh period differs in intelligent LEDs. The basic sequence decode chart is shown in *Figure 4-12*.

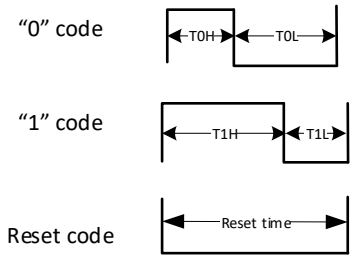


Figure 4-12 LED decode data sequence

Figure 4-13 shows the LEDC frame output. Before sending a frame of data, a RESET is sent to refresh the LED lamp. 'wait_time1' is used to slow down the refresh rate.

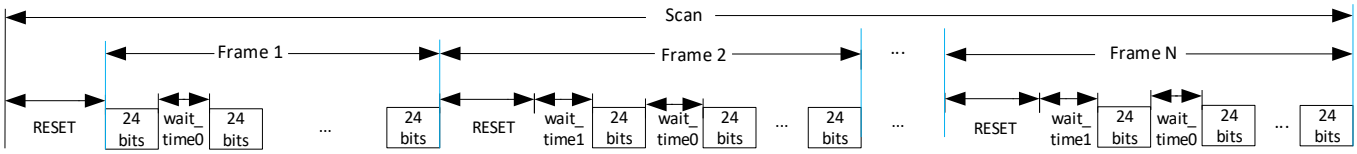


Figure 4-13 LEDC output timing diagram of a scan

4.18 I2S Characteristics

The Inter-IC Sound (I2S) supports both master and slave operations. The following tables and diagrams provide timing characteristics for I2S.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-28 Timing data of I2S

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	I2S clock	Master	41	1953	41	1953	ns
		Slave	41	1953	41	1953	ns
Duty	Clock duty	Master	45	55	45	55	%
		Slave	35	65	35	65	%
$t_{SU;DAT(I)}$	Input data setup time	Master	10	-	13	-	ns
$t_{SU;DAT(I)}$/$t_{SU;WS}$	Input data/WS setup time	Slave	5	-	5	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Master	0	-	0	-	ns
		Slave	5	-	5	-	ns
$t_{VD;DAT(O)}$	Output data valid time	Master	-4	4	-4	4	ns
$t_{VD;WS}$	Output WS valid time	Master	-4	4	-4	4	ns
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	13	-	17	ns

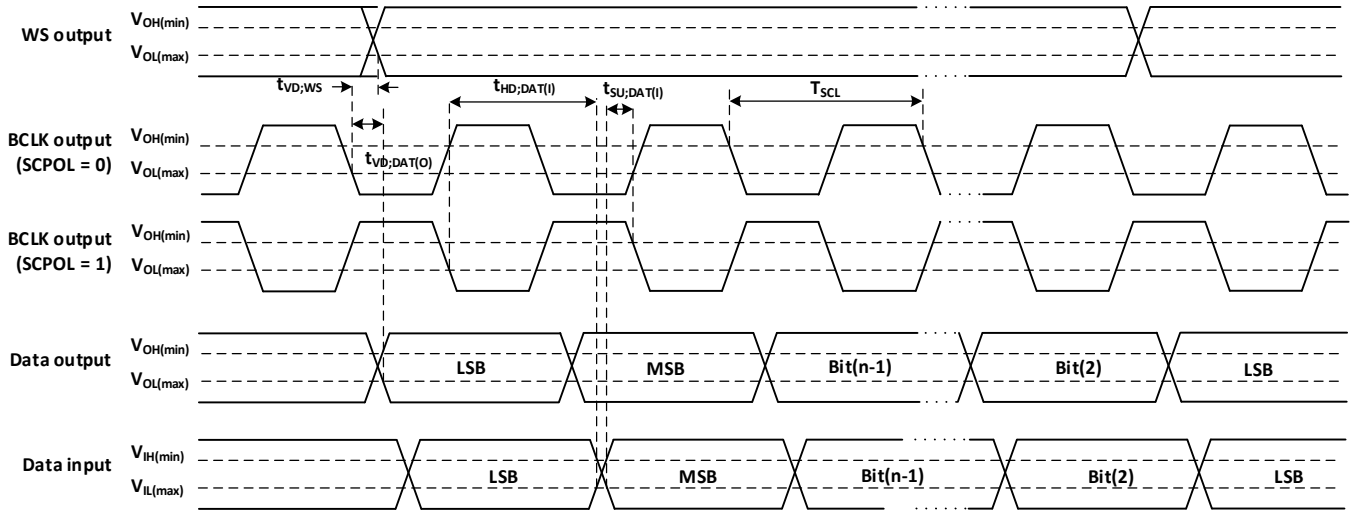


Figure 4-14 Timing diagram for I2S master

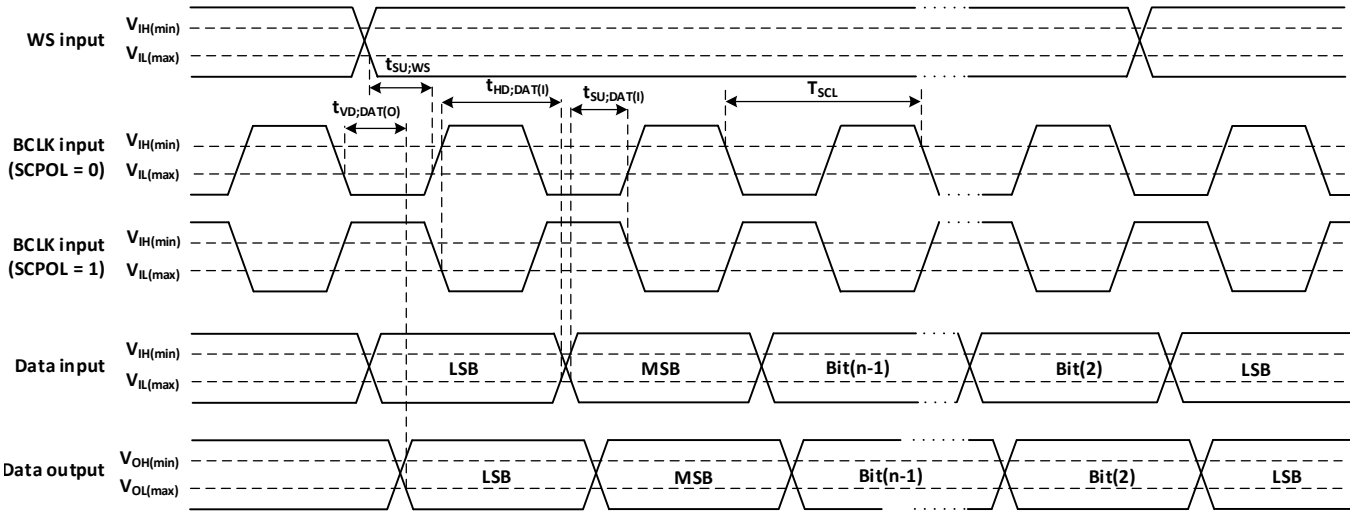


Figure 4-15 Timing diagram for I2S slave

4.19 DMIC Characteristics

The Digital Microphone (DMIC) supports only master operations. The following tables and diagrams provide timing characteristics for DMIC.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-29 Timing data of DMIC

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	DMIC clock period	Master	200	32000	20	32000	ns
Duty cycle	DMIC clock duty cycle	Master	45	55	45	55	%
$t_{SU;DAT(R)}$/$t_{SU;DAT(F)}$	Input data rising/falling edge setup time	Master	13	-	13	-	ns
$t_{HD;DAT(R)}$/$t_{HD;CS(F)}$	Input data rising/falling edge hold time	Master	2	-	2	-	ns

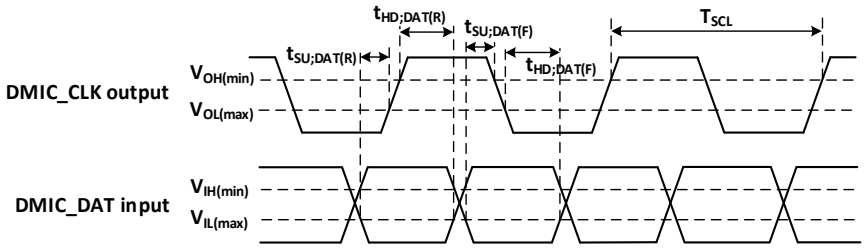


Figure 4-16 Timing diagram of DMIC

4.20 PDM Characteristics

The Pulse Density Modulation (PDM) supports only master operations. The following tables and diagrams provide timing characteristics for PDM.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-30 Timing Data of PDM

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	PDM clock period	Master	150	400	150	400	ns
Duty cycle	PDM clock duty cycle	Master	45	55	45	55	%
$t_{VD;DAT(R)}/t_{VD;DAT(F)}$	Output data rising/falling edge valid time	Master	22	28	22	28	ns

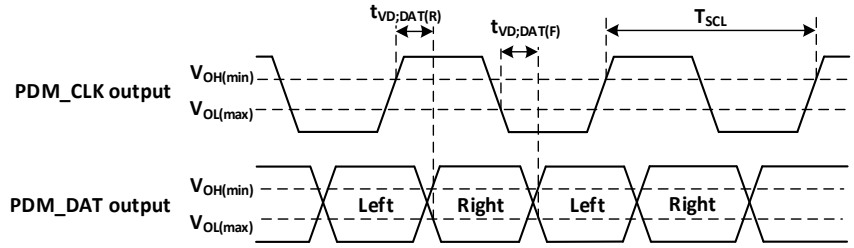


Figure 4-17 Timing diagram of PDM

4.21 MIPI-DSI Characteristics

The D-PHY is designed according to MIPI Alliance's D-PHY V1.2. The DSI is designed according to MIPI Alliance's DSI V1.3.

Table 4-31 MIPI parameter specification

Parameter		Description	Min.	Typ.	Max.	Unit
|VOD|		HS transmit differential voltage	0.14	0.2	0.27	V
LP Mode	V_{OH}	Output high level	1.1	1.2	1.3	V
	V_{OL}	Output low level	-50	-	50	mV
HS mode	V_{OH}	HS output high voltage	-	-	360	mV
	V_{OL}	HS output low voltage	-	-	-	-
HS Mode Clock Lane	T_R	HS rise time	-	-	0.3	UI[1]
	T_F	HS fall time	-	-	0.3	UI
HS Mode Data Lane	T_R	HS rise time	-	-	0.3	UI

	T_F	HS fall time	-	-	0.3	UI
Skew	Data to clock	Data to clock skew	-0.15	-	0.15	UI

NOTE

[1] UI: Unit Interval, equal to the duration of any HS state on the Clock Lane.

4.22 SDIO Host Characteristics

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-32 Timing data of SDIO host (default speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SDIO clock period	Master	40	-	40	-	ns
Duty cycle	SDIO duty cycle	Master	45	55	45	55	%
$t_{VD;DAT(O)}/t_{VD;CMD(O)}$	Data output valid time	Master	-5	2	-5	2	ns
$t_{SU;DAT(I)}/t_{SU;CMD(I)}$	Data input setup time	Master	4	-	4	-	ns
$t_{HD;DAT(I)}/t_{HD;CMD(I)}$	Data input hold time	Master	2	-	2	-	ns

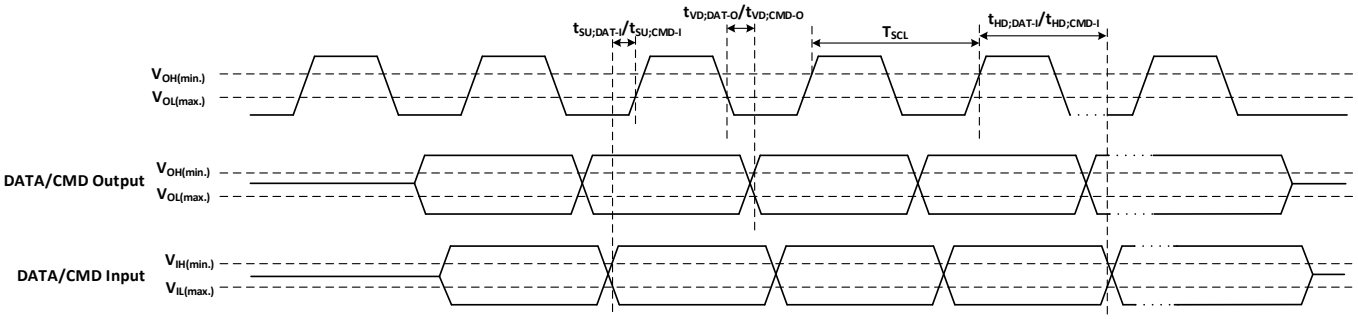


Figure 4-18 Timing parameters for SDIO host (default speed mode)

Table 4-33 Timing data of SDIO host (high speed mode)

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SDIO clock period	Master	20	-	20	-	ns
Duty cycle	SDIO duty cycle	Master	45	55	45	55	%
$t_{VD;DAT(O)}/t_{VD;CMD(O)}$	Data output valid time	Master	-5	2	-5	2	ns
$t_{SU;DAT(I)}/t_{SU;CMD(I)}$	Data input setup time	Master	9	-	9	-	ns
$t_{HD;DAT(I)}/t_{HD;CMD(I)}$	Data input hold time	Master	2	-	2	-	ns

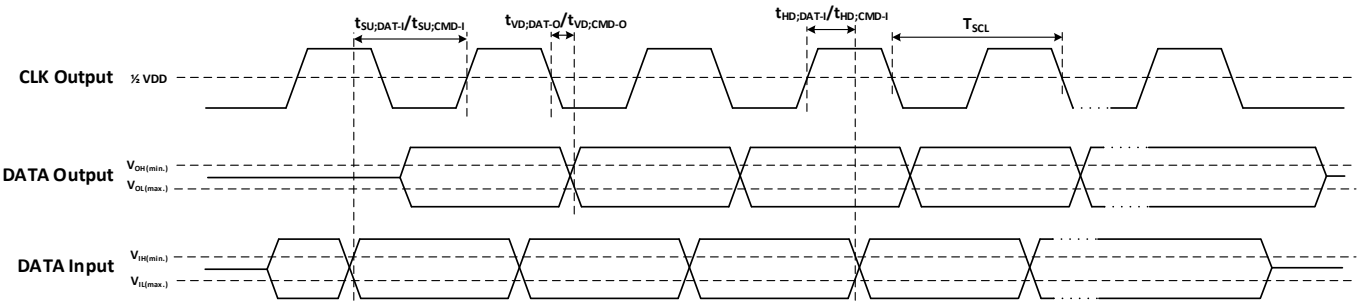


Figure 4-19 Timing parameters for SDIO host (high speed mode)

4.23 USB Interface Characteristics

The Universal Serial Bus (USB) interface complies with USB 2.0 standard. All AC parameters related to these buffers can be found within the USB 2.0 electrical specifications. The following sections give a brief overview of the electrical requirements on a USB interface. For extensive information, refer to the USB specification.

The USB of RTL8730E supports high-speed, full-speed and low-speed data rates.

4.23.1 Signal Level

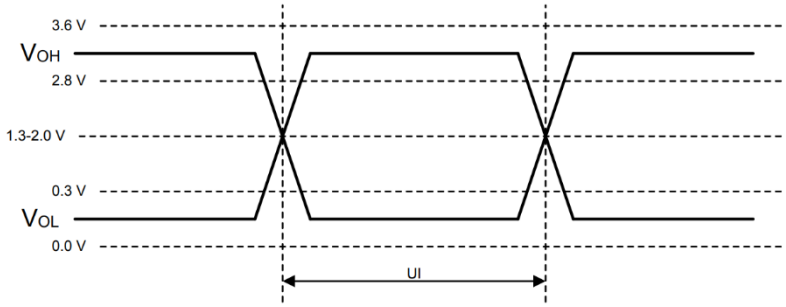


Figure 4-20 Signal waveform

Table 4-34 Signal waveform parameters

Mode	V_{OL}	V_{OH}	Bit period (UI)
High speed	-10 ~ 10mV	360 ~ 440mV	2.08ns
Full speed	0.0 ~ 0.3V	2.8 ~ 3.6V	83ns
Low speed	0.0 ~ 0.3V	2.8 ~ 3.6V	667ns

4.23.2 Signal Rising and Falling Times

The rising and falling times are measured from 10% ~ 90% of the signal low and high levels.

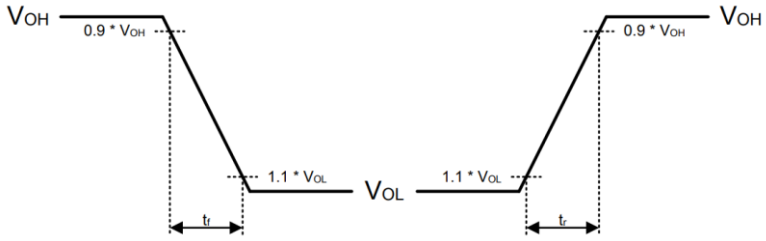


Figure 4-21 Data signal rising and falling time

For a device with detachable cable, the 10% to 90% high-speed differential rising and falling times must be 500ps or longer when measured at the A or B receptacles (respectively).

Table 4-35 Data signal rising and falling time

Mode	Rising/falling time (10% ~ 90%)
High speed	500ps
Full speed	4ns ~ 20ns
Low speed	75ns ~ 300ns

4.23.3 Speed Identification

A USB device must identify its data rate capabilities to the USB host. To do this, the USB standard has set up a scheme where USB hosts have a weak pull-down resistor on both data lines, and devices have a strong pull-up resistor on one of the data lines. The size of these resistors are set to ensure that the pull-up on the device-end will pull the data line from 0V to high (3.0V ~ 3.6V) as seen from the host.

Nominal values for these resistors are 15kΩ for the pull-downs on the host side, and 1.5kΩ for the pull-up on the device-end. When a device is connected to a host, the host checks which of the data lines is pulled high.

- Full-speed capable devices has the pull-up on D+
- Low-speed capable devices has the pull-up on D-
- High-speed USB connections are initialized as a full-speed connection, before a negotiation sequence sets up the transition to high speed.

4.24 Debug Interface Characteristics

The debug interface of RTL8730E is Arm standard bi-directional Serial Wire Debug (SWD).

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.71V to 1.98V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 5-37 Timing data of SWD

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SWCLK clock period	Slave	50	-	50	-	ns
Duty cycle	Input clock duty cycle	Slave	30	70	30	70	%
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	10	-	15	ns
$t_{VD;DAT(I)}$	Input data setup time	Slave	2	-	2	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Slave	2	-	2	-	ns

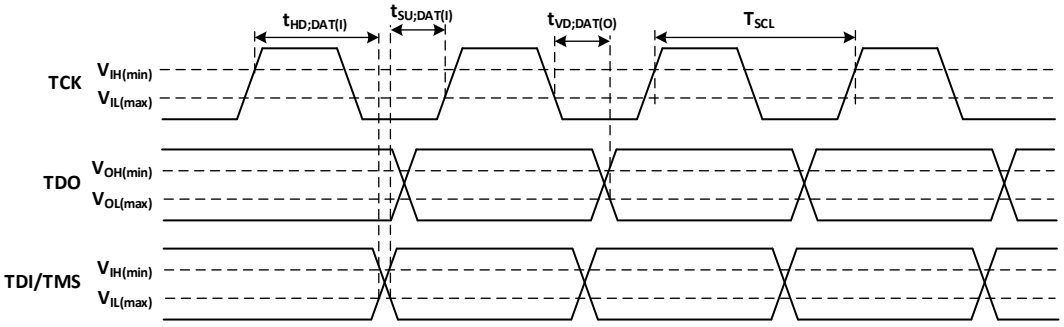


Figure 4-22 Timing diagram of SWD

5 Package Information

In order to meet environmental requirements, Realtek offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

5.1 Package Outline

5.1.1 QFN100 Package

The QFN100 package is a 100-pin, 10mm x 10mm quad flat no-leads package with 0.35mm pitch.

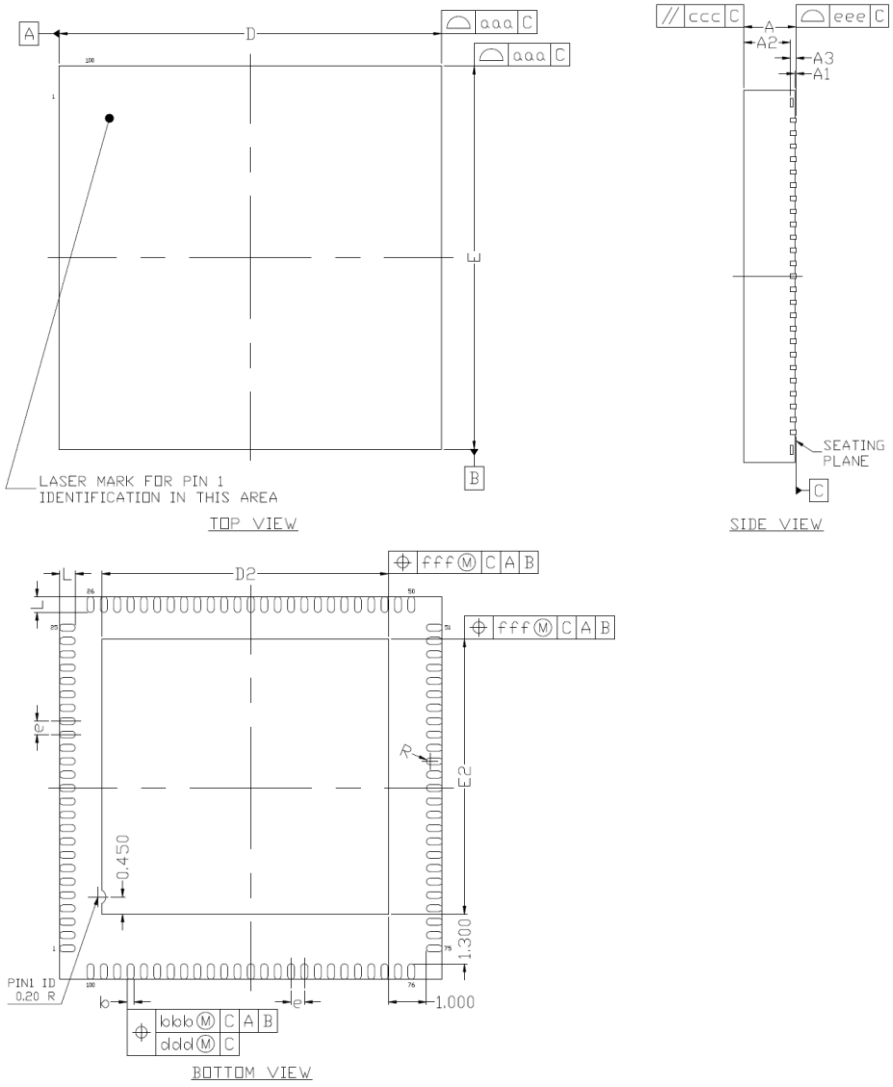


Figure 5-1 QFN100 package outline

Table 5-1 QFN100 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.500	-	-	0.059
A1	0.000	-	0.050	0.000	-	0.002
A2	-	1.250	1.300	-	0.049	0.051
A3	0.152 REF			0.006 REF		
b	0.130	0.180	0.230	0.005	0.007	0.009

D	10 BSC			0.394 BSC		
D2	7.400	7.500	7.600	0.291	0.295	0.299
E	10 BSC			0.394 BSC		
E2	7.100	7.200	7.300	0.280	0.283	0.287
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.350 BSC			0.014 BSC		
R	0.065	-	-	0.003	-	-
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

5.1.2 DR-QFN144 Package

The DR-QFN144 package is a 144-pin, 11mm x 11mm dual-row quad flat no-leads package with 0.5mm pitch.

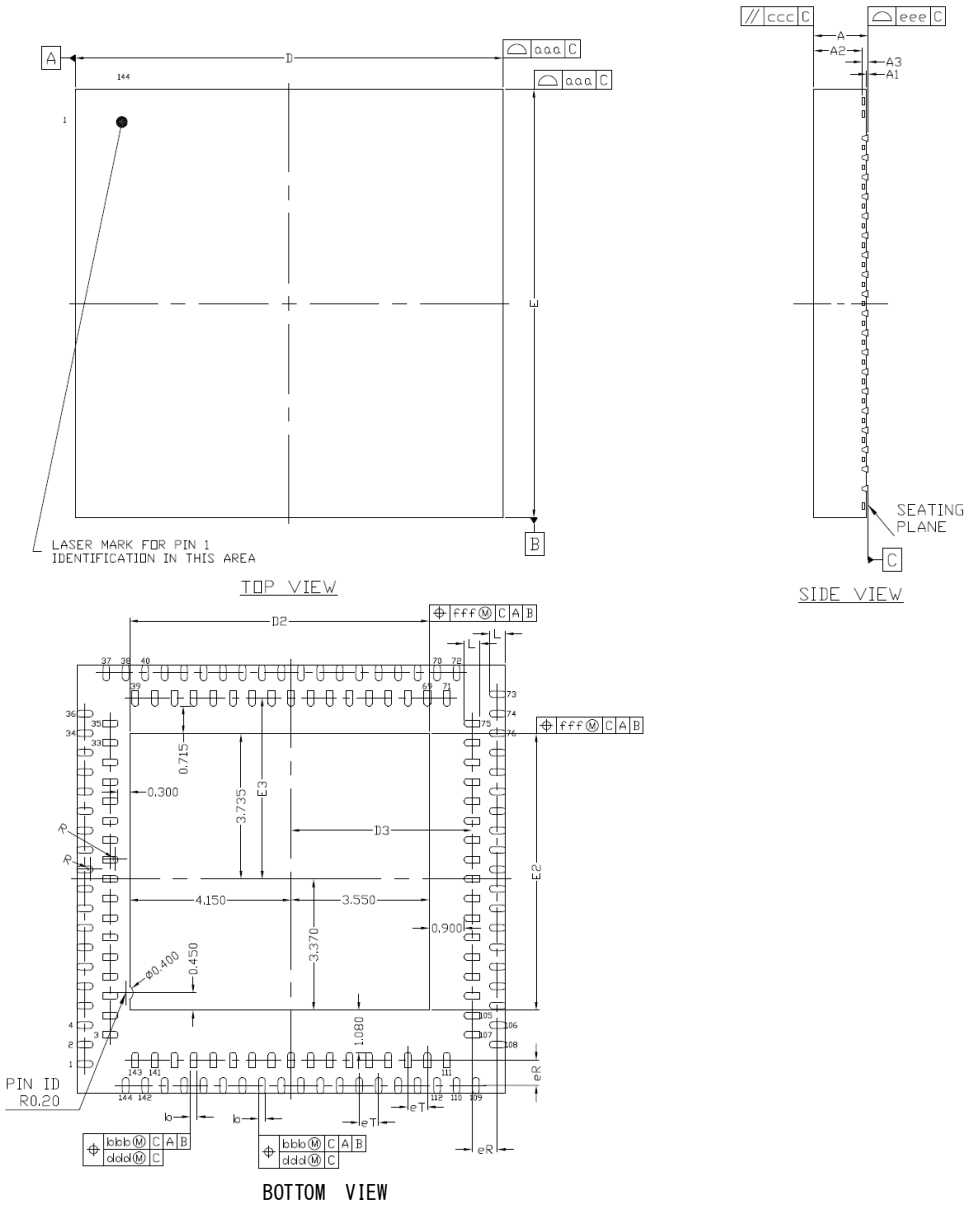


Figure 5-2 DR-QFN144 package outline

Table 5-2 DR-QFN144 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.500	-	-	0.059
A1	0.000	-	0.050	0.000	-	0.002
A2	-	1.250	1.300	-	0.049	0.051
A3	0.152 REF			0.006 REF		
b	0.150	0.200	0.250	0.005	0.007	0.010
D	11 BSC			0.433 BSC		
D2	7.600	7.700	7.800	0.299	0.303	0.307
D3	4.550	4.650	4.750	0.179	0.183	0.187
E	11 BSC			0.433 BSC		
E2	7.005	7.105	7.205	0.276	0.280	0.284
E3	4.550	4.650	4.750	0.179	0.183	0.187
L	0.300	0.400	0.500	0.012	0.016	0.020
eT	0.500 BSC			0.020 BSC		
eR	0.650 BSC			0.026 BSC		
R	0.065	-	-	0.003	-	-
aaa	0.150			0.006		
bbb	0.100			0.004		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

5.2 Thermal Characteristics

Table 5-3 Package thermal characteristics

Symbol	Parameter[1]		Condition	Value[2][3]	Unit
θ_{JA}	Junction-to-ambient thermal resistance	144-pin, DR-QFN package	85mm x 56mm 4-layer PCB with no air flow	27.9	°C/W
		100-pin, QFN package	85mm x 56mm 4-layer PCB with no air flow	29.7	
Ψ_{JT}	Junction-to-top center thermal characterization parameter	144-pin, DR-QFN package	85mm x 56mm 4-layer PCB with no air flow	0.61	
		100-pin, QFN package	85mm x 56mm 4-layer PCB with no air flow	0.7	
Ψ_{JB}	Junction-to-board thermal characterization parameter	144-pin, DR-QFN package	85mm x 56mm 4-layer PCB with no air flow	14.4	
		100-pin, QFN package	85mm x 56mm 4-layer PCB with no air flow	15.6	

NOTE

[1] Refer to EIA/JESD51-2, Integrated circuit Thermal Test Method Environment Conditions – Natural Convection (Still Air) for more information.

[2] These values are based on customized PCB systems designed by Realtek Semiconductor Corp. and will vary in function of board thermal characteristics and other components on the board.

[3] An ambient temperature of 85°C is assumed.

Revision History

Date	Revision	Release Notes
2025-05-28	5.5	Updated the following sections: ● *Inter-IC Sound (I2S)* ● *General Analog-to-digital Converter (ADC)* ● *Cap-Touch Controller (CTC)* ● *General ADC Characteristics*
2025-04-29	5.4	Updated *Pin Assignments* to modify the location of pins
2025-04-03	5.3	● Updated the WLAN feature to support 802.11 ac ● Updated the Bluetooth feature to support ISO ● Updated pin #6/7/42 of RTL8730ELM series and RTL8730ELH series ● Added the power consumption of RTL8730EAH-VD3 ● Updated the feature of *Real-time Clock (RTC) Timer*
2024-10-31	5.2	● Updated *Figure 3-3 Power domains and wakeup sources* ● Updated *Table 3-2 Wakeup sources of power-saving mode*
2024-10-25	5.1	● Updated the maximum frequency of CA32 ● Updated the following sections: ■ *Power Domain* ■ *Power Mode*
2024-09-03	5.0	Added the information of RTL8730EAM-VA6
2024-08-13	4.9	● Updated the features of *WLAN MAC* ● Updated the values of *RF Power Consumption*
2024-06-28	4.8	Updated *General Features*
2024-06-17	4.7	● Updated *Table 4-2 Recommended operation conditions* ● Updated the section: *Power Sequence*
2024-05-31	4.6	● Added the information of RTL8730ELM-VA7 and RTL8730ELM-VA8 ● Updated the following tables: ■ *Table 4-1 Absolute maximum ratings* ■ *Table 4-2 Recommended operation conditions* ■ *Table 4-3 Power sequence specification* ● Updated the section: *Maximum Power Consumption*
2024-04-24	4.5	● Added the following sections: ■ *UART Characteristics* ■ *SDIO Host Characteristics* ● Updated the following sections: ■ *Power Consumption Characteristics* ■ *SPI Characteristics* ■ *I2S Characteristics* ● Updated the CPU frequency of CA32
2024-02-29	4.4	● Added the section: *RSA Engine* ● Updated the section: *Thermal Sensor* ● Updated the typical acceptable voltage of VDH_IO3 of RTL8730ELH
2023-12-22	4.3	● Updated the CPU frequency of CA32 ● Updated the Bluetooth features ● Updated the following sections: ■ *Parameters Definitions* ■ *Absolute Maximum Ratings*
2023-11-22	4.2	● Updated *Table 4-2 Recommended operation conditions* ● Added the information of RTL8730EAH-VH6 instead of RTL8730EAH-VA6
2023-08-08	4.1	Added the information of RTL8730EAH-VD3
2023-07-28	4.0	● Added the following sections: ■ *Power Consumption Characteristics* ■ *RF Characteristics* ■ *MIPI-DSI Characteristics* ■ *QSPI Flash Controller Characteristics* ■ *SPI Characteristics* ■ *I2C Characteristics* ■ *I2S Characteristics* ■ *DMIC Characteristics*

		■ *PDM Characteristics* ■ *Debug Interface Characteristics* ■ *LEDC Characteristics* ■ *USB Interface Characteristics* ■ *Thermal Characteristics* ● Updated the following sections: ■ *Serial Data (SD) Host Controller* ■ *Operation Conditions* ■ *WLAN 2.4GHz Band Transmitter Performance* ■ *WLAN 5GHz Band Transmitter Performance* ■ *Package Outline*
2023-06-02	3.0	● Optimized the content structure of Datasheet ● Updated the section: *Power Management* ● Added sections and values to the chapter: *Electrical Characteristics*
2022-10-17	2.2	Updated the value of b in *Table 5-2 DR-QFN144 package mechanical data*
2022-09-26	2.1	● Updated the section: *WLAN Baseband* ● Updated the section: *DR-QFN144 Package*
2022-07-15	2.0	● Updated *Figure 5-2 DR-QFN144 package outline* ● Updated *Table 5-2 DR-QFN144 package mechanical data*
2022-07-14	1.9	● Updated the pin description of RTL8730ELH: ■ VBUS_OTG pin ■ ID pin ● Updated the description of PSRAM
2022-06-22	1.8	● Update the section: *General Analog-to-digital Converter (ADC)* ● Updated *Figure 3-1 Power block diagram* ● Changed the pin name VBAT_MEAS to BAT_MEAS ● Updated the pin description
2022-05-30	1.7	● Updated the section: *Power Management* ● Updated the pin description
2022-05-01	1.6	● Updated *Figure 3-1 Power block diagram* ● Optimized the pin names for easy understanding
2022-04-15	1.5	● Changed the frequency range of 5G to 5180MHz ~ 5885MHz ● Updated the ordering information
2022-04-07	1.4	● Updated the ordering information ● Updated the information of QFN100 package instead of QFN88 package
2022-03-15	1.3	● Updated *Figure 5-1 QFN100 package outline* ● Added the following sections: ■ *Power Mode* ■ *Power Supply for Pins* ● Updated the section: *Bluetooth Radio Specifications*
2022-02-24	1.2	● Updated the section: *Pin Assignments* ● Updated *Figure 3-5 RF block diagram*
2022-02-18	1.1	● Updated the RF block ● Updated the pin assignment and pin description ● Updated the section: ADC Characteristic ● Updated the PMU block diagram ● Updated the functional description of RCC
2021-10-29	1.0	Initial release