DS0900
RTL8726EA Datasheet

This document provides features and information on RTL8726EA microcontroller.

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This document is intended for the engineer's reference and provides detailed development information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this document.

Contents

Conventions

The following abbreviations apply to indicate the MCUs of Realtek.

Real-M300 (KM4)	Arm® Cortex®-M55 compatible instruction set core based on Armv8.1-M architecture, running at a frequency of up to 400MHz.
KR4	A 32-bit processor supporting RISC-V compatible instruction set RV32IMAFC, running at a frequency of up to 400MHz.
HiFi5 DSP	Cadence® Tensilica® HiFi5 DSP for audio and voice processing, running at a frequency of up to 500MHz.
AP	Application Processor, designed for user application.
NP	Network Processor, designed for network protocol, provides network and power management services to AP.

For most purposes, KM4 and KR4 are interchangeable. That is to say, both of them can work as AP or NP. If one of them is used as AP, the other is regarded as NP.

1 Product Overview

1.1 General Description

The RTL8726EA is a low-power single-chip microcontroller integrating dual RISC cores (Arm® Cortex®-M55 compatible instruction set and RISC-V compatible instruction set) and a digital signal processor (Cadence® Tensilica® HiFi 5 DSP). It is designed for optimized power efficiency, RF performance, and reduced audio transmission latency. It also encompasses the characteristics of low-power chip, including fine-grained clock gating, multiple power modes, and dynamic power scaling.

The KM4 (also called Real-M300) is a 3-staged pipelined 32-bit processor based on Armv8.1-M architecture supporting Cortex-M55 compatible instruction set, running at a frequency of up to 400MHz. It offers system enhancements such as enhanced debug features, single-precision floating-point unit (FPU), Digital Signal Processing (DSP) extension, TrustZone-M security for hardware-enforced isolation, and a high level of support block integration.

The KR4 is a 32-bit processor that supports RISC-V compatible instruction set RV32IMAFC, running at a frequency of up to 400MHz. RISC-V is a standard free and open instruction set architecture (ISA) based on RISC, delivering a new level of free, extensible software and hardware freedom on architecture.

The Cadence Tensilica HiFi 5 DSP is a high-performance embedded DSP optimized for high-performance front-end, far-field and near-field audio and voice processing, running at a frequency of up to 500MHz. It is also designed for enabling efficient implementations of neural network (NN) based speech recognition algorithms. The HiFi 5 DSP is a five-slot VLIW machine which can execute up to eight 32x32-bit MACs per cycle. It can issue two 128-bit loads per cycle, or one load and one store of 128-bit per cycle for parallel loads and stores of the operand and results. The HiFi 5 DSP offers additional floating-point precision support through an optional Single Precision vector floating-point unit (SP FPU), which can perform up to eight single-precision floating-point MACs per cycle. For supporting neural network-based speech recognition algorithms, the HiFi 5 DSP provides Neural Network Extension option which enables the hardware to perform up to thirty-two 8x16, 4x16 and 8x8-bit MACs per cycle.

The RTL8726EA integrates the latest specifications of Wi-Fi (Wi-Fi 6) and Bluetooth (Bluetooth 5.2). It supports 802.11 b/g/n/ax wireless LAN (WLAN) network at 2.4GHz with 20MHz bandwidth. It consists of WLAN MAC, a 1T1R capable WLAN baseband, RF, and Bluetooth, providing complete Wi-Fi and Bluetooth functionalities.

A variety of peripheral interfaces, including UART, SPI, I2C, LEDC, etc., as well as sensor controllers (such as ADC, Cap-Touch, and thermal) are integrated into RTL8726EA. Besides, the RTL8726EA has rich audio features for smart audio applications with dedicated microphone interfaces (AMIC/DMIC), built-in voice activity detection (VAD), acoustic echo cancellation (AEC) reference ADC, mono audio DAC, and I2S. Abundant general-purpose I/O (GPIOs) can be configured to different functions according to different secure IoT (Internet of Things) applications flexibly. The user-friendly development kits (SDK and HDK) are provided to customers for developing applications.

The RTL8726EA also incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash controller provides a flexible and efficient way to access NOR Flash (e.g., byte and block access). A multilayer AXI bus interconnect supports internal and external memory access.

1.2 Block Diagram

The functional block diagram is shown in *Figure 1-1*. This diagram provides a view of the chip's major functional components and core complexes.

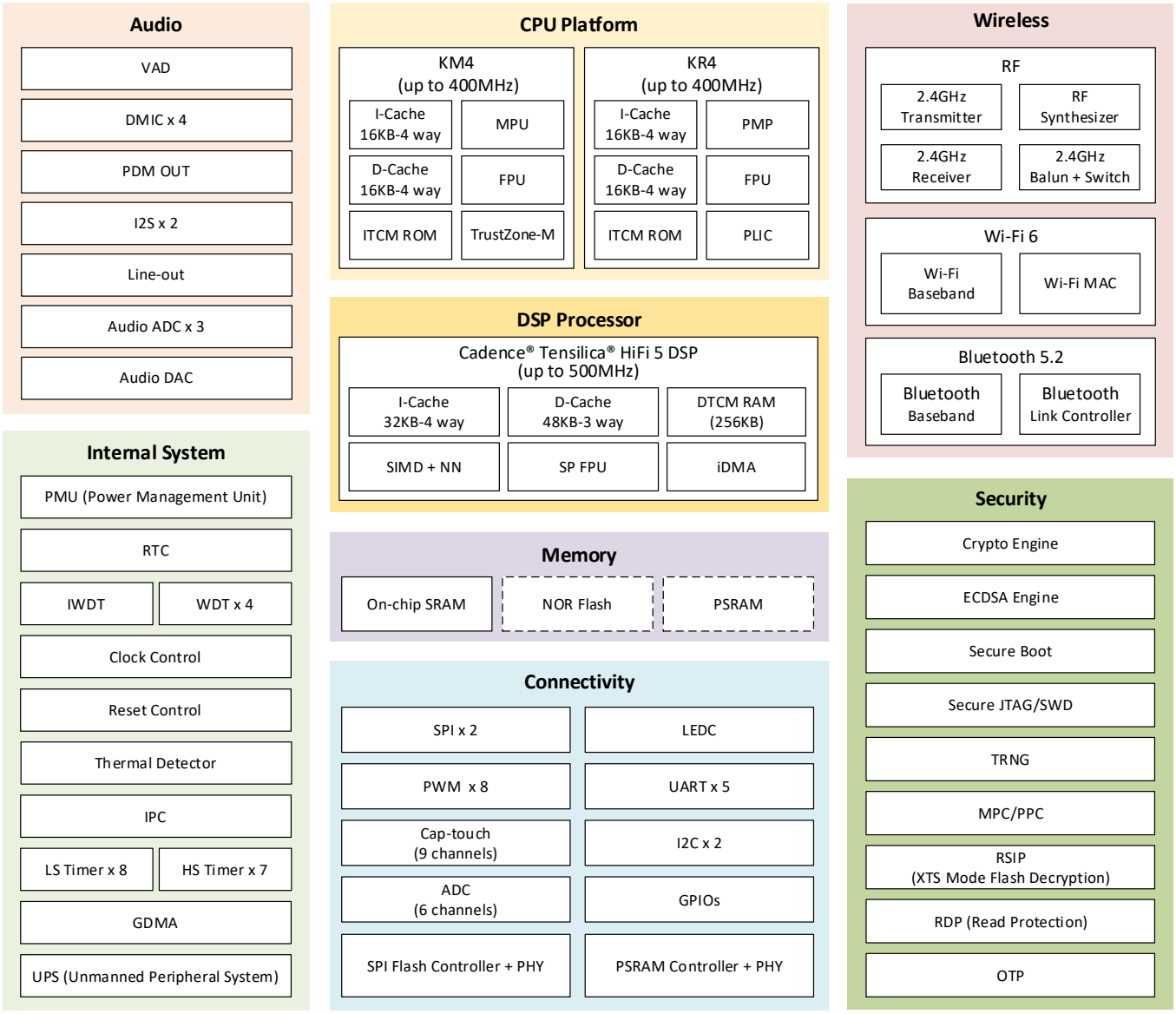


Figure 1-1 Block diagram

1.3 General Features

Table 1-1 General features

Item	Features
Number of Cores	3
KM4 Processor	● Arm Cortex-M55 compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 400MHz ● Memory Protection Unit (MPU) with up to 16 regions per security state ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Single-precision floating point unit (FPU) ● SWD with 8 instruction breakpoints and 1 data watchpoint
KR4 Processor	● RISC-V compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 400MHz ● Single-precision floating point unit (FPU)

	● Platform-Level Interrupt Controller (PLIC) ● Physical Memory Protection (PMP) with up to 16 regions ● Supports 8 trigger points
DSP Processor	● Cadence Tensilica HiFi 5 DSP ■ I-Cache: 32K bytes ■ D-Cache: 48K bytes ■ DTCM RAM: 256K bytes ● Running at a frequency of up to 500MHz ● 5 slot VLIW engine ● 128 bit SIMD support ● Two 128-bit loads store units ● Fixed-point MACs per cycle ■ 32bit x 32bit: up to 8 ■ 24bit x 24bit: up to 8 ■ 32bit x 16bit: up to 16 ■ 16bit x 16bit: up to 16 ■ 16bit x 8bit, 8bit x 8bit, 16bit x 4bit through special NN engine: up to 32 ● Up to 8 single-precision floating-point MACs per cycle
Memory Supported	● On-chip SRAM ● PSARM (optional) ● NOR Flash (optional)
WLAN	● 2.4GHz Wi-Fi 6 (802.11 b/g/n/ax), 1x1 ● Tx power (2.4G): ■ 11b 11Mbps: 20dBm ■ 11g 54Mbps: 19dBm (EVM< −25dB) ■ 11n MCS7-HT20: 18dBm (EVM< −27dB) ■ 11ax MCS9-HE20: 16dBm (EVM< −32dB) ● Rx sensitivity (2.4G): ■ 11b 11Mbps: −91dBm ■ 11g 54Mbps: −78dBm ■ 11n MCS7-HT20: −76.5dBm ■ 11ax MCS9-HE20: −70.5dBm
Bluetooth	● Bluetooth 5.2 specification compliant, dual mode: ■ Bluetooth Basic Rate/Enhanced Data Rate (BR/EDR) ■ Bluetooth Low Energy (BLE) ● Supports both 500kbps and 125kbps LE-Coded PHY (long range) ● Supports scatter-net (concurrent central and peripheral mode) ● Supports SIG Mesh v1.0 and v1.1 ● AoA and AoD (both connection-oriented and connectionless) ● ISO (both CIS and BIS)
RF	Supports antenna diversity
Audio	● Built-in a low-energy Voice Activity Detection (VAD) ● Up to 128KB VAD buffer ● 3-channel Audio ADC, SNR > 98dB A-weighted and THD+N < -80dB ● Mono DAC, SNR > 100dB A-weighted and THD+N < -85dB ● PDM interface function for external speaker AMP ● 4-channel digital microphone interface supported ● I2S x 2 ● Supports up to 8-channel I2S transmitter and receiver by TDM or PCM mode ● Up to 4 serial data outputs/inputs are transmitted within a sample period
Serial Communication	● I2C x 2 ● UART x 5 ● SPI x 2
Package	QFN68, 8mm x 8mm, 0.4mm pitch

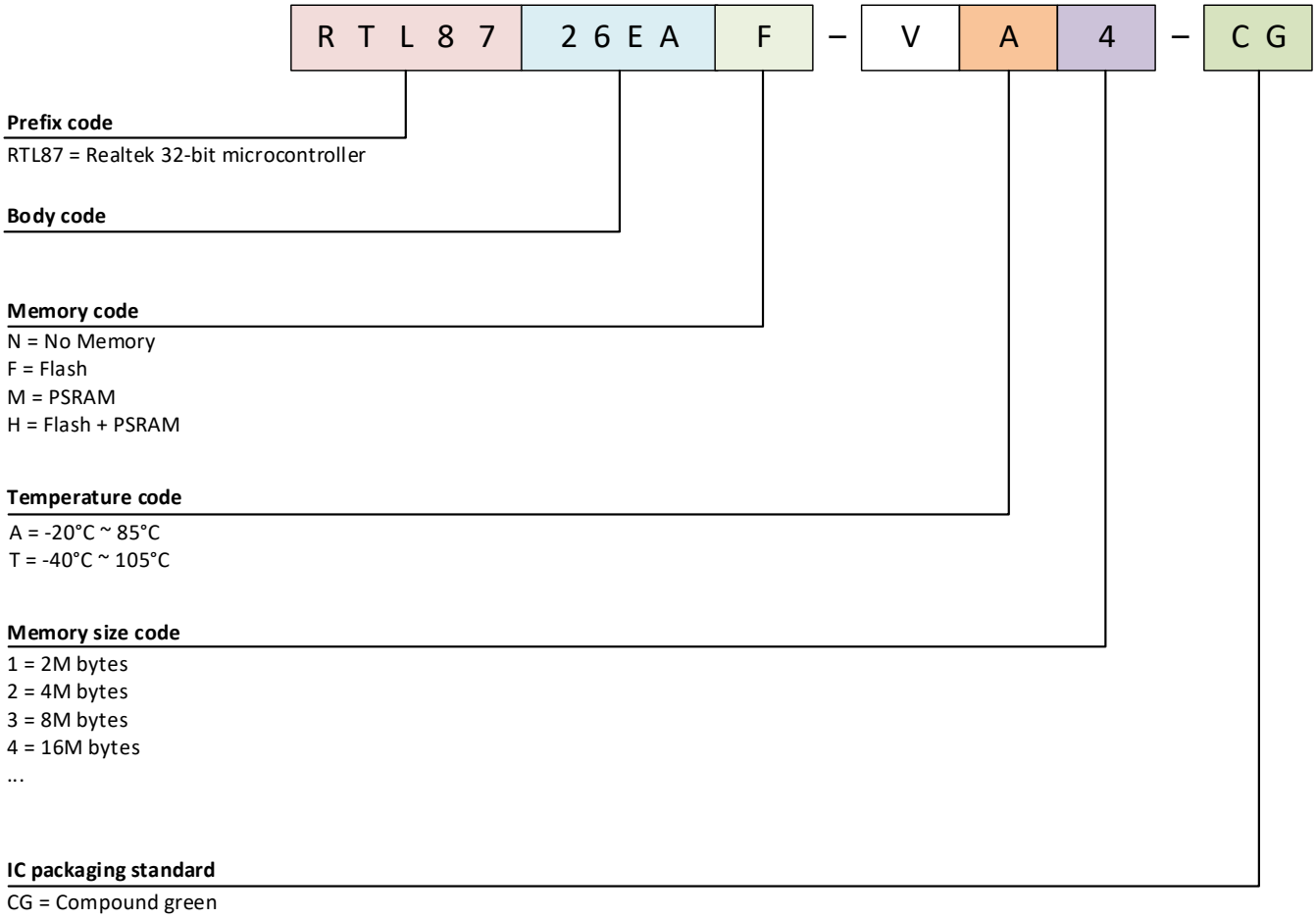
1.4 Target Applications

With dual RISC cores running up to 400MHz, enhanced computing capability, stable security performance and abundant peripheral resources, the RTL8726EA series is widely used in various fields, such as:

- Smart home appliance
- Line controller

- BLE gateway
- Micro inverter
- Portable energy storage
- Home energy storage
- …

1.5 Ordering Information



Part number	Package	Flash	PSRAM	Status
RTL8726EAM-VA4-CG	QFN68	-	16M bytes	

2 Chip Pinout Information

2.1 Pin Assignments

2.1.1 RTL8726EAM Pinout

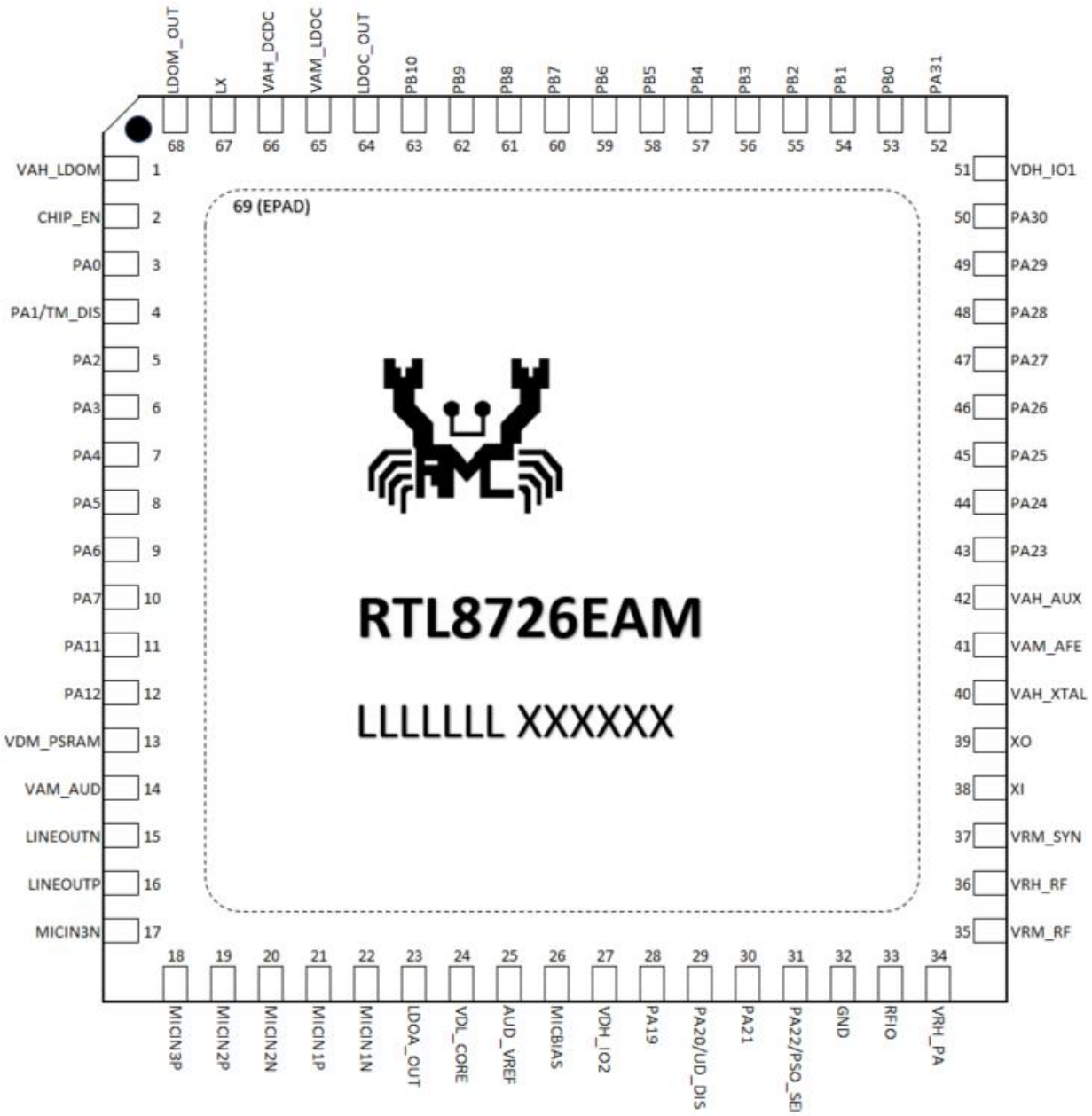


Figure 2-1 Pin assignments of RTL8726EAM series

2.2 Pin Description

The definitions of pin type are listed below:

- I/O: Input/output pin
- A: Analog signal pin
- P: Power supply pin
- G: Ground pin
- RST: Reset pin

Pin No. (RTL8726EAM)	Pin name	Pin type	Default function	Description
1	VAH_LDOM	P	-	Power input for LDOM
2	CHIP_EN	RST	-	Chip enable ● 1: Enable the chip ● 0: Shut down the chip
3	PA0	I/O	GPIO	Wakeup pin This pin should maintain PU during reset. The default function is general-purpose input/output, and it can be configured as other functions.
4	PA1/TM_DIS	I/O	GPIO	Wakeup pin The IC operating mode is determined by the level of trap pin PA1/TM_DIS during the process of power on. ● 1: Normal mode ● 0: Test mode The default function is general-purpose input/output, and it can be configured as other functions.
5	PA2	I/O	Flash Data2	These pins can only be used as Flash-dedicated pins, but not as normal GPIO pins.
6	PA3	I/O	Flash Data1	
7	PA4	I/O	Flash CS	
8	PA5	I/O	Flash Data3	
9	PA6	I/O	Flash CLK	
10	PA7	I/O	Flash Data0	
11	PA11	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
12	PA12	I/O	GPIO	
13	VDM_PSRAM	P	-	Power input for PSRAM
14	VAM_AUD	P	-	Power input for audio codec
15	LINEOUTN	A	Audio LINEOUTN	The default function is audio LINEOUTN function, and it can be configured as other functions after IC boot.
16	LINEOUTP	A	Audio LINEOUTP	The default function is audio LINEOUTP, and it can be configured as other functions after IC boot.
17	MICIN3N	A	Audio MICIN3N	The default function is audio MICIN3N, and it can be configured as other functions after IC boot.
18	MICIN3P	A	Audio MICIN3P	The default function is audio MICIN3P, and it can be configured as other functions after IC boot.
19	MICIN2P	A	Audio MICIN2P	The default function is audio MICIN2P, and it can be configured as other functions after IC boot.
20	MICIN2N	A	Audio MICIN2N	The default function is audio MICIN2N, and it can be configured as other functions after IC boot.
21	MICIN1P	A	Audio MICIN1P	The default function is audio MICIN1P, and it can be configured as other functions after IC boot.
22	MICIN1N	A	Audio MICIN1N	The default function is audio MICIN1N, and it can be configured as other functions after IC boot.
23	LDOA_OUT	P	-	Audio LDO output
24	VDL_CORE	P	-	Power input for digital core domain
25	AUD_VREF	P	-	Reference voltage of Audio Codec AD/DA circuit
26	MICBIAS	A	Audio MICBIAS	The default function is audio MICBIAS, and it can be configured as other functions after IC boot.
27	VDH_IO2	P	-	Power input for digital I/O power domain. Refer to Section *4.8* for more details.
28	PA19	I/O	LOGUART Rx	The default function is LOGUART Rx, and it can be configured as

				other functions after IC boot. If it is configured as a GPIO function, the LOGUART function becomes invalid.
29	PA20/UD_DIS	I/O	LOGUART Tx	The default function is LOGUART Tx, and it can be configured as other functions after IC boot. If it is configured as a GPIO function, the LOGUART function becomes invalid.
30	PA21	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
31	PA22/PSO_SEL	I/O	GPIO	The power supply option is determined by the level of trap pin PA22/PSO_SEL during the process of power-on. Refer to Section *3.1.2* for more details. The default function is general-purpose input/output, and it can be configured as other functions.
32	GND	G	-	To be connected to ground
33	RFIO	A	-	Radio transmitter output and receiver input
34	VRH_PA	P	-	Power input for RF circuit
35	VRM_RF	P	-	Power input for RF circuit
36	VRH_RF	P	-	Power input for RF circuit
37	VRM_SYN	P	-	Power input for RF circuit
38	XI	A	-	Input of 40MHz crystal clock reference
39	XO	A	-	Output of 40MHz crystal clock reference
40	VAH_XTAL	P	-	Power input for XTAL circuit
41	VAM_AFE	P	-	Power input for RF AFE circuit
42	VAH_AUX	P	-	Power input for AUX ADC circuit
43	PA23	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
44	PA24	I/O	GPIO	
45	PA25	I/O	GPIO	
46	PA26	I/O	GPIO	
47	PA27	I/O	GPIO	
48	PA28	I/O	GPIO	
49	PA29	I/O	GPIO	
50	PA30	I/O	GPIO	
51	VDH_IO1	P	-	Power input for digital I/O power domain. Refer to Section *4.8* for more details.
52	PA31	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
53	PB0	I/O	SWD DATA	The default function is SWD DATA, and it can be configured as other functions after IC boot.
54	PB1	I/O	SWD CLK	The default function is SWD CLK, and it can be configured as other functions after IC boot.
55	PB2	I/O	GPIO	The default function is general-purpose input/output, and it can be configured as other functions.
56	PB3	I/O	GPIO	
57	PB4	I/O	GPIO	
58	PB5	I/O	GPIO	
59	PB6	I/O	GPIO	
60	PB7	I/O	GPIO	
61	PB8	I/O	GPIO	
62	PB9	I/O	GPIO	
63	PB10	I/O	GPIO	
64	LDOC_OUT	P	-	Power output of LDOC & Power input for digital core domain.
65	VAM_LDOC	P	-	Power input for LDOC
66	VAH_DCDC	P	-	Power input of DCDC
67	LX	P	-	DCDC output
68	LDOM_OUT	P	-	Power output of LDOM

2.3 Alternate Functions

The RTL8726EA supports two function configuration methods: dedicated function and full-matrix function.

- For the dedicated function, the function ID is from 0 to 17. Each ID corresponds to a specific function. Only some pins configured with a function ID can be connected to the fixed signal of the corresponding function. Other pins that are not assigned this function will be invalid even if they are configured with a function ID.
- For the full-matrix function, the function ID is from 20 to 67. Each pin of PA8 ~ PA31, PB0 ~ PB10 can be configured as a function ID 20~67 (only if the corresponding value of the pin under the function ID in the PINMUX table is displayed as 1). Each function ID corresponds to a certain signal of a specific function.

Compared with the dedicated function, the full-matrix function is not limited to a few specific pins when used, which increases flexibility and provides more combinations. But at the same time, the timing performance of the full-matrix function will be worse than that of the dedicated function. For specific usage restrictions, refer to the relevant content of interface timing in Chapter *Electrical Characteristics*.

Each GPIO of RTL8726EA can be flexibly used for different functions through software configuration according to the specific usage requirements.

For the configurable functions on each GPIO, refer to *UM0902_RTL8726EA_pin_mux.xls*.

2.4 Power Supply for Pins

Several GPIO pins belong to a specific power supply group. Each power pin may be supplied at different voltage levels as needed by the application, and can be powered by 1.8V or 3.3V according to different packages.

Refer to *UM0902_RTL8726EA_pin_mux.xls* for more details on power supply pins.

3 Functional Description

3.1 Power Management

3.1.1 Power Structure

Only an external typical 3.3V power supply is required for the RTL8726EA; all the other required voltages can be converted and output by embedded three low-dropout regulators (LDO) and one DC-DC switching regulator (DCDC). The recommended power on off sequence can be found in Section *Power Sequence*.

There are two options for power supply, the block diagrams are summarized in *Figure 3-1* and *Figure 3-2*.

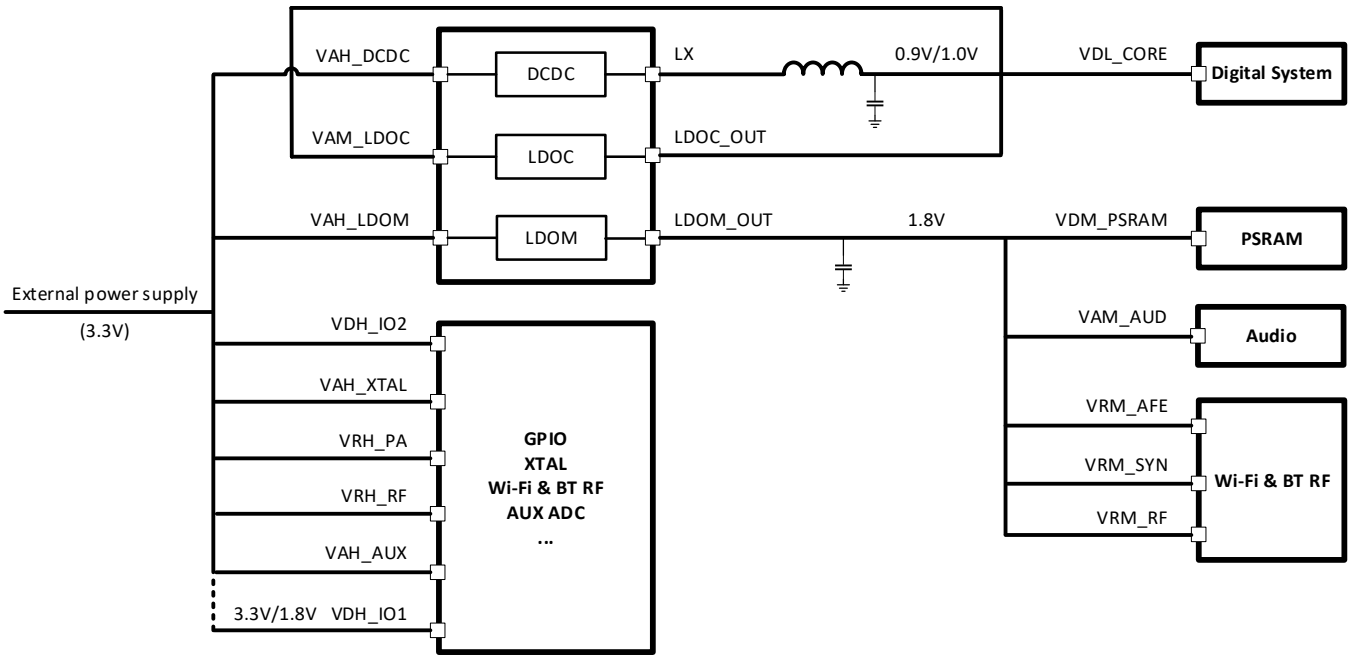


Figure 3-1 Power structure (power supply option 1)

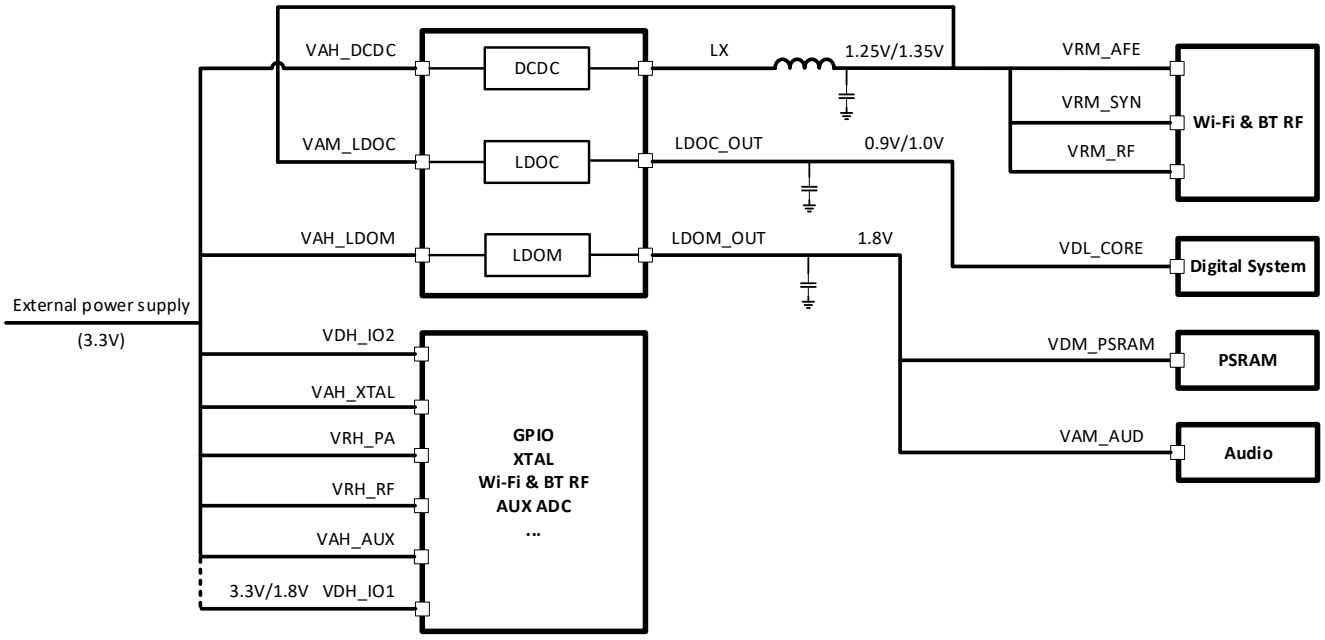


Figure 3-2 Power structure (power supply option 2)

The power supply option is determined by the level of trap pin PSO_SEL during the process of power on. The peripheral circuit needs to match the level of trap pin PSO_SEL to prevent damage to the circuits.

Table 3-1 Power supply option details

PSO_SEL	Power supply option	Power supply	
Low level	Option 1	DCDC	DCDC outputs typical 0.9V or 1.0V, which is controlled by software based on application requirements, for digital core circuits.
		LDO core (LDOC)	LDOC is not used but its input and output pins are connected to 0.9V or 1.0V for leakage consideration.
		LDO memory (LDOM)	LDOM outputs typical 1.8V for PSRAM, Audio Codec and RF circuits.
High level	Option 2	DCDC	DCDC outputs typical 1.25V or 1.35V for RF circuits and LDOC input.
		LDO core (LDOC)	LDOC outputs typical 0.9V or 1.0V for digital core circuits.
		LDO memory (LDOM)	LDOM outputs typical 1.8V for PSRAM and Audio Codec circuits.

The difference between option 1 and option 2 is the power supply solution for digital core and Wi-Fi & BT RF circuits.

- If the digital core circuit is the main power consumption circuit in the application scenario, it is recommended to choose option 1 to achieve a lower overall power.
- If the Wi-Fi & BT RF circuit is the main power consumption circuit, option 2 is recommended to achieve a lower overall power.

3.1.2 Power Supply Supervisor

The RTL8726EA has integrated a power-on reset (POR) circuit and a brownout detect (BOD) circuit.

3.1.2.1 Power-on Reset (POR)

The POR supervisor monitors VAH_LDOM power supply input during power-on and power-off.

- When VAH_LDOM is higher than V_{POR_H}, the chip releases the internal reset.
- When VAH_LDOM is lower than V_{POR_L}, the chip remains in reset mode.

Refer to Section *Power Sequence* for more details.

3.1.2.2 Brownout Detect (BOD)

The BOD supervisor monitors VAH_LDOM power supply input. The BOD circuit is disabled by default and can be enabled by setting the register. The BOD circuit can work in reset mode or interrupt mode and has independent falling threshold V_{BOD_L} and rising threshold V_{BOD_H}.

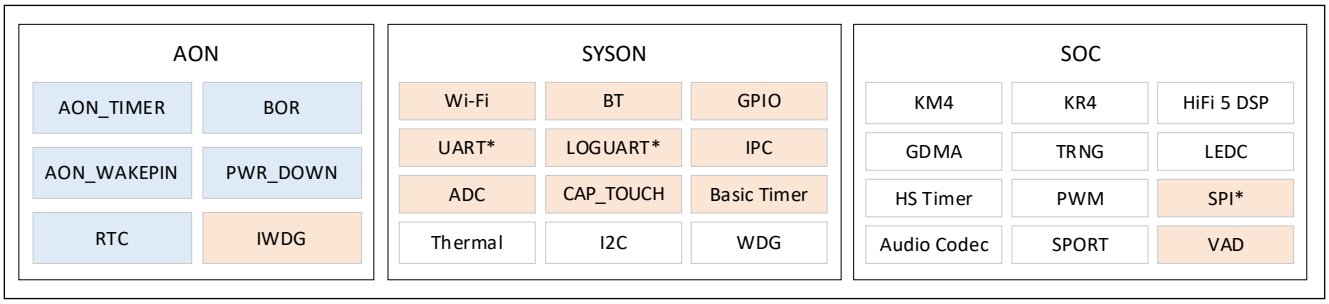
- When VAH_LDOM drops below V_{BOD_L}, the BOD circuit will trigger an interrupt or a reset depending on the register configuration.
- When VAH_LDOM rises above V_{BOD_H}, the BOD circuit will release the internal reset. V_{BOD_L} and V_{BOD_H} can be chosen by setting the register, but V_{BOD_H} must be set higher than V_{BOD_L}.

Refer to Section *Power Sequence* for more details.

3.1.3 Power Domain

There are different power domains in the RTL8726EA, and AON, SYSON, and SOC are three main power domains in the digital system. Users can flexibly power up different power domains to achieve the best balance between the performance and power consumption. Functions in different power domains will be turned off differently in different power-saving modes. More information about power domains and wakeup sources are depicted in *Figure 3-3*.

Some peripherals (such as UART, LOGUART, …) can only wake up the system under some special conditions, refer to *Table 3-3* for more details.



The peripheral on AON domain can be a wakeup source from deep-sleep mode.
The peripheral on different power domains can be a wakeup source from sleep mode.
* The peripheral can only wake up the system under some special conditions.

Figure 3-3 Power domains and wakeup sources

3.1.4 Power Mode

By controlling the power and clock of individual functions, the RTL8726EA can support both active mode and power saving mode.

There are two special power-saving modes, sleep mode and deep-sleep mode, which are to achieve low power consumption with different peripherals running.

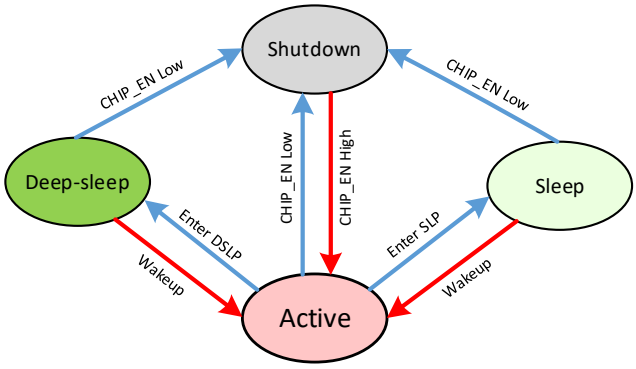


Figure 3-4 Switch among different power modes

3.1.4.1 Active Mode

In active mode, all the digital modules are powered on. Each of them can be configured as active or clock-gated, depending on the application requirement. In addition, there are individual power-down controls for some of the analog peripherals.

3.1.4.2 Sleep Mode

In sleep mode, most of the functions are powered off or clock-gated to save power.

Two kinds of peripherals can be configured to continue operating.

- One kind is the peripherals, which can be used as wakeup sources. Any interrupt/event can trigger the peripheral to wake up the system.
- The other kind is the peripherals, which are needed to keep the wireless link alive. The system memory can be optionally set to retention mode, so that the system can wake up quickly without reloading content from Flash.

3.1.4.3 Deep-sleep Mode

In deep-sleep mode, all functions are powered off except the AON functions. This is to achieve ultra-lower power consumption. The system can only be woken up by the interrupt/event generated from AON domain. When exiting from the deep-sleep mode, the system will go through normal boot flow.

3.1.4.4 Wakeup Source

Table 3-2 shows typical power modes supported by RTL8726EA, which is a non-exhaustive list.

Table 3-2 Power modes

Function		Power mode				
		Shut down	Deep-sleep	Sleep		Active
				Power gating	Clock gating	
WLAN		OFF	OFF	Software configurable	Software configurable	Software configurable
Bluetooth		OFF	OFF	Software configurable	Software configurable	Software configurable
Processors + Cache		OFF	OFF	OFF	Clock gating	ON
SRAM		OFF	OFF	Retention	Retention	ON
Security		OFF	OFF	OFF	OFF	ON
VAD		OFF	OFF	Software configurable	Software configurable	Software configurable
AON	RTC	OFF	ON	ON	ON	ON
	AON_GPIO	OFF	ON	ON	ON	ON
SYSON	GPIO	OFF	OFF	Software configurable	Software configurable	Software configurable
	Timer	OFF	OFF	Software configurable	Software configurable	Software configurable
	ADC	OFF	OFF	Software configurable	Software configurable	Software configurable
	Cap-Touch	OFF	OFF	Software configurable	Software configurable	Software configurable
	UART	OFF	OFF	Software configurable	Software configurable	Software configurable

Table 3-3 lists the wakeup sources of power-saving mode.

Table 3-3 Wakeup sources of power-saving mode

Power-saving mode	Wakeup source	Restriction
Sleep mode	WLAN	
	BT	
	IWDG	
	IPC	
	Basic Timer	
	UART	● When using UART as a wakeup source, if the Rx clock source is XTAL40M, do not turn off XTAL during sleep. ● The portion of the command used to wake up that exceeds the FIFO depth (64B) will be lost.
	LOGUART	● When using LOGUART as a wakeup source, if the Rx clock source is XTAL40M, do not turn off XTAL during sleep. ● The portion of the command used to wake up that exceeds the FIFO depth (16B) will be lost.
	GPIO	
	SPI	● When using UART as a wakeup source, do not turn off the power and clock of SOC domain. ● Only when the NP core is active and AP core is sleep, NP can use the SPI to wake up AP.
	CAP_TOUCH	
	ADC	
	VAD	
Deep-sleep mode	AON_TIMER	
	AON_WAKEPIN	
	RTC	
	BOR	
	PWR_DOWN	

3.2 Reset and Clock Control (RCC)

The RCC module manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides high flexibility in the choice of clock sources and allows the application of clock ratios to improve power consumption.

3.2.1 Reset Control

3.2.1.1 Reset Diagram

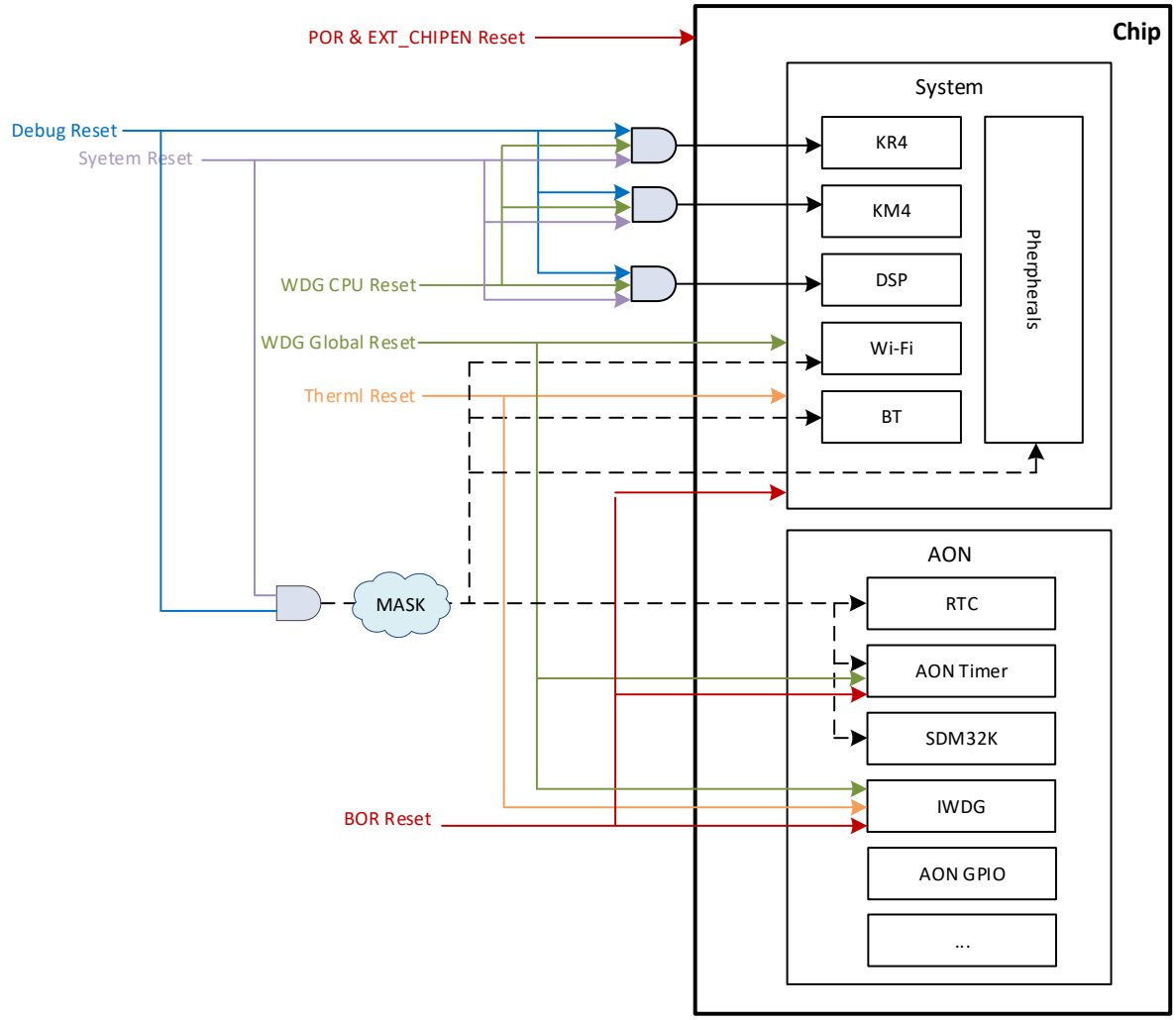


Figure 3-5 Reset diagram

3.2.1.2 Reset Type

The following reset sources or events can generate a reset.

Table 3-4 Reset types

Reset type	Description
POR	A regulator power-on reset is generated when power on
BOR	A regulator brownout reset is generated when BOR detected
EXT_POR	An external power-on reset is generated when external power on
WDG Global	A global reset is generated when watchdog timeout
WDG	CPU reset is generated when watchdog timeout or abnormal feed watchdog
THM	A thermal reset is generated when an abnormal temperature detected
SYSRST	Triggered by software

3.2.1.3 Reset Domain

Different reset types reset different domains:

- Regulator Power-on reset (POR) and External CHIP_EN reset (EXT_POR) can reset the whole chip.
- System reset is triggered by software.
- A watchdog reset is generated when watchdog timeout or abnormal feed watchdog. Watchdog reset can be divided into watchdog CPU reset and watchdog global reset. Watchdog CPU reset only resets the specific CPU, while watchdog global reset can reset most of the system. IWDG can only trigger global reset, and the system watchdog can trigger both CPU reset and global reset according to different configurations and circumstances.
- A thermal reset is generated when abnormal temperature detected. Thermal reset can reset the system and IWDG of AON domain.

3.2.2 Clock Control

The clock sources of this chip are listed below. Different clock sources can drive different functions.

- External oscillators:
  - XTAL40M: used for peripherals directly or after frequency division.
- Internal oscillators:
  - OSC4M: provides 4MHz clock for lbus, and 2MHz clock for peripherals after frequency division.
  - OSC131K: used for input of SDM and other peripherals.
  - OSC100K: resides in the AON domain and used for driving the IWDG.
- Separate PLLs: each of them can be configured with integer or fractional ratios.
  - DSP_PLL: 300MHz~600MHz, provides clock for HiFi 5 CPU, HiFi 5 bus, and TRNG.
  - CPU_PLL: 300MHz~600MHz, provides clock for KM4 CPU, and peripherals after frequency division.
  - FLASH_CPU_PLL: same frequency different phase with CPU_PLL
  - FLASH_DSP_PLL: same frequency different phase with DSP_PLL
  - FLASH_CPU_PLL_PS: for SPI controller power-saving
  - FLASH_DSP_PLL_PS: for SPI controller power-saving
  - One PLL dedicated for Wi-Fi: 320MHz

3.3 CPU Architecture

There are three processors in RTL8726EA for different purposes, which are KM4, KR4, and HiFi 5.

For most purposes, KM4 and KR4 are interchangeable. That is to say, both of them can work as application processor (AP) or network processor (NP). If one of them is used as AP, the other is regarded as NP. HiFi 5 is a DSP processor which is dedicated for AI speech and audio processing.

The boot sequence always starts from KM4. After KM4 boots up, it will decide whether to bring up the other two processors for execution.

3.3.1 KM4 Processor

The KM4 is a 3-staged pipelined 32-bit processor that bases on Armv8.1-M architecture supporting Cortex-M55 compatible instruction set, and offers system enhancements such as low power consumption, enhanced debug features, floating-point computation, TrustZone-M security for hardware-enforced isolation, and a high level of support block integration. It achieves an optimal blend between real-time determinism, energy efficiency, software productivity, and system security that opens the door for many new applications and opportunities across diverse markets.

The KM4 processor has the following features:

- Armv8.1-M architecture
- 3-stage pipeline to support the clock frequency of up to 400MHz
- Thumb/Thumb-2 technology
- TrustZone-M technology for Armv8-M, with Security Attribution Unit (SAU) of up to 8 regions
- 16K bytes I-Cache, 16K bytes D-Cache
- Single-precision floating point unit (FPU)
- Memory Protection Unit (MPU) with up to 16 regions per security state
- Non-maskable Interrupt (NMI) and physical interrupts with 8 to 256 priority levels
- Waking up the processor from state retention power gating or when all clocks are stopped
- Integrated wait for event (WFE) and wait for interrupt (WFI) instructions
- JTAG and Serial Wire Debug ports, up to 8 instruction breakpoints and 1 data watchpoint

The KM4 is designed to run up to 300MHz at 0.9V and 400MHz at 1.0V.

3.3.2 KR4 Processor

The KR4 is a 32-bit processor that supports RISC-V compatible instruction set RV32IMAFC. RISC-V is a standard free and open instruction set architecture (ISA) based on RISC, delivering a new level of free, extensible software and hardware freedom on architecture.

The KR4 processor has the following features:
- RISC-V compatible instruction set
  - I-Cache: 16K bytes
  - D-Cache: 16K bytes
- Running at a frequency of up to 400MHz
- Equipped with FPU for better floating point capability
- Platform-Level Interrupt Controller (PLIC)
- Physical Memory Protection (PMP) with up to 16 regions
- Supports 8 trigger points

The KR4 is designed to run up to 300MHz at 0.9V and 400MHz at 1.0V.

3.3.3 HiFi 5 DSP

The Cadence Tensilica HiFi 5 DSP is a high-performance embedded DSP optimized for high-performance front-end, far-field and near-field audio and voice processing, running at a frequency of up to 500MHz. It is also designed for enabling efficient implementations of neural network (NN) based speech recognition algorithms. The HiFi 5 DSP is a five-slot VLIW machine that can execute up to eight 32x32-bit MACs per cycle. It can issue two 128-bit loads per cycle, or one load and one store of 128-bit per cycle for parallel loads and stores of the operand and results. The HiFi 5 DSP offers additional floating-point precision support through an optional single-precision n vector floating-point unit (SP FPU), which can perform up to eight single-precision floating-point MACs per cycle. For supporting neural network-based speech recognition algorithms, the HiFi 5 DSP provides Neural Network Extension option which enables the hardware to perform up to thirty-two 8x16, 4x16 and 8x8-bit MACs per cycle.

It supports generic MAC, vector FPU, and NN functions.

The key features of HiFi 5 DSP include:
- 32K bytes I-Cache, 48K bytes D-Cache
- 256K bytes DTCM RAM, no ROM
- 5 slot VLIW engine
- 128 bit SIMD support
- Two 128-bit loads store units
- Fixed-point MACs per cycle
  - 32 bit x 32 bit: up to 8
  - 24 bit x 24 bit: up to 8
  - 32 bit x 16 bit: up to 16
  - 16 bit x 16 bit: up to 16
  - 16 bit x 8 bit, 8 bit x 8 bit, 16 bit x 4 bit through special NN engine: up to32
- Up to 8 single-precision floating-point MACs per cycle

The HiFi 5 DSP is designed to run up to 400MHz at 0.9V and 500MHz at 1.0V.

3.4 Memory

The RTL8726EA incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash memory controller provides a flexible and efficient way to access NOR Flash (e.g., byte and block access). A multilayer AXI interconnect supports internal and external memory access.

The memory of RTL8726EA consists of four types:
- ROM
- SRAM
- Flash
- PSRAM

3.4.1 ROM

All three processors share the same memory map for SRAM, Flash and PSRAM, except ROM. The ROM has special handling.

- HiFi 5 DSP does not have ROM.
- The ROM address of KM4 and KR4 is the same from 0x0000_0000 to 0x0007_FFFF. However, KM4 and KR4 have physically separated internal ROMs, and each CPU can only access its own ROM.

3.4.2 SRAM

The on-chip SRAM consists of three blocks:

- A specific high-speed 256KB data SRAM (DTCM) for HiFi 5 DSP
- A general purposed on-chip 512KB SRAM for system heap and application
- A dedicated connectivity SRAM shared with Wi-Fi and Bluetooth (lower protocol stack)

All of the SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits) by processors, DMA engine and other AXI masters.

The entire SRAM can be disabled or enabled in the Power Management Unit (PMU) to save power, and can also enter retention mode for quickly resuming from sleep mode when the system enters sleep mode.

3.4.3 Flash

The Flash memory consists of a SPI Flash controller and a Flash memory array module. The SPI Flash controller acts as an interface between the system bus and the Flash memory device. It implements the erase and program Flash memory operations, and the read/write protection mechanisms, and accelerates code execution with a system of instruction prefetch and cache lines.

The SPI Flash controller of RTL8726EA supports SPI NOR Flash with Single/Dual/Quad I/O pins. The I/O voltage is 3.3V. It can run up to 100MHz Single Data Rate (SDR) speed.

3.4.4 PSRAM

The PSRAM controller of RTL8726EA supports high-speed hyperbus PSRAM with Double Data Rate (DDR) and 1.8V I/O voltage.

- Clock rate: up to 250MHz
- 8-bit I/O
- Supports half-sleep and deep power-down mode

3.5 RF Subsystem

3.5.1 RF Block Diagram

The Radio Frequency (RF) block diagram of RTL8726EA, including WLAN and BLE modem, is given in *Figure 3-6*.

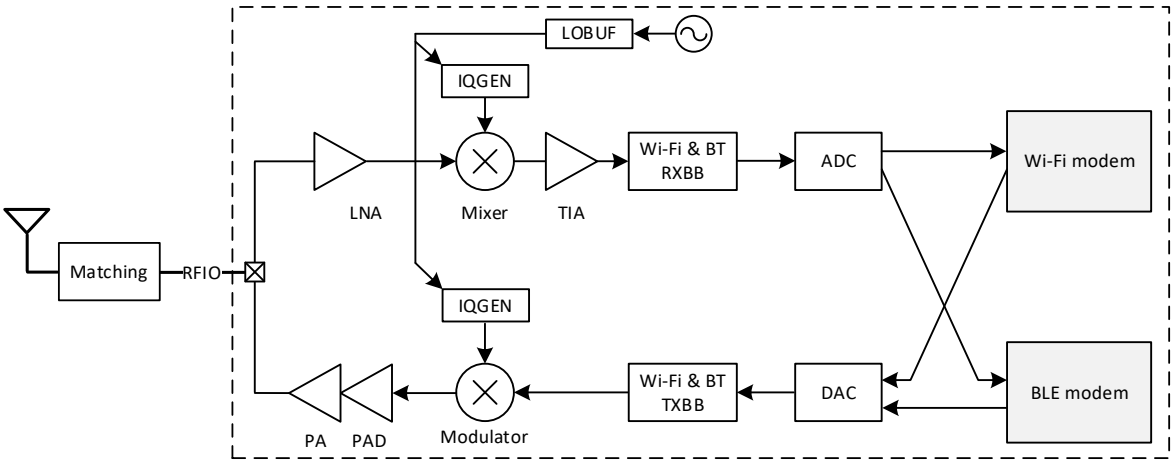


Figure 3-6 RF block diagram

3.5.2 WLAN

3.5.2.1 WLAN Receiver

The RTL8726EA has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. At RFIO port, an on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN 2.4G receivers. Because the NF of receiver path is lower enough, external LNA is not necessary, which can increase the receive sensitivity no more than 1dB.

3.5.2.2 WLAN Transmitter

The Baseband data is modulated and up-converted to the 2.4 GHz ISM band. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11 b/g/n/ax specifications without the need for external PAs.

3.5.2.3 Real-time Calibration

The RTL8726EA adopts real-time and automatic on-chip calibration mechanisms to ensure that normal radio system can operate perfectly, and users do not need to do extra operations to enhance Tx/Rx performance. These calibration mechanisms that are merged into software or hardware continually compensate for temperature and process variations across components. Examples of some of these algorithms are digital correction, such as:

- I-Q compensation calibration
- Digital pre-distortion calibration for good EVM performance of the transmitter
- LO calibration for carrier leakage reduction

3.5.3 Bluetooth

3.5.3.1 Bluetooth Transceiver

The fully integrated radio transceiver is compliant with Bluetooth SIG test specification, and designed for low power consumption, excellent transmit and receive performance in the ISM band.

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy (BLE)
- Integrated 32K oscillator for power management

3.5.3.2 Bluetooth Transmitter

The modulator translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

3.5.3.3 Bluetooth Receiver

The LNA amplifies a low energy RF signal to the desired level without significantly increasing the noise power. When input power is high, the design limits non-linearity. The Receive mixer is a device whose input is an RF signal, and the output is an IF signal. The IF signal is then passed along the IF path to the demodulator.

3.6 WLAN Subsystem

3.6.1 WLAN Baseband

The RTL8726EA is designed to support 802.11 b/g/n/ax single-stream WLAN. The PHY has implied efficient algorithms to provide high throughput and enhanced sensitivity, including advanced algorithms for DC, frequency and timing offset estimation, adaptive frequency domain equalizer, and a Viterbi decoder.

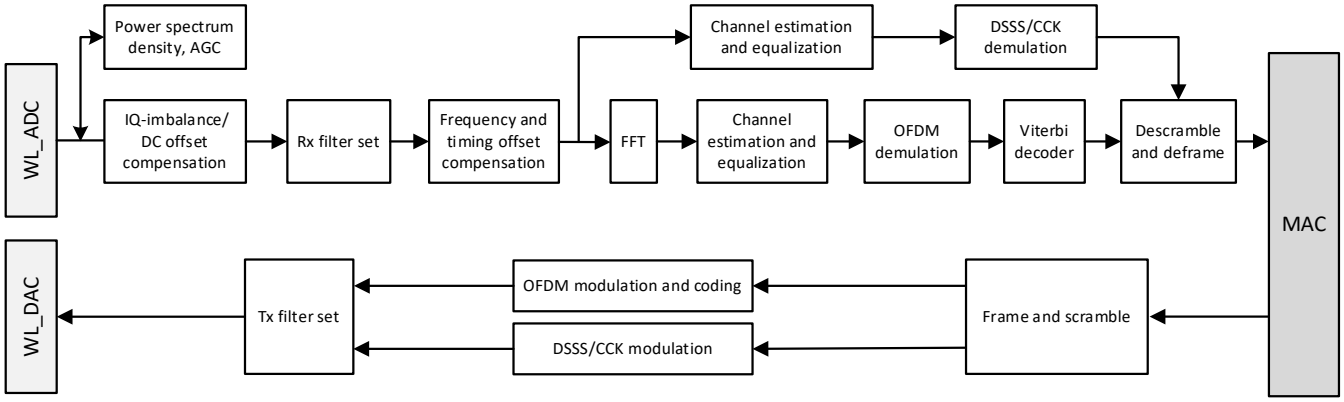


Figure 3-7 PHY block diagram

The WLAN baseband of RTL8726EA supports the following features:

- 802.11 b/g/n/ax
- 802.11n MCS0-7, 20MHz bandwidth, up to 72.2Mbps of data rate
- 802.11ax MCS0-9, 20MHz bandwidth, up to 114.7Mbps of data rate
- Integrated 2.4GHz PA and LNA, and T/R switch
- Integrated 2.4GHz balun
- Supports both internal and external PA
- Adjustable transmitting power
- Supports Channel State Info (CSI)
- Supports Tx Low-density Parity Check (LDPC), Tx Binary Convolutional Code (BCC), and Rx BCC
- Supports Rx STBC 2x1
- Supports SU/MU Beamformee
- Supports Rx DL-OFDMA, Tx UL-OFDMA
- Supports 802.11ax DCM/ER Tx/Rx
- Supports Spatial Reuse
- Short guard interval
- Supports digital pre-distortion to enhance PA performance
- Smoothing for channel estimation
- Antenna diversity

The RTL8726EA supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and select the best antenna to minimize the effects of channel fading.

3.6.2 WLAN MAC

The WLAN Media Access Control (MAC) of RTL8726EA applies low-level protocol functions automatically. It supports the following features:

- Frame aggregation for increased MAC efficiency (A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- Power-saving mechanism
- Target Wake Time (TWT) function for power saving
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- Enhanced Distribution Channel Access (EDCA) and MU EDCA
- Transmitting beamforming as beamformee
- Supports 2 Network Allocation Vector (NAV)
- Supports Basic Service Set (BSS) color
- Supports Time Synchronization Function (TSF) auto-sync
- IEEE 802.11i (WPA, WPA2, WPA3), open, shared key, and pair-wise key authentication services
- Rx trigger frame (except GCR MU-BAR and NFRP)
- Supports AP/STA/Concurrent mode (802.11ax AP not supported)
- Supports Multi Channel Concurrent (MCC) mode by software TDMA

3.7 Bluetooth Subsystem

The RTL8726EA integrates a hardware link layer controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

3.7.1 Bluetooth Baseband

The Bluetooth baseband of RTL8726EA supports the following features:

- Compliant with Bluetooth Core Specification including BR/EDR/LE-1M/LE-2M/LE-Coded PHY (long range)
- Fully integrated balun and synthesizer minimize external components
- 40MHz main clock
- Supports serial Flash for firmware storage and parameter upgrade
- Adaptive Frequency hopping (AFH)

3.7.2 Bluetooth Link Controller

- Bluetooth 5.2 specification compliant, dual mode:
  - Bluetooth Basic Rate/Enhanced Data Rate (BR/EDR)
  - Bluetooth Low Energy (BLE)
- Supports all packet types in BR/EDR
- High-speed UART interface for Bluetooth data transmission
- Integrated MCU to execute Bluetooth protocol stack
- Supports Secure Simple Pairing
- Enhanced Bluetooth/WLAN Co-existence Control to improve transmission quality in different profiles
- Supports BLE 5.2 Connection Isochronous Channel
- Supports multiple Low Energy states

3.8 Security

The RTL8726EA is designed to safely hold security-related data such as cryptographic keys and general-purpose security information with the following security techniques.

- Secure boot
- Arm TrustZone-M
- True Random Number Generator (TRNG)
- Hardware crypto engine
- ECDSA engine
- Whole or partial Flash encryption
- Read Protection (RDP)
- JTAG/SWD password protection/forbidden
- 2K bytes OTP, up to 2K bits for users

3.8.1 Secure Boot

Secure boot aims at firmware protection, which prevents attackers from modifying or replacing firmware maliciously. When the chip is powered on, the secure boot ROM executes to check the validity of the image signature.

The RTL8726EA supports the following algorithms of secure boot:

- Signing/Authentication algorithm:
  - Ed25519 (software only)
  - ECDSA
- Hash algorithm:
  - SHA
  - HMAC

3.8.2 Elliptic Curve Signature Algorithm (ECDSA)

The ECDSA implements a complete asymmetric (public/private) key cryptographic signature solution based upon Elliptic Curve Cryptography and the ECDSA signature protocol. The device features hardware acceleration for the NIST standard SECP256K1 and P256 prime curve including ECDSA signature generation, ECDH key agreement, and ECDSA public-key signature verification. The processing of it is faster than software.

It has the following features:

- Supports the following Elliptic Curves and all other Elliptic Curves with N no more than 256 bits
  - ECDSA_ECP_SECP192R1
  - ECDSA_ECP_SECP224R1
  - ECDSA_ECP_SECP256R1
  - ECDSA_ECP_BP256R1
  - ECDSA_ECP_CURVE25519
  - ECDSA_ECP_SECP192K1
  - ECDSA_ECP_SECP224K1
  - ECDSA_ECP_SECP256K1
- Two private keys in OTP can only be accessed by hardware engine.
- Performance: about 3.5ms for signature verification which is much faster than software

3.8.3 Hardware Crypto Engine (IPsec)

The RTL8726EA integrates two hardware crypto engines: SHA engine and AES engine, which can accelerate applications that need cryptographic functions, such as authentication, encryption and decryption. Hardware crypto engines executing these functions cannot only reduce software overhead but also save CPU and memory resources, and the processing is more secure and faster than software.

The IPsec provides basic cryptographic features:

- Authentication algorithms
  - General cryptographic hash function
    - MD5 (weak, not recommended)
    - SHA1 (weak, not recommended)
    - SHA2-224
    - SHA2-256
    - SHA2-384
    - SHA2-512
  - HMAC (Hash-based message authentication code)
    - HMAC_MD5 (weak, not recommended)
    - HMAC_SHA1 (weak, not recommended)
    - HMAC_SHA2-224
    - HMAC_SHA2-256
    - HMAC_SHA2-384
    - HMAC_SHA2-512
- Cipher (Encryption/Decryption) algorithms
  - AES-128/192/256
    - ECB (Electronic Codebook) mode (weak, not recommended)
    - CBC (Cipher Block Chaining) mode
    - OFB (Output Feedback) mode
    - CFB (Cipher Feedback) mode
    - CTR (Counter) mode (weak, not recommended)
    - GCM (Galois/Counter Mode) mode
- Four keys in OTP, two for secure mode and two for non-secure mode. The keys can be configured by software, or read from OTP by hardware engine.

3.8.4 Secure Image Protection (RSIP)

Generally, both firmware and some data are stored in Flash memory. The SPI Flash controller is used to transmit/receive data from/to SPI Flash memory. In order to protect firmware, the code and data in Flash can be encrypted with Advanced Encryption Standard (AES) algorithm. The RSIP is mainly used for MMU and image decryption.

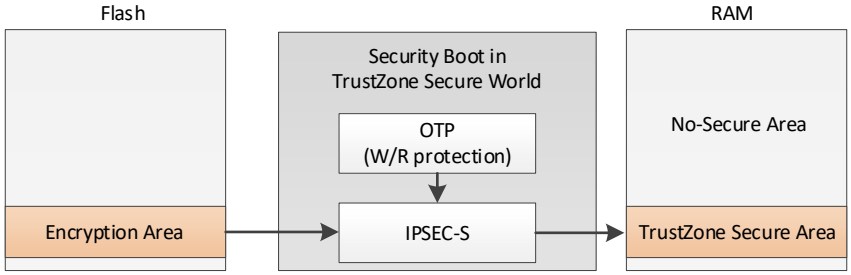
The RSIP consists of two parts:

- RSIP-AES: performs Flash decryption on the fly.
- RSIP-MMU: used for virtual-to-physical memory address translation.

The RSIP-AES has the following features:
- The whole or part of Flash can be encrypted.
- Encrypted Flash data is decrypted by hardware engine on the fly.
- Optional crypto algorithm: AES-256 CTR mode and XTS mode.
- Key length is 256 bits, which should be programmed into OTP, and can be set to Read Protection and Write Protection.
- IV length is 128 bits, the higher 64 bits can be defined by users, and the lower 64 bits are decided by the address.
- Keys are auto-loaded to hardware engine; software cannot access them after read protection is enabled.
- Keeps 8 IVs in the engine, and each of eight entries can choose a different IV and mode independently to enable decryption for specific areas.

3.8.5 Read Protection (RDP)

Read Protection (RDP) is used to protect security-critical code, which is implemented with Arm TrustZone technology. The security-critical code is stored in the Flash with encrypted form, and would be decrypted in secure bootloader and loaded into secure SRAM protected by TrustZone.



3.8.6 True Random Number Generator (TRNG)

The TRNG of RTL8726EA is a true random number generator that provides full entropy outputs to the application as 32-bit samples.

It has the following features:
- Delivers 32-bit true random numbers, produced by an analog entropy source
- Embeds with a health test unit and an error management unit
- Two independent FIFOs, the secure one has a higher priority
- Throughput of the TRNG is up to about 2Mbps

3.9 Timers and Watchdogs

The RTL8726EA includes 13 basic timers, one capture timer, one PWM timer, also a RTC timer, a debug timer and several watchdog timers.

Table 3-5 Timer feature comparison

Type	Number	Counter resolution	Counter mode	Prescaler	INT generation	Sleep mode	Secure mode
Basic timer	13	32-bit	Up	×	✓	✓	✓
Capture timer	1	16-bit	Up	16-bit	✓	×	✓
PWM timer	1	16-bit	Up	16-bit	✓	×	✓

3.9.1 Basic Timer (TIM0 ~ TIM7, TIM10 ~ TIM14)

The RTL8726EA has 13 basic timers:
- TIM0, TIM1, TIM2, TIM3, TIM4, TIM5, TIM6, TIM7: clock source is SDM32kHz
- TIM10, TIM11, TIM12, TIM13, TIM14: clock source is XTAL1M

The basic timers also can be used as generic timers for time-based generation.

All the basic timers support:
- Resolution: 32-bit
- Counter mode: up

- Interrupt generation
- Secure mode
- Wakeup from sleep mode

3.9.2 PWM Timer (TIM8)

The RTL8726EA has one pulse width modulation (PWM) timer (TIM8), which is a special timer to generate PWM output waveform and synchronize the multiple PWM output. Pulse lengths and waveform periods can be modulated from a few microseconds to several seconds using the timer prescaler.

The PWM timer supports:
- Channel: 8
- Clock source: XTAL40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- One pulse mode with configurable default level and trigger edge
- PWM mode with polarity selection
- Interrupt generation
- Duty cycle: 0% ~ 100%
- Phase shift
- Secure mode

3.9.3 Capture Timer (TIM9)

The RTL8726EA has one capture timer (TIM9), which can be used for a variety of purposes, including measuring the input signal pulse width or numbers of input signals.

The capture timer supports:
- Clock source: XTAL40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- Statistic pulse width
- Statistic pulse number
- Secure mode

3.9.4 Real-time Clock (RTC) Timer

The RTC timer is an independent binary coded decimal (BCD) timer/counter that counts to a maximum error of 2s per 24 hours (23.15ppm, with the error correction circuit on).

One 32-bit register contains the seconds, minutes, hours (12- or 24-hour format) expressed in BCD format. One 32-bit register contains the days expressed in binary format. One 8-bit register contains the years expressed in binary format.

When the system boots up, the clock source of RTC timer is from SDM32K.

The features of RTC are as follows:
- Time with seconds, minutes, hours (12- or 24-hour format) days and years
- Daylight saving compensation programmable by software
- One programmable alarm with interrupt function. The alarm can be triggered by any combination of the time fields.
- Maskable interrupt/event:
  - Alarm
  - Day threshold
  - Wakeup timer
- Digital calibration circuit to compensate for source clock inaccuracy
- Register write protection
- Periodic auto-wakeup

3.9.5 Debug Timer

Debug timer is a common timestamp for all debug messages originating from all on-die processors and processor execution domains (application, kernel and firmware). It also includes a lock-free increment counter. It features:

- A simple 32-bit wrap timer
- A lock-free counter

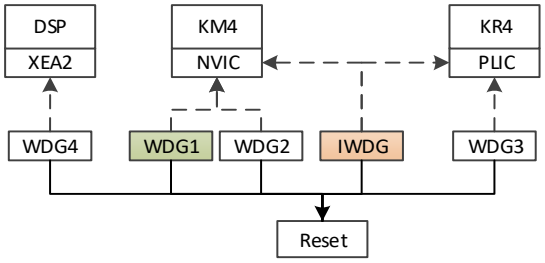
The counter is enabled by default. The counter wraps around to zero and continues to count once it reaches 32'hFFFFFFFF. A write to the timestamp will set the current value of it, however, it must continue to increment at the base of the new setting value if the writing happens when the counter is active.

The debug timer has two types of clock sources: XTAL and internal 32K. The XTAL clock may be gated in sleep mode. If user selects XTAL as the clock source in sleep mode, the debug timer will stop counting, and all the registers will be maintained. The counter will resume the increment immediately after XTAL resumes. User can select 32K as the clock source in sleep mode; however, the counter itself needs 220us to switch the clock before continuing counting. In this period, writing to this IP is not allowed. All the registers will be reset to the initial values after wakeup from deep-sleep mode.

3.9.6 Watchdog Timer

The RTL8726EA includes five watchdog timers: one independent watchdog (IWDG) and four system watchdogs (WDG).

- IWDG: dedicated for NP
- WDG1: a secure watchdog for KM4
- WDG2: a non-secure watchdog for KM4
- WDG3: watchdog for KR4
- WDG4: watchdog for HiFi 5 DSP



All the watchdogs can trigger the reset of the corresponding CPU or the whole system.

Once enabled, the watchdogs cannot be disabled.

3.9.6.1 Independent Watchdog (IWDG)

The independent watchdog (IWDG) is powered by always-on power and always-on clock source, meaning that it can stay active even when the core power or crystal fails. Also, IWDG can be configured to start by hardware at the very beginning of reset.

It features:

- Powered by always-on power and always-on clock source
- Once enabled, cannot be disabled
- Can wake up the system from sleep mode with an early interrupt
- Can reset the whole system even in sleep mode
- Optional early interrupt can be generated at a programmable time prior to watchdog timeout
- Gates automatically when the NP or AP is in debug mode
- Can be configured to run or gate in sleep mode
- A separate wake reason for each watchdog

3.9.6.2 System Watchdog (WDG1, WDG2, WDG3, WDG4)

The power and clock of system watchdog are protected by watchdog itself. Once the watchdog is enabled, the processor cannot shut off the watchdog's power and clock again.

It features:

- Optional early interrupt can be generated at a programmable time prior to watchdog timeout
- Watchdog gates automatically when the processor is in debug mode
- Gates and maintains settings in sleep mode
- Window protection function and timeout cannot be changed anymore once WDG is enabled
- Has a separate boot reason for each watchdog

3.10 Unmanned Peripheral System (UPS)

The Unmanned Peripheral System (UPS) can be regarded as a network that lets the different peripheral modules communicate directly with each other without the participation of MCU. With UPS, the participation of software can be minimized to avoid the time error caused by software operation while realizing the control of light dimming. The two sides communicating through UPS are called producer and consumer, among which the producer is the peripheral module sending out signal, and the consumer is another peripheral module that applies corresponding actions according to the received signal. It features:

- Producer and Consumer
- Configurable signal source
- Configurable input reverse
- Positive edge detection
- Various dimming signal types

3.11 General Direct Memory Access (GDMA)

The RTL8726EA has a GDMA, which allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory transactions without the participation of CPU. Each DMA stream provides unidirectional DMA transfers for a single source and destination. It features:

- Up to eight independent channels, with programmable priority
- FIFO per channel for source and destination
- Programmable flow control at block transfer level (source, destination or DMAC)
- Transaction: supports single and burst transaction mode
- DMA transfer: supports single-block and multi-block transfer
- Supports secure transfer mode

3.12 Audio

The audio module is divided into six parts: VAD, Audio ADC, DMIC interface, Audio DAC, PDM interface, and I2S. The functions and features are described below.

3.12.1 Built-in Voice Activity Detection (VAD)

The VAD is to accurately locate the beginning and end of the actual audio from the original data with noise, removing the mute and noise as interference signals from original data. It features:

- Supports MIC data from analog MIC or PDM digital MIC
- Supports single MIC human voice detection
- Supports Multi-MIC array data store before/after voice detection event
- Works in 16kHz

3.12.2 Audio Analog-to-Digital Converter (ADC)

- Built-in three channels audio ADC
- Supports programmable sampling rate from 8kHz to 96kHz
- SNR > 98dB A-weighted and THD+N < -80dB
- Supports differential microphone input and can also be configured as single-ended
- Supports programmable input analog gains
- Supports one microphone bias. The max. programmable voltage can reach 1.8V.
- Supports zero-crossing detection
- Digital volume control
- DC remove function

3.12.3 Digital Microphones (DMIC) Interface

- Up to 4 channels digital microphones
- DC remove function
- DMIC clock: 312.5kHz, 625kHz, 1.25MHz, 2.5MHz, 5MHz

3.12.4 Audio Digital-to-Analog Converter (DAC)

- Built-in mono audio DAC with line-out
- Supports programmable sampling rate from 8kHz to 192kHz
- SNR >= 98dB A-weighted, THD+N <= -85dB (AVDD=1.8V, load=10kΩ, differential output)
- Differential output or single-ended output
- Digital volume control, zero-crossing detection
- DC remove function

3.12.5 Pulse Density Modulation (PDM) Interface

- Supports 1 channel PDM output for external speaker amplifier
- PDM clock: 2.5MHz, 5MHz, 6.67MHz

3.12.6 Inter-IC Sound (I2S) Interface

The audio module integrates two I2S interfaces.

- Support I2S normal, left-justified mode, etc.
- Supports up to 8-channel I2S transmitter by TDM or PCM mode
- Audio data word length: 16/20/24/32 bits
- Channel length: 16/20/24/32 bits
- Works in master and slave mode
- In 2 channels mode, fs supports up to 384kHz.

3.13 Inter-Processor Communication (IPC)

The inter-processor communication (IPC) hardware is designed to make any two CPUs communicate with each other. The IPC provides a set of registers for each processor that facilitates inter-processor communication via interrupts. Interrupts may be independently masked by each processor to allow polled-mode operation.

The IPC communication data must be located in a common memory. It features:

- Status signaling for the 32 channels (16 channels for Tx and 16 channels for Rx)
  - Channel empty/full flag, also used as a lock
- Four sets interrupt lines per processor
  - Two sets for Rx channel full (communication data posted by sending processors)
  - Two sets for Tx channel empty (communication data retrieved by receiving processors)
- Interrupt masking per channel
  - Channel Tx empty mask
  - Channel Rx full mask
- Four hardware semaphores for atomic operation of shared resources

3.14 General-Purpose Input/Output (GPIO)

The GPIO supports the following features:

- Clock source:
  - 10MHz
  - SDM32kHz
- Separate data register and data direction register for each signal
- Read back the data on external pads using memory-mapped registers.
- Independently controllable signal by bits
- Interrupt mode for each pin

  - Level sensitive: active-high level or active-low level interrupt
  - Edge trigger: rising edge, falling edge or both edges
- Option to generate single or multiple interrupts
- Configurable de-bounce time up to 8ms to de-bounce interrupts
- Level interrupt synchronization

Each of the GPIO pins can be dynamically configured by software as output or input. GPIO pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Most of the GPIO pins are shared with digital or analog alternate functions.

3.15 Inter-integrated Circuit Interface (I2C0, I2C1)

The RTL8726EA embeds two I2C interfaces (I2C0, I2C1), which handle communications between the RTL8726EA and the serial I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing. The design of RTL8726EA I2C aims at sensor-hub application in low-power or battery-powered productions. Essential features of I2C bus protocol should be provided for acquiring or controlling external sensor data.

The I2C interface supports:
- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three speed modes
  - Standard Speed, up to 100Kbps
  - Fast Speed, up to 400Kbps
  - High Speed, up to 3.4Mbps
- Master or Slave I2C operation
- Transmitter or Receiver
- Transmit and receive FIFOs with depth of 16 and width of 12-bit
- Multi-master ability including bus arbitration scheme
- Clock stretch in master/slave mode
- 7-bit or 10-bit addressing mode, 7-bit or 10-bit combined format transfer
- Manual START/RESTART/STOP bit control
- Supports General Call, NULL DATA, START BYTE transfer protocol
- Component parameters for configurable software driver support (programmable SDA hold time, slave address, SCL duty cycle, etc.)
- Filter to eliminate the glitches on signals of SDA and SCL, programmable digital noise filter
- Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)
- Slave Mode Dual Own Address
  - Slave 1 supports 7-bit or 10-bit address mode
  - Slave 2 only supports 7-bit address mode
- Operation mode
  - Polling mode
  - Interrupt mode

3.16 Universal Asynchronous Receiver/Transmitter (UART0, UART1, UART2, UART3, LOGUART)

The UART offers a flexible means of full-duplex data exchange with external equipment, requiring an industry-standard NRZ asynchronous serial data format. It provides a very wide range of baud rates using a fractional baud rate generator. Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

3.16.1 UART0 ~ UART3

Except the LOGUART, the RTL8726EA has embedded four general UART interfaces:
- UART0: 4-wire
- UART1: 2-wire
- UART2: 2-wire
- UART3: 4-wire, reserved to control BT HCI UART. If BT function is not used, UART3 can be used for other purposes.

These UARTs have the following features:
- Clock source: XTAL or OSC2M
- Various UART formats: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Fractional baud rate

  - Up to 8Mbps within high-speed mode (40MHz)
  - 115.2Kbps within low-power mode (2MHz)
- Separated clocks for Tx path and Rx path
  - Tx path: XTAL 40MHz
  - Rx path: XTAL 40MHz, XTAL 2MHz, OSC 2MHz
- 11 bits * 16 asynchronous Transmit/Receive FIFO
- Hardware Interface auto-flow control
- Interrupt control and error detection
- IrDA (SIR mode) encoder and decoder module
- Loop-back mode for self-test
- Low power mode for Rx path
- Monitor and elimination of Rx baud rate error and own frequency drift automatically for Rx path
- UART Rx timeout mechanism
- DMA interface for DMA transfer
  - DMA as DMA TRx flow controller
  - UART as DMA Rx flow controller
- Operation mode
  - Polling mode
  - Interrupt mode

3.16.2 LOGUART

The RTL8726EA has one LOGUART. LOGUART is responsible for printing logs. It can print logs from five sources at the same time without disordered logs, also it can receive commands for CPU to process.

The LOGUART features:
- Clock source: XTAL40M, XTAL20M and OSC2M
- Follows UART protocol
- Various UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Up to 3Mbps baud rate for fast log printing
- Fractional baud rate
- Monitor function to eliminate Rx baud rate error and own frequency drift automatically for Rx path
- Five Tx ports for multi-core or multi-function to print log, which are KR4 CPU, KM4 CPU, HiFi 5 DSP, Bluetooth and Bluetooth firmware
- Supports UART relay function, Bluetooth firmware log of UART protocol from other SoC can be relayed by this IP to print out through one Tx port
- Hardware arbitration for Tx ports so that all Tx ports can print log concurrently without disordered log
- Independent open and close for five Tx ports
- Tx AGG supported, hardware adds AGG header automatically so that console can separate logs from different Tx ports
- Wakes up the system when clock source is open during sleep mode.

3.17 Serial Peripheral Interface (SPI0, SPI1)

The RTL8726EA features up to two SPIs (SPI0, SPI1) that allow communication at up to 50Mbps in master and slave modes, in half-duplex, full-duplex and simplex modes. All SPI interfaces support hardware CRC calculation and 64x16-bit embedded Rx and Tx FIFOs with DMA capability.

The SPI has the following features:
- Supports Motorola SPI Serial interface operation
- Master and slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps
- DMA interface for DMA transfer
- Independent masking of interrupts
- The Transmit and Receive FIFO buffers are 64 words in depth. The FIFO width is fixed at 16 bits.
- Hardware/Software slave-select
  - Dedicated hardware slave-select lines
  - Software control to select target serial-slave device
- Programmable features
  - Clock bit-rate – Dynamic control of the serial bit rate of the data transfer, only when configured in Master Mode.
  - Data frame size (4 to 16 bits) – Frame size of each data transfer under the control of the programmer.
  - Configurable clock polarity and phase
  - Programmable delay sample time of the received serial data bit (rxd), when configured in Master Mode

- Transfer mode
  - Transmit and receive
  - Transmit only
  - Receive only
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

3.18 Light Emitting Diode Controller (LEDC)

The RTL8726EA embeds a LEDC. LEDC is used to control external LED lamps, a common light-emitting device. It can efficiently convert electrical energy into light energy, which has a wide range of applications in modern society.

The LEDC supports the following features:
- Clock: XTAL 40MHz
- Configurable LED output high/low level time from 0 to 6.4us
- Configurable LED refresh time period up to 400us
- DMA interface with LEDC as DMA flow controller
- Configurable RGB888 display mode
- Maximum 1024 LED serial connection
- Transmit FIFO is 32*24bits
- Configurable IDLE state output level
- Operation mode
  - DMA mode
  - Interrupt mode

3.19 General Analog-to-Digital Converter (ADC)

The RTL8726EA integrates a 12-bit successive-approximation register (SAR) ADC, which provides a solution for collecting analog sensor and system power-consumption data with a low-power requirement in itself. Various operation modes, for instance, auto mode, timer-trigger mode, comparator-assist mode, and software-trigger mode, are adopted according to different using strategies.

It has the following features:
- Resolution: 12-bit SAR
- ENOB: 10-bit
- Available channel number:
  - 6 external channels
  - 1 internal channel
- Configurable input:
  - Single-ended
  - Differential with predefined channel pair
- Input voltage range:
  - Single-ended external channels:
    - Divided mode: 0 ~ 3.3V
  - Differential channels (P-N):
    - Divided mode: 0 ~ 1.65V
- Configurable ADC clock
  - Prescaler with oscillator 2MHz clock input
  - Prescaler with XTAL 40MHz clock input
- Configurable channel switch order and channel number
- Contain 64 FIFO entry which is 16-bit width
- Individual channel compare mode
- Individual channel register
- Multi-sampling trigger sources
  - Software
  - Timer
- Manual and auto mode conversion
  - Manual mode for software-controllable conversion
  - Auto mode for hardware continuous conversion

3.20 Thermal Sensor

The RTL8726EA has integrated a thermal sensor, which can be used to detect and monitor the real-time temperature inside the chip. It has the following features:

- Measurement range: –40°C ~ 125°C
- Variation: ±1°C (typical), ±3°C (worst)
- Provides low- temperature warning, high-temperature warning and over-temperature protection
- Provides thermal enable and over-temperature protection enable write access control

The temperature protection mechanism is an important feature provided by the thermal sensor, and is implemented as follows:

- When the temperature exceeds the limit high-temperature threshold, an interrupt is sent to the CPU, and the CPU will reduce the frequency and speed.
- When the temperature exceeds the limit low-temperature threshold, an interrupt is sent to the CPU, and the CPU will increase the frequency and speed.
- When the temperature exceeds the limit over-temperature protection threshold, the hardware will be powered down automatically for over-temperature protection.

By default, Realtek's SDK does not automatically adjust the CPU frequency and speed based on the temperature detected by thermal meter. If users need to use this function, please call the thermal related APIs to configure the temperature threshold according to the actual application and heat dissipation conditions.

3.21 Cap-Touch Controller (CTC)

Self-capacitance touch controller measures the capacitance between the capacitive sensor pin and ground. The capacitive touch controller detects the presence of a finger on or near a touch surface through capacitance changes.

The CTC of RTL8726EA provides up to 9 channels for capacitive sensing, which offers a wide range of capacitance detection. It can adjust the sensitivity and threshold of each channel according to different noise environment. It also can calibrate the baseline and absolute finger touch threshold automatically when environment changes. At the same time, the CTC offers an adjustable scan period to achieve lower power consumption.

The CTC has the following features:

- 9 capacitive sensor channels:
  - A wide range of parasitic capacitance for each channel: 5 ~ 45pF (@5uA sensitivity @OSC131kHz)
  - Detection of both finger touch and proximity touch
  - Programmable enable/disable for each channel
  - Adjustable sensitivity for each channel: 0.25uA ~ 15.75uA
- Adjustable baseline and touch threshold (both difference and absolute value) for each channel
- Automatic channel scan: hardware scans each enabled channel automatically in sequence
- Programmable scan period: sample number and scan interval
  - Configurable sample clock:
    - OSC131kHz
    - XTAL 2M divider: max. sample clock = 1MHz
- Two touch judgment modes:
  - Difference threshold judgment mode (with ETC function enabled)
  - Absolute threshold judgment mode (with ETC function disabled)
- Debug mode: only scan channel specified, hardware bypass ADC raw code to software
- Active noise immunity:
  - Supports SNR information monitor
  - Adjustable environmental noise threshold for each channel
- Automatic environment tracking and calibration (ETC)
  - Automatic hardware baseline initialization
  - Automatic baseline and threshold update for different noise environments
  - Programmable ETC update step and factor
- Programmable button debounce function
- Interrupt control:
  - Programmable interrupt enabled for each interrupt source
  - Software readable interrupt status and raw status register
- 64*16 bit FIFO: for ADC sample data
- Low power consumption

4 Electrical Characteristics

4.1 Parameters Definitions

4.1.1 Maximum and Minimum Values

Unless otherwise specified, all data are guaranteed by design, simulation and samples test to be applicable to all declared temperature, voltage ranges and processes, and are not tested in production.

4.1.2 Typical Values

Unless otherwise specified, the typical values are reference results when the IC is at an ambient temperature of 25°C and an operating voltage of 3.3V. This value is for reference design only and not actually tested.

4.1.3 Pin Status

4.1.3.1 Loading Capacitor

Unless otherwise specified, the load refers to the equivalent capacitance mounted on the chip pin. Schematic diagrams used for loading capacitor measurements is illustrated in *Figure 4-1*.

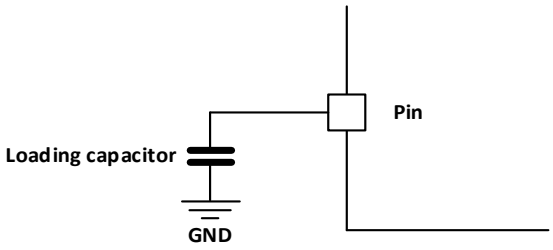


Figure 4-1 Loading capacitor diagram of pin

4.1.3.2 Input Voltage

Unless otherwise specified, the input voltage of the chip pin refers to the voltage difference between the pin and ground. The schematic diagram is illustrated in *Figure 4-2*.

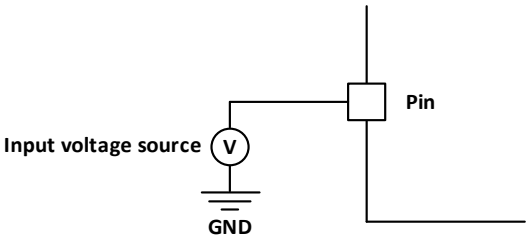


Figure 4-2 Input voltage diagram of pin

4.2 Absolute Maximum Ratings

Stresses beyond absolute maximum ratings may cause permanent damage to the device. These are emphasized ratings only and do not imply functional operation of the device.

Table 4-1 Absolute maximum ratings

Symbol	Parameter	Condition	Min.	Max.	Unit
VAH_LDOM, VDH_IO1, VDH_IO2, VRH_PA, VRH_RF, VAH_XTAL, VAH_AUX, VAH_DCDC	External main supply voltage	Input DC voltage at power pin	-0.3	3.63	V
VIN	Input voltage on PA*x* & PB*x* pins	Input DC voltage at digital I/O pin, VDH_IO*x*≤3.63V	-0.3	VDH_IO*x*+0.3	V
	Input voltage on MIC*x* pins	Input DC voltage at analog pin, VAM_AUD≤1.95V		VAM_AUD+0.3	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		0	dBm
T_{STORE}	Storage temperature range		-65	+150	°C
MSL	Moisture Sensitivity Level			MSL3	
HBM	ESD Human Body Model	T_A=25°C, conforming to JESD22-A114F		Class 2	
CDM	ESD Charged Device Model	T_A=25°C, conforming to JESD22-C101F		Class C2	

4.3 Operation Conditions

Table 4-2 Recommended operation conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
VAH_LDOM, VDH_IO2, VRH_PA, VRH_RF, VAH_XTAL, VAH_AUX, VAH_DCDC[1]	Power pin voltage		2.97	3.3	3.63	V
VDH_IO1	Power supply pin for I/O pins		1.7	3.3/1.8	3.63	V
VAM_AUD, LDOM_OUT, VDM_PSRAM	Power pin voltage		1.7	1.8	1.95	V
VDL_CORE, LDOC_OUT	Power pin voltage		0.81	0.9/1.0	1.05	V
VRM_RF, VRM_SYN, VAM_AFE	Power pin voltage		1.2	1.25/1.8	1.95	V
VAM_LDOC	Power pin voltage		1.2	1.25/1.35	1.45	V
I_{VDD}	Capability of external power supply[2]		0.8	-	-	A
T_A	Ambient operating temperature	Standard temperature IC	-20		+85	°C
		Wide-range temperature IC	-40		+105	°C
T_J max.	Maximum junction temperature[3][4]		-	-	+125	°C

CAUTION

[1] All these power pins must be powered by the same voltage. For IC's stable performance, the voltage ripple on these pins is suggested to be under +/-100mV.

[2] When using an external single power supply, the output current needs to reach more than 0.8A, which does not include the power consumption on peripherals and GPIOs.

[3] The junction temperature must not exceed T_J max. in all T_A ranges. When T_A is high and the power consumption of device is also high, a well-designed thermal management should be implemented to the board system to guarantee proper T_J. Refer to Section Thermal Characteristics to estimate T_J.

[4] The IC must not operate at junction temperature of 125°C for extended periods of time.

4.4 Power Sequence

The recommended power-on and power-off sequences are depicted in the following sections. The VDH_*x*/VAH_*x*/VRH_*x* and CHIP_EN are powered and controlled by external power sources. Other used voltages are recommended to be powered by the embedded regulator or LDO.

NOTE

The VDH_x/VAH_x/VRH_x refers to typical 3.3V power supply including VAH_LDOM, VDH_IO2, VRH_PA, VRH_RF, VAH_XTAL, VAH_AUX and VAH_DCDC. The VDH_IO1 can be powered by typical 3.3V or 1.8V, and should be stable before the corresponding GPIOs normal operation.

The parameter specification of power sequence is listed in *Table 4-3*.

Table 4-3 Power sequence specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{NORMAL}	VDH_*x*/VAH_*x*/VRH_*x* normal operation voltage	2.97	3.3	3.63	V
V_{POR_H}	Power on reset high level	1.9	2.1	2.7	V
V_{POR_L}	Power on reset low level	0.5			V
V_{IL}	CHIP_EN input low voltage	0	0	0.8	V
V_{IH}	CHIP_EN input high voltage	2.0	3.3	3.63	V
T_0	VDH_*x*/VAH_*x*/VRH_*x* rising time	0.1			ms
T_1	VDH_*x*/VAH_*x*/VRH_*x* ready time			3.2	ms
T_{CORE}	Core power on time		4.5/6[1]		ms
T_{TM}	Test mode trap time	0		4	ms
T_{PSO}	Power supply option trap time	0		4	ms
T_{UD}	UART download mode trap time	0		5	ms
T_2	VDH_*x*/VAH_*x*/VRH_*x* falling time	0.1	100		ms
T_3	VDH_*x*/VAH_*x*/VRH_*x* low voltage last time	0.3			ms
Debounce time	CHIP_EN debounce time, set by registers				
T_4	CHIP_EN low voltage last time	0.1			ms

NOTE

[1] T_{CORE} is characterized under 3.3V power supply and 25°C. 4.5ms is characterized under power supply option 1, and 6ms is characterized under power supply option 2

4.4.1 Power-on Sequence

During power on, the VDH_*x*/VAH_*x*/VRH_*x* needs to rise monotonously. When the VDH_*x*/VAH_*x*/VRH_*x* is over V_{POR_H} and the CHIP_EN is high, the chip releases internal reset, and the VDH_*x*/VAH_*x*/VRH_*x* needs to rise up to V_{NORMAL} within T_1. There is no restriction that CHIP_EN is pulled up earlier or later than VDH_*x*/VAH_*x*/VRH_*x* or at the same time with VDH_*x*/VAH_*x*/VRH_*x*.

- T_{TM} after IC release internal reset, the IC will get PA1/TM_DIS state. When PA1/TM_DIS is high, the IC will enter normal mode. When PA1/TM_DIS is low, the IC will enter test mode.
- T_{PSO} after IC release internal reset, the IC will get PA22/PSO_SEL state. When PA22/PSO_SEL is high, the IC is supposed to be powered by power supply option2. When PA22/PSO_SEL is low, the IC is supposed to be powered by power supply option1. Refer to Section *3.1.1* for more details.
- T_{CORE} after IC release internal reset, embedded SWR and LDO will start to output core power for VDL_CORE. In the following TUD, the IC will get PA20/UD_DIS state. When PA20/UD_DIS is high, the IC will enter normal boot mode. When PA20/UD_DIS is low, the IC will enter UART download mode.

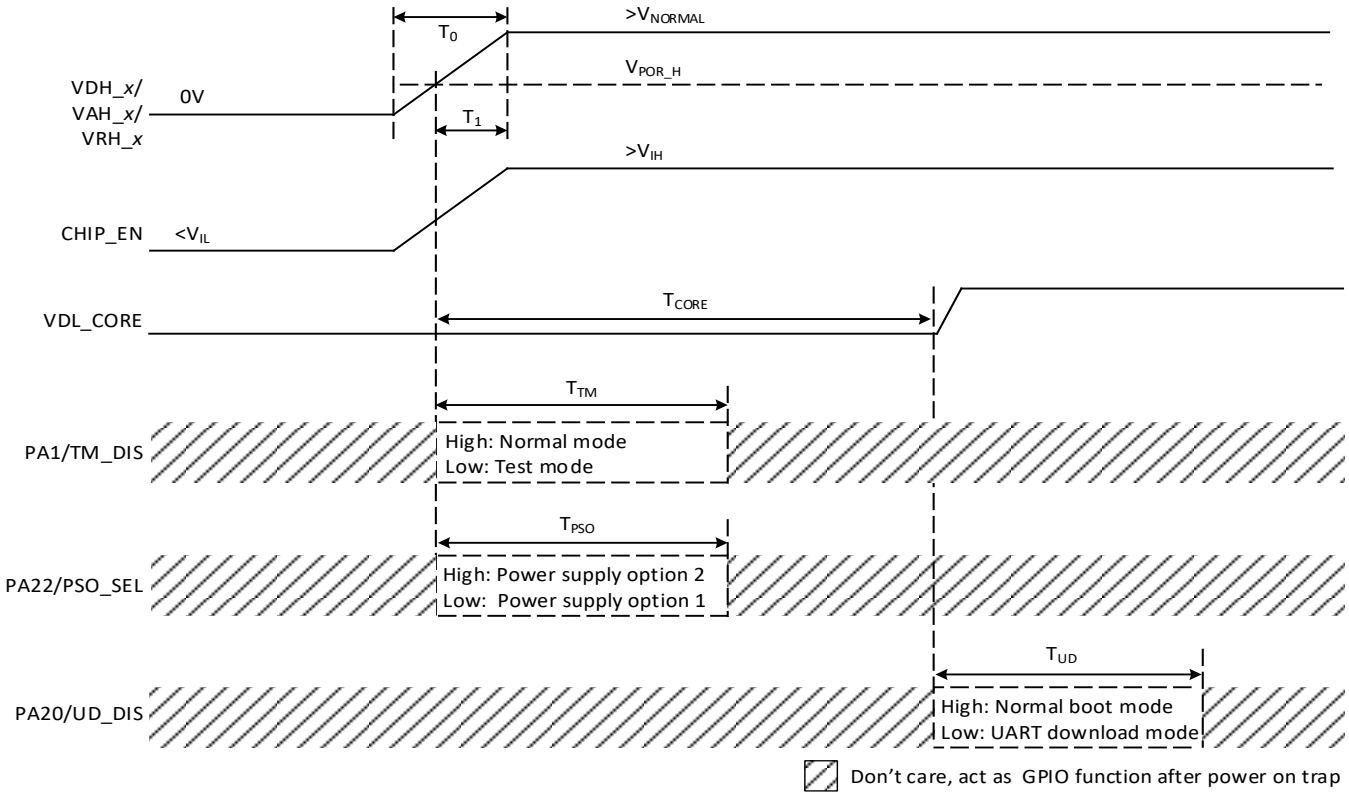


Figure 4-3 Power-on sequence

4.4.2 Power-off Sequence

In the process of power-off, the VDH_*x*/VAH_*x*/VRH_*x* needs to drop down below V_{POR_L} and lasts for at least T_3 before it can be boosted and the IC can be powered on again. Any voltage between V_{NORMAL} and V_{POR_L} may not trigger a reset, and it may cause the chip to work abnormally.

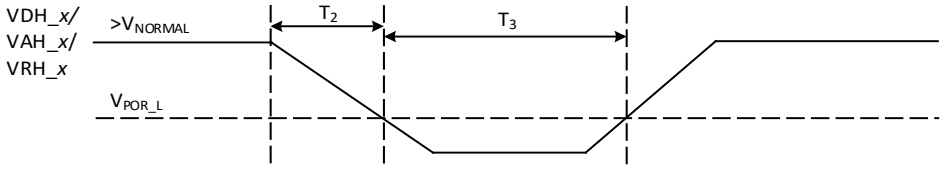


Figure 4-4 Power-off sequence

4.4.3 CHIP_EN Reset Sequence

When using the CHIP_EN as normal reset function, users can set the expected debounce time, ranging from 0us to 16ms. This time may have max. ±50% variation under different conditions, such as different voltage, temperature, etc. When reset, the pull down time must be T_4 more than debounce time, and the variation of debounce time needs to be taken into consideration.

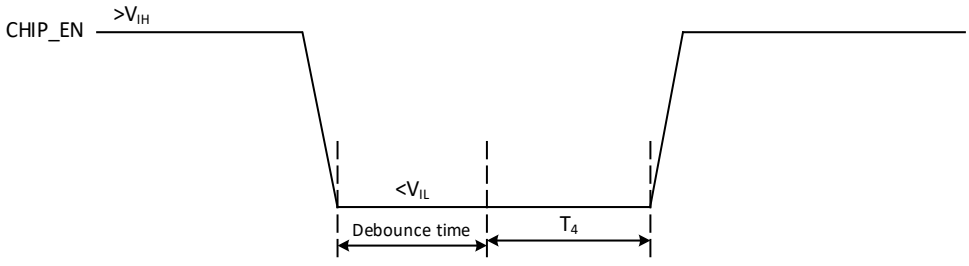


Figure 4-5 CHIP_EN reset sequence

4.5 Reset Detection

The parameters given in *Table 4-4* are derived from test under ambient operating temperature.

Table 4-4 Embedded power supply supervisor characteristics

Symbol	Parameter	Configuration	Min.	Typ.	Max.	Unit
V_{BOD_L}	Brownout detect falling threshold	BOD_THRESHOLD9	-5%	2.82	+5%	V
		BOD_THRESHOLD10		2.77		V
		BOD_THRESHOLD11		2.73		V
		BOD_THRESHOLD12		2.69		V
		BOD_THRESHOLD13		2.64		V
		BOD_THRESHOLD14		2.58		V
		BOD_THRESHOLD15		2.54		V
V_{BOD_H}	Brownout detect rising threshold	BOD_THRESHOLD7	-5%	2.97	+5%	V
		BOD_THRESHOLD8		2.92		V
		BOD_THRESHOLD9		2.87		V
		BOD_THRESHOLD10		2.83		V
		BOD_THRESHOLD11		2.78		V
		BOD_THRESHOLD12		2.74		V
		BOD_THRESHOLD13		2.68		V

NOTE

The V_{BOD_L} and V_{BOD_H} can be set independently. V_{BOD_H} needs to be set higher than V_{BOD_L}. It is recommended to reserve about 200mV or higher hysteresis window between V_{BOD_H} and V_{BOD_L}.

4.6 Embedded Regulators Characteristics

The characteristics of embedded regulators including LDOC, DCDC, and LDOM are guaranteed by design.

Table 4-5 Embedded regulators characteristics

Regulators	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
LDOC	V_{IN}	Input voltage range		1.2	1.25/1.35	1.45	V
	V_{OUT}	Output voltage range		0.81	0.9/1.0	1.05	V
	I_{LOAD}	Load current[1]				410	mA
DCDC	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range	Power supply option 1[2]	0.81	0.9/1.0	1.05	V
			Power supply option 2[2]	1.2	1.25/1.35	1.45	V
	I_{LOAD}	Load current[1]	PWM mode			480	mA
			PFM mode			50	mA
	F	Switching frequency	PWM mode		2		MHz
LDOM	V_{IN}	Input voltage range		2.97	3.3	3.63	V
	V_{OUT}	Output voltage range		1.7	1.8	1.95	V
	I_{LOAD}	Load current[1]				160	mA

NOTE

[1] No additional external load is accepted unless mentioned.

[2] Refer to Section Power Structure for details of power supply options.

4.7 Crystal Characteristics

The RTL8726EA has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned. The characteristic requirements of external crystal are listed in *Table 4-6*.

Table 4-6 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm

Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

4.8 I/O Pin Characteristics

This section applies when GPIO is used as a digital function, but not when it is used as an analog function.

Table 4-7 Digital I/O pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	V_{IO}[1]=1.8V±10%	-0.3	-	0.35 * V_{IO}	V
		V_{IO}[1]=3.3V±10%	-0.3	-	0.8	
V_{IH}	I/O input high level voltage	V_{IO}[1]=1.8V±10%	0.65 * V_{IO}	-	-	
		V_{IO}[1]=3.3V±10%	2	-	-	
V_{OL}[2]	I/O output low level voltage	V_{IO}[1]=1.8V±10%, I_{OL} Max.[2]	-	-	0.15 * V_{IO}	
		V_{IO}[1]=3.3V±10%, I_{OL} Max.[2]	-	-	0.15 * V_{IO}	
V_{OH}[2]	I/O output high level voltage	V_{IO}[1]=1.8V±10%, I_{OH} Max.[2]	0.85 * V_{IO}	-	-	
		V_{IO}[1]=3.3V±10%, I_{OH} Max.[2]	0.85 * V_{IO}	-	-	

NOTE

[1] V_{IO} is the power supply for I/O pin.
[2] Refer to Table 4-8 for driving strength.

All I/O types are listed in *Table 4-8*.

Table 4-8 I/O types

Pin name	I/O power pin	Driving (mA)[1]		Internal pull resistor (kΩ)[2]			Resistor available in deep-sleep mode[3]?
		1.8V (±10%)	3.3V (±10%)	Min.	Typ.	Max.	
PA0~PA13[4]	VAH_LDOM	-	8/16	40	80	120	Y
PA14~PA18[4]	VDH_IO2	-	8/16	2.3/5	4.7/10	7.1/15	Y
PA19~PA22[4]	VDH_IO2	-	4/8	40	80	120	Y
PA28~PA31/PB0~PB5[5]	VDH_IO1	1/2	4/8	40	80	120	Y
PA23~PA27/PB6~PB10[5]	VDH_IO1	2/4	8/16	2.3/5	4.7/10	7.1/15	Y
PB11~PB19[6]	VAM_AUD	1/3	-	PU:185 PD:52	PU:300 PD:100	PU: 431 PD:165	N

NOTE

[1] The I/O powers supported by different I/Os are different, and the driving capability is related to the I/O powers. Refer to Table 4-7 for V_{OH} and V_{OL}. Different drive capabilities can be controlled by registers. For example, 4/8 refers to the driving capability of 4mA or 8mA, which can be adjusted through registers.
[2] Except for PB11~PB19, the pull-up and pull-down values of other I/Os are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The range is ±50%. Different resistor can be controlled by registers. For example, 4.7/10 refers to the internal pull resistor of 4.7kΩ or 10kΩ, which can be adjusted through registers.
[3] In deep-sleep mode, PB11~PB19 are in floating state, and the internal resistors of these pins are not available. If circuit connected with these GPIOs needs to be pulled high or low state, external resistors on PCB are needed. In other mode except deep-sleep, internal resistors of all GPIOs are available.
[4] The pins of this group only support 3.3V I/O power.
[5] The pins of this group support 1.8V/3.3V I/O power.
[6] The pins of this group only support 1.8V I/O power.

4.9 Power Consumption Characteristics

For the current data provided in the following sections, the typical current is the average current of multiple typical process chips, and the maximum current is the worst case caused by process deviations. The power consumption of chip is affected by voltage, temperature and process deviations.

The power consumption data given in the following sections is the result of the IC powered by 3.3V and different ambient temperatures.

4.9.1 Power-Saving Mode Power Consumption

The MCU is under the following working conditions:

- Except for LOGUART Tx/Rx (PA20/PA19), other I/O pins are in input mode.
- All peripherals except GPIOs are disabled.
- The thermal sensor is off.

Table 4-9 Power-saving mode

Operating mode	KM4 mode	KR4 mode	DSP mode	DCDC mode	LDOM	Wi-Fi/BT	SRAM state
Sleep Mode 1	CG[1]	CG	OFF	PFM	ON	OFF	Retention
Sleep Mode 2	PG[2]	PG	OFF	PFM	ON	OFF	Retention
Deep-sleep mode[3]	OFF	OFF	OFF	OFF	OFF	OFF	Shut down

NOTE

[1] CG: Clock Gating
[2] PG: Power Gating
[3] Only some circuits in the AON area are still working.

4.9.1.1 RTL8726EAM

Operating voltage	Symbol	Operating mode	Typ.		Unit
			25°C	85°C	
3.3V	I_{VDD} (LP1)	Sleep mode 1	2.53	16.3	mA
	I_{VDD} (LP2)	Sleep mode 2	0.70	4.73	mA
	I_{VDD} (LP3)	Deep sleep mode	57.4	362	µA

4.9.2 MCU Operating Mode Power Consumption

The MCU is under the following working conditions:

- Except for LOGUART Tx/Rx (PA20/PA19), other I/O pins are in input mode.
- All peripherals except GPIOs are disabled.
- The thermal sensor is off.
- KM4 is set as the application processor and KR4 is set as the network processor.

For different application scenarios, the required CPU operating frequency is different, and the corresponding power consumption will also be different.

Table 4-10 MCU operating mode

MCU operating mode	KM4	KR4	DSP	VDL_CORE voltage
MCU operating mode 1	40MHz	40MHz	40MHz	0.9V
MCU operating mode 2	300MHz	300MHz	400MHz	0.9V
MCU operating mode 3	400MHz	400MHz	500MHz	1.0V

In the case of the same MCU operating mode, the CPU will be in different modes at different times.

Table 4-11 IC status in operating mode

Active mode	KM4 mode	KR4 mode	DSP mode	Wi-Fi/BT	SRAM state
Active mode 1	WFI[1]	WFI	WFI	OFF	Standby
Active mode 2	WFI	WFI	CG[3]	OFF	Standby
Active mode 3	NOP[2]	WFI	CG	OFF	Standby
Active mode 4	NOP	NOP	CG	OFF	Standby
Active mode 5	WFI	WFI	FC[4]	OFF	Standby
Active mode 6	NOP	NOP	FC	OFF	Standby

NOTE

[1] WFI (Wait for interrupt): Arm instruction
[2] NOP (NO Operation): Arm instruction
[3] CG: Clock Gating
[4] FC: Full Connect

4.9.2.1 MCU Operating Mode 1

4.9.2.1.1 RTL8726EAM

Operating voltage	Symbol	Active mode	Typ.		Unit
			25°C	85°C	
3.3V	I_{VDD} (Active 1)	Active mode 1	6.08	18.7	mA
	I_{VDD} (Active 2)	Active mode 2	6.01	18.7	
	I_{VDD} (Active 3)	Active mode 3	6.41	19.1	
	I_{VDD} (Active 4)	Active mode 4	6.96	19.7	
	I_{VDD} (Active 5)	Active mode 5	11.0	24.1	
	I_{VDD} (Active 6)	Active mode 6	11.8	24.9	

4.9.2.2 MCU Operating Mode 2

4.9.2.2.1 RTL8726EAM

Operating voltage	Symbol	Active mode	Typ.		Unit
			25°C	85°C	
3.3V	I_{VDD} (Active 1)	Active mode 1	12.7	25.8	mA
	I_{VDD} (Active 2)	Active mode 2	11.9	24.8	
	I_{VDD} (Active 3)	Active mode 3	14.9	28.0	
	I_{VDD} (Active 4)	Active mode 4	18.7	31.7	
	I_{VDD} (Active 5)	Active mode 5	67.2	85.4	
	I_{VDD} (Active 6)	Active mode 6	74.4	92.9	

4.9.2.3 MCU Operating Mode 3

4.9.2.3.1 RTL8726EAM

Operating voltage	Symbol	Active mode	Typ.		Unit
			25°C	85°C	
3.3V	I_{VDD} (Active 1)	Active mode 1	17.0	35.2	mA
	I_{VDD} (Active 2)	Active mode 2	15.8	33.8	
	I_{VDD} (Active 3)	Active mode 3	20.6	39.1	
	I_{VDD} (Active 4)	Active mode 4	27.3	46.0	
	I_{VDD} (Active 5)	Active mode 5	98.9	127	
	I_{VDD} (Active 6)	Active mode 6	110	140	

4.9.3 RF Power Consumption

RF power consumption refers to the static power consumption of the IC in the Tx/Rx states as well as Idle/Standby states under MP mode.

All measurements are tested under the following conditions:

- CPU work mode:
  - CPU frequency: KM4 200MHz, KR4 200MHz, DSP off
  - Both KM4 and KR4 are in WFI working state.
- RF operation mode:
  - Active (RF works)
    - Continuous Tx (Duty 100%)
    - Packet Rx
  - RF Idle: RF enters Rx mode but doesn't receive any signal.
  - RF Standby: RF bias circuits and synthesizer on.
  - Channel: CH7 @2.4G BW20M

4.9.3.1 RTL8726EAM

Operating voltage	Power supply option	Conditions	Typ.	Unit
3.3V	Power supply option 1[1]	1T-HE MCS9/BW20M (16dBm@2.4G)	286	mA
		1T-HE MCS0/BW20M (20dBm@2.4G)	354	
		1T-HT MCS7/BW20M (18dBm@2.4G)	314	
		1T-HT MCS0/BW20M (20dBm@2.4G)	358	
		1T-OFDM54M (19dBm@2.4G)	332	
		1T-OFDM6M (20dBm@2.4G)	356	
		1T-CCK11M (20dBm@2.4G)	358	
		1T-CCK1M (20dBm@2.4G)	357	
		1R-HE MCS9/BW20M (Pin= -60dBm)	85	
		1R-HT MCS7/BW20M (Pin= -60dBm)	85	
		1R-OFDM54M (Pin= -60dBm)	85	
		1R-CCK11M (Pin= -60dBm)	72	
		RF Idle	70	
		RF Standby	74	
	Power supply option 2[2]	1T-HE MCS9/BW20M (16dBm@2.4G)	275	mA
		1T-HE MCS0/BW20M (20dBm@2.4G)	347	
		1T-HT MCS7/BW20M (18dBm@2.4G)	310	
		1T-HT MCS0/BW20M (20dBm@2.4G)	353	
		1T-OFDM54M (19dBm@2.4G)	328	
		1T-OFDM6M(20dBm@2.4G)	350	
		1T-CCK11M (20dBm@2.4G)	356	
		1T-CCK1M (20dBm@2.4G)	354	
		1R-HE MCS9/BW20M (Pin= -60dBm)	75	
		1R-HT MCS7/BW20M (Pin= -60dBm)	75	
		1R-OFDM54M (Pin= -60dBm)	75	
		1R-CCK11M (Pin= -60dBm)	59	
		RF Idle	57	
		RF Standby	46	

NOTE

[1] Power supply option 1: VDL_CORE is 1.0V from DCDC and VRM_RF is 1.8V from LDOM_OUT, refer to Section 3.1.1 for more details.

[2] Power supply option 2: VDL_CORE is 1.0V and VRM_RF is 1.35V, refer to Section 3.1.1 for more details.

4.9.4 WoWLAN Power Consumption

This section provides power consumption data in Wake on Wireless Lan (WoWLAN) state. The power consumption data in the following sections are the results of the IC operating at 25°C and 3.3V.

All measurements are tested under the following conditions:

- MCU working conditions:
  - Except for UART_LOG TXD/RXD (PA20/PA19), other I/O pins are in input mode.
  - All peripherals except GPIOs are disabled.
  - The CPU is in PG mode outside the wake-up state.
  - The thermal sensor is on.
- WoWLAN power consumption test conditions:
  - Test environment: shielded room
  - Ambient temperature: 25°C
  - AP: Tenda AX3000
  - Wi-Fi works in 2.4G frequency band.
  - The power consumption when Delivery Traffic Indication Message (DTIM) is 1/3/10 is measured separately.
  - Take the average current value within 20 minutes as the test value.

4.9.4.1 RTL8726EAM

Operating voltage	DTIM	Wi-Fi frequency	Typ.	Unit
3.3V	DTIM=1	2.4G	1.77	mA

	DTIM=3	2.4G	1.48	
	DTIM=10	2.4G	1.36	

4.9.5 Bluetooth Power Consumption (TBD)

4.9.6 Maximum Power Consumption

The maximum power consumption scenario will cause the IC temperature to rise significantly, so the heat dissipation of the circuit board will have a great impact on the temperature rise and current data.

This section provides current data in the maximum power consumption scenario, which is measured on Realtek's EVB.

The maximum power consumption scenario is as follows:

- KM4: 400MHz, in drystone state
- KR4: 400MHz, in drystone state
- DSP: 500MHz, runs IIR algorithm (Biquad Real IIR DF1 implementation for stereo channels)
- Wi-Fi: uses 20dBm power to continuously Tx in 2.4G frequency band

4.9.6.1 RTL8726EAM

Symbol	Parameter	Condition	Maximum power consumption (mA)
I_{VDD33}	Absolute maximum power consumption at 3.3V DC power supply	Ambient temperature = 25°C	470
		Junction temperature = 125°C	764

4.10 RF Characteristics

4.10.1 WLAN Radio Specifications

This section describes the RF characteristics of WLAN 2.4GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

4.10.1.1 WLAN 2.4GHz Band Receiver Performance

Table 4-12 WLAN 2.4GHz band receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Rx Sensitivity 802.11b	1Mbps CCK		-100		dBm
	2Mbps CCK		-97		dBm
	5.5Mbps CCK		-94		dBm
	11Mbps CCK		-91		dBm
Rx Sensitivity 802.11g	BPSK rate 1/2, 6Mbps OFDM		-95		dBm
	BPSK rate 3/4, 9Mbps OFDM		-94		dBm
	QPSK rate 1/2, 12Mbps OFDM		-92.5		dBm
	QPSK rate 3/4, 18Mbps OFDM		-90		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-87		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-83.5		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-79.5		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-78		dBm
Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-95		dBm
	MCS 1, QPSK rate 1/2		-92.5		dBm
	MCS 2, QPSK rate 3/4		-90		dBm
	MCS 3, 16-QAM rate 1/2		-86.5		dBm
	MCS 4, 16-QAM rate 3/4		-83.5		dBm
	MCS 5, 64-QAM rate 2/3		-79.5		dBm

	MCS 6, 64-QAM rate 3/4		-78		dBm
	MCS 7, 64-QAM rate 5/6		-76.5		dBm
Rx Sensitivity 802.11ax BW = 20MHz	MCS 0, BPSK rate 1/2		-95		dBm
	MCS 1, QPSK rate 1/2		-92		dBm
	MCS 2, QPSK rate 3/4		-89.5		dBm
	MCS 3, 16-QAM rate 1/2		-86.5		dBm
	MCS 4, 16-QAM rate 3/4		-83		dBm
	MCS 5, 64-QAM rate 2/3		-79		dBm
	MCS 6, 64-QAM rate 3/4		-78		dBm
	MCS 7, 64-QAM rate 5/6		-76.5		dBm
	MCS 8, 256-QAM rate 3/4		-72.5		dBm
	MCS 9, 256-QAM rate 5/6		-70.5		dBm
Max. Receive Level	6Mbps OFDM		0		dBm
	54Mbps OFDM		0		dBm
	11n MCS 0, HT20		0		dBm
	11n MCS 7, HT20		0		dBm
	11ax MCS 0, HE20		0		dBm
	11ax MCS 9, HE20		0		dBm
Adjacent Channel Rejection	11Mbps CCK		46		dB
	BPSK rate 1/2, 6Mbps OFDM		45		dB
	64-QAM rate 3/4, 54Mbps OFDM		25		dB
	HT20, MCS 0, BPSK rate 1/2		42		dB
	HT20, MCS 7, 64-QAM rate 5/6		24		dB
	HE20, MCS 0, BPSK rate 1/2		42		dB
	HE20, MCS 8, 256-QAM rate 3/4		20		dB
	HE20, MCS 9, 256-QAM rate 5/6		17		dB

4.10.1.2 WLAN 2.4GHz Band Transmitter Performance

Table 4-13 WLAN 2.4GHz band transmitter performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK		20		dBm
	11Mbps CCK		20		dBm
	BPSK rate 1/2, 6Mbps OFDM		20		dBm
	64-QAM rate 3/4, 54Mbps OFDM		19		dBm
	HT20,MCS 0, BPSK rate 1/2		20		dBm
	HT20, MCS 7, 64-QAM rate 5/6		18		dBm
	HE20, MCS 8, 256-QAM rate 3/4		17		dBm
	HE20, MCS 9, 256-QAM rate 5/6		16		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM		-32	-5	dB
	64-QAM rate 3/4, 54Mbps OFDM		-34	-25	dB
	HT20, MCS 0, BPSK rate 1/2		-32	-5	dB
	HT20, MCS 7, 64-QAM rate 5/6		-35	-27	dB
	HE20, MCS 8, 256-QAM rate 3/4		-36	-30	dB
	HE20, MCS 9, 256-QAM rate 5/6		-36	-32	dB
Output power variation	TSSI on across operating temperature range, all channels and VSWR≤1.5:1 at RFIO port	-1.5		1.5	dB
Carrier suppression				-32	dBc
Harmonic output power[2]	2nd harmonic		-21		dBm/MHz
	3rd harmonic		-20		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable.
[2] Harmonic output power is tested at IC port.
[3] Harmonic output power is measured at RF connector with pi-shape LC low pass filter.

4.10.2 Bluetooth Radio Specifications

This section describes the RF characteristics of Bluetooth 2.4GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

4.10.2.1 Basic Rate (BR) Receiver Performance

Table 4-14 BR receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	2441	2480	MHz
Receiver Sensitivity	BER<0.1%		-94.5		dBm
Max. Usable Signal	BER<0.1%		0		dBm
C/I co-channel (BER<0.1%)	Co-channel sensitivity		9		dB
C/I 1MHz (BER<0.1%)	Adjacent channel selectivity		-17		dB
C/I 2MHz (BER<0.1%)	2nd adjacent channel selectivity		-46		dB
C/I 3MHz (BER<0.1%)	3rd adjacent channel selectivity		-53		dB
C/I Image Channel (BER<0.1%)	Image channel selectivity		-22		dB
C/I Image 1MHz (BER<0.1%)	1MHz adjacent to image channel selectivity		-31		dB
Inter-modulation			-33		dBm
Out-of-band blocking	30MHz to 2000MHz	-10			dBm
	2000MHz to 2400MHz	-27			dBm
	2500MHz to 3000MHz	-27			dBm
	3000MHz to 12.75GHz	-10			dBm

4.10.2.2 Basic Rate (BR) Transmitter Performance

Table 4-15 BR transmitter performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	2441	2480	MHz
Max. Transmit Power	At max. power output level		8		dBm
Gain step			4		dB
Modulation characteristics	Δf1 avg.		165		kHz
	Δf2 max. (for at least 99.9% of all Δf2 max.)	115			kHz
	Δf1 avg./Δf2 avg.		0.93		
ICFT	Initial carrier frequency tolerance		±15		kHz
Carrier Frequency Drift	One slot packet (DH1)		±10		kHz
	Two slot packet (DH3)		±10		kHz
	Five slot packet (DH5)		±10		kHz
	Max. drift rate		±10		kHz
Tx Output Spectrum	20dB bandwidth			1000	kHz
Adjacent Channel Power	±2MHz offset		-55		dBm
	±3MHz offset		-57		dBm
	>±3MHz offset		-59		dBm

4.10.2.3 Enhanced Data Rate (EDR) Receiver Performance

Table 4-16 EDR receiver performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	2441	2480	MHz
Receiver Sensitivity (BER < 0.007% after 1600000 bits/BER < 0.01% after 16000000 bits)	π/4 DQPSK		-94.4		dBm
	8PSK		-88.1		dBm
Max. Usable Signal (BER<0.1%)	π/4 DQPSK		0		dBm

	8PSK		0		dBm
C/I co-channel (BER<0.1%)	π/4 DQPSK		8		dB
	8PSK		15		dB
C/I 1MHz (BER<0.1%)	π/4 DQPSK		-15		dB
	8PSK		-8		dB
C/I 2MHz (BER<0.1%)	π/4 DQPSK		-47		dB
	8PSK		-41		dB
C/I 3MHz (BER<0.1%)	π/4 DQPSK		-54		dB
	8PSK		-48		dB
C/I Image Channel (BER<0.1%)	π/4 DQPSK		-23		dB
	8PSK		-21		dB
C/I Image 1MHz (BER<0.1%)	π/4 DQPSK		-31		dB
	8PSK		-28		dB

4.10.2.4 Enhanced Data Rate (EDR) Transmitter Performance

Table 4-17 EDR transmitter performance

Parameter	**Condition**		**Performance**			**Unit**
			Min.	Typ.	Max.	
Frequency Range	Center channel frequency		2402	2441	2480	MHz
Max. Transmit Power	π/4 DQPSK				10	dBm
	8PSK				10	dBm
Relative Transmit Power	π/4 DQPSK			8		dB
	8PSK			8		dB
Frequency Stability	Max. carrier frequency stability, ωo	π/4 DQPSK		0		kHz
		8PSK		0		kHz
	Max. carrier frequency stability, ωi	π/4 DQPSK		±10		kHz
		8PSK		±10		kHz
	Max. carrier frequency stability, |ωo + ωi|	π/4 DQPSK		±10		kHz
		8PSK		±10		kHz
Modulation Accuracy	RMS DEVM	π/4 DQPSK			20	%
		8PSK			13	%
	99% DEVM	π/4 DQPSK			30	%
		8PSK			20	%
	Peak DEVM	π/4 DQPSK			35	%
		8PSK			25	%
In-Band	±1MHz offset	π/4 DQPSK		-42		dB
	±1MHz offset	8PSK		-42		dB
Spurious Emissions	±2MHz offset	π/4 DQPSK		-46		dBm
	±2MHz offset	8PSK		-46		dBm
	±3MHz offset	π/4 DQPSK		-48		dBm
	±3MHz offset	8PSK		-48		dBm

4.10.2.5 Bluetooth Low Energy (BLE) Receiver Performance

Table 4-18 BLE receiver performance

Parameter	**Condition**	**Performance**			**Unit**
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	2440	2480	MHz
Receiver Sensitivity	PER<30.8%		-99		dBm
Max. Usable Signal	PER<30.8%		0		dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		5		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-7		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-48		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-56		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-25		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-29		dB

Inter-modulation			-27		dBm
Out-of-band blocking	30MHz to 2000MHz	-30			dBm
	2003MHz to 2399MHz	-35			dBm
	2484MHz to 2997MHz	-35			dBm
	3000MHz to 12.75GHz	-30			dBm

4.10.2.6 Bluetooth Low Energy (BLE) Transmitter Performance

Table 4-19 BLE transmitter performance

Parameter	Condition	Performance			Unit
		Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402	2440	2480	MHz
Output Power	At max. power output level		8	10	dBm
Carrier Frequency Offset and Drift	Frequency offset		±10		kHz
	Frequency drift		±10		kHz
	Max. drift rate		±10		kHz
Modulation characteristics	Δf1 avg.		250		kHz
	Δf2 max.	185			kHz
	Δf1 avg./Δf2 avg.		0.93		
In-Band Emissions	±2MHz offset		-51		dBm
	≥ ±3MHz offset		-53		dBm

4.11 Audio Characteristics

4.11.1 Audio ADC

Table 4-20 Analog performance of recording path

Parameter	Conditions		Min.	Typ.	Max.	Unit
Sample rate	8/16/32/44.1/48/88.2/96kHz		8	48	96	kHz
Bit width	Configured by I2S interface data length		8	16	24	Bits
Analog supply voltage (VAM_AUD)	Powered by system power source		1.71	1.8	1.95	V
Reference voltage (LDOA_OUT)	From reference generator LDO			1.8		V
MICBIAS	LDO for analog microphone			1.8		V
MIC boost gain	0/5/10/15/20/25/30/35/40		0	20	40	dB
ADC channel variation	Measured at -10dBV@1kHz input			±0.2		dB
MICBIAS noise floor	MICBIAS=1.8V, load=3mA			-100		dBV
SNR	B/W=20Hz~20kHz, A-weighted, 0dB gain, VAM_AUD =1.8V	Single-ended mode		98		dBA
		Differential mode		98		dBA
THD+N @-3dBFS output	VAM_AUD=1.8V, 0dB gain, single-ended mode			-80		dB
	VAM_AUD=1.8V, 0dB gain, differential mode			-80		dB

4.11.2 Audio DAC

Table 4-21 Analog performance of playback path

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sample rate	8/16/22.05/32/44.1/48/88.2/96/192kHz	8	48	192	kHz
Bit width	Configured by I2S interface data length	8	16	24	Bits
Analog supply voltage (VAM_AUD)	Powered by system power source	1.71	1.8	1.95	V
Reference voltage (LDOA_OUT)	From reference generator LDO		1.8		V
Output amplitude	Single-ended mode		0.5		Vrms
	Differential mode		1		Vrms
SNR	B/W=20Hz~20kHz, A-weighted, load=10kΩ, VAM_AUD=1.8V, differential mode		98		dBA
Noise floor	B/W=20Hz~20kHz, A-weighted, load=10kΩ,		-100		dBV

	VAM_AUD=1.8V, differential mode				
THD+N @0dBFS output	Load=10kΩ, VAM_AUD=1.8V, differential mode		-85		dB

4.12 General ADC Characteristics

Table 4-22 ADC characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
VAH_AUX	Analog power supply			2.97	3.3	3.63	V
fs	ADC sample frequency			31.25	166.67	250	kHz
V_{IN}[1]	Conversion input voltage range	External channel (ch0 ~ ch5)		0	-	Min(3.3, VAH_AUX)	V
R	Input impedance	External channel (ch0 ~ ch5)		412	491	574	kΩ
t_{STAB}	ADC total power-up time	Including internal BG/LDO/ADC power-up time		-	-	220	μs
Resolution				-	12	-	bits
EO	Offset error	fs = 166.67kHz V_{DDA} = 3.3 V T = 25°C	Single-ended	-	±2	±3	LSB
			Differential	-	±2	±3	
EG	Gain error		Single-ended	-	±1	±3	
			Differential	-	±1	±3	
INL	Integral linearity error		Single-ended	-5.5	-	4.3	
			Differential	-2	-	3.6	
DNL	Differential linearity error		Single-ended	-1	-	2	
			Differential	-1	-	2	
SFDR	Spurious free dynamic range		Single-ended	-	54	-	dB
			Differential	-	53	-	
THD	Total harmonic distortion		Single-ended	-	-50	-	
			Differential	-	-51	-	
SNR[2]	Signal-to-noise ratio		Single-ended	-	62	-	
			Differential	-	62	-	
ENOB[2]	Effective number of bits		Single-ended	-	10	-	bits
			Differential	-	10	-	

NOTE

[1] Conversion input voltage range: 0~3.3V (if VAH_AUX >= 3.3V) or 0~ VAH_AUX (if VAH_AUX < 3.3V).

[2] It is ADC performance which does not include harmonic distortion.

4.13 QSPI Flash Controller Characteristics

This section describes the timing characteristics of the Quad Serial Peripheral Interface (QSPI) for Flash controller.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V.
- The process includes all corners.

Table 4-23 Timing data of QSPI Flash controller

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SCL}	Clock period	Master	10	-	ns
t_{LOW}	Clock Low time	Master	45%*T_{SCL}	55%*T_{SCL}	ns
t_{HIGH}	Clock High time	Master	45%*T_{SCL}	55%*T_{SCL}	ns
t_r	Data/Clock raise time	Master	-	1	ns
t_f	Data/Clock fall time	Master	-	1	ns
$t_{SU;DAT(I)}$	Data input setup time	Master	2	-	ns
$t_{HD;DAT(I)}$	Data input hold time	Master	1	-	ns
$t_{SU;DAT(O)}$	Data output setup time	Master	(T_{SCL}/2)-2	-	ns
$t_{HD;DAT(O)}$	Data output hold time	Master	(T_{SCL}/2)-1	-	ns
$t_{VD;DAT(O)}$	Data output valid time	Master	-1	1	ns

$t_{SU;CS(A)}$	CS active setup time relative to CLK	Master	$(T_{SCL}/2)-1$	-	ns
$t_{HD;CS(A)}$	CS active hold time relative to CLK	Master	$T_{SCL}-1$	-	ns

NOTE

- *The timing data of $t_{SU;DAT(I)}$ is only applicable to clock frequency of 20MHz or below. When QSPI needs a faster clock frequency, the RTL8726EA would activate a special sampling mechanism internally.*
- *The timing data of $t_{SU;CS(A)}$ and $t_{HD;CS(A)}$ can be adjusted by configuring registers, and the adjustment unit is TSCL/2.*

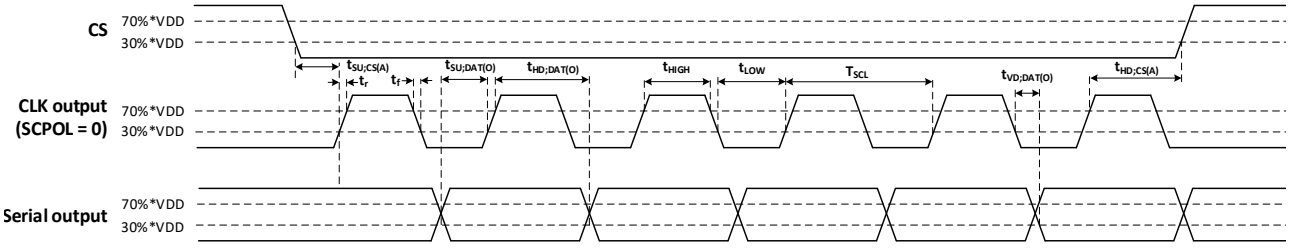


Figure 4-6 Output timing diagram (SCPH = 0)

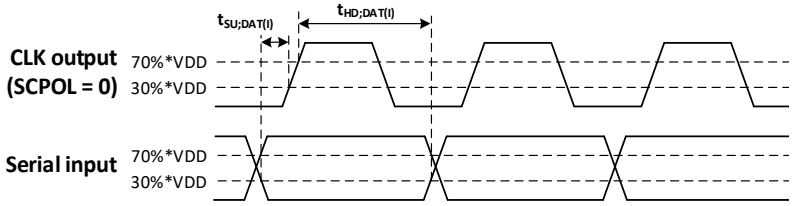


Figure 4-7 Input timing diagram (SCPH = 0)

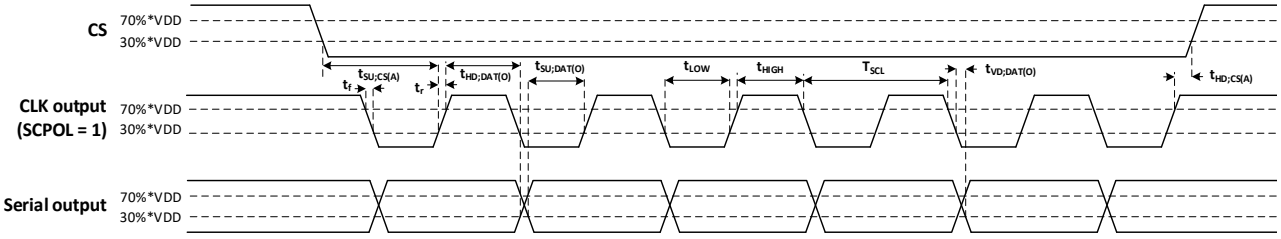


Figure 4-8 Output timing diagram (SCPH = 1)

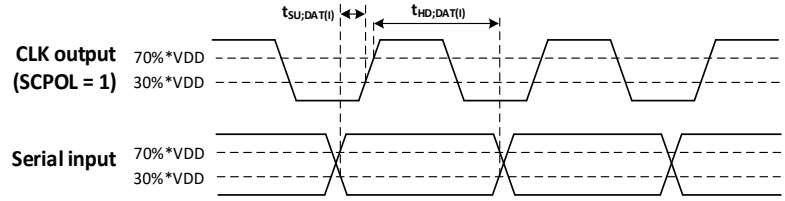


Figure 4-9 Input timing diagram (SCPH = 1)

4.14 SPI Characteristics

The SPI function of RTL8726EA is divided into dedicated SPI and full-matrix SPI, refer to Section *2.3* for the function comparison between them.

The dedicated SPI has the following features:

- Limited choices with fixed group usage, that is to say, only the specified pins configured as function ID6 can be used in combination:
  - Group 1: PA28, PA29, PA30, PA31
  - Group 2: PB2, PB3, PB4, PB5
  - Group 3: PB7, PB8, PB9, PB10
  - Group 4: PB12, PB14, PB17, PB19
- Better timing performance compared to full matrix SPI.

The full-matrix SPI has the following features:

- More combinations and each pin signal can be flexibly configured, that is to say, more pins that can be freely configured as individual

signals of SPI function ID (ID32 (SPI1_CLK), ID33 (SPI1_MISO), ID34 (SPI1_MOSI), ID35 (SPI1_CS)), and can be used in any combination.
- Limited timing performance.

All measurements are tested under the following conditions:
- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE
- *Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.*
- *When the pins of Group 4 are used as SPI, the I/O power can only be fixed at 1.8V (typical).*

Table 4-24 Timing data of dedicated SPI

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	20	-	20	-	ns
		Slave	40	-	40	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	1.5*T_{SCL} -2	-	1.5* T_{SCL} -2	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	T_{SCL} -2	-	T_{SCL} -2	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	T_{SCL} -2	-	T_{SCL} -2	-	ns
		Slave	-	9	-	15	ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-1	1	-1	1	ns
		Slave	-	10	-	15	ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	3	-	3	-	ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	2	-	2	-	ns

NOTE
- *The maximum value of $t_{VD;DAT(SO)}$ is already greater than half of a 50M clock cycle, so when used as a slave, the maximum speed supported by SPI is 25MHz. But if the connected master supports sampling with a delay, it could support higher clock frequency.*
- *The timing data of $t_{SU;DAT(MI)}$ is only applicable to speeds of 25MHz or below. When the RTL8726EA is used as a master running at 50MHz, due to the sample delay function of IC, the accepted minimum value of $t_{SU;DAT(MI)}$ can be -5ns for 3.3V I/O and 0ns for 1.8V I/O.*

Table 4-25 Timing data of full-matrix SPI

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	40	-	40	-	ns
		Slave	80	-	80	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	1.5*T_{SCL} -5	-	1.5* T_{SCL} -5	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	T_{SCL} -5	-	T_{SCL} -5	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	T_{SCL} -4	-	T_{SCL} -4	-	ns
		Slave	-	11	-	16	ns
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-4	4	-4	4	ns
		Slave	-	12	-	17	ns
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	4	-	4	-	ns
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	4	-	4	-	ns

NOTE

If the connected master supports sampling with a delay, the SPI slave could support higher speed.

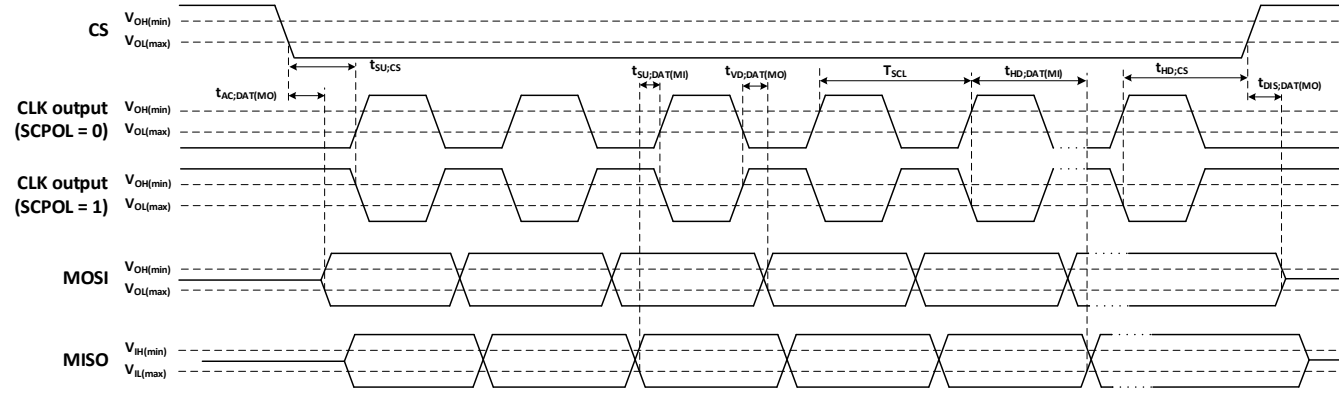


Figure 4-10 Timing diagram for master (SCPH = 0)

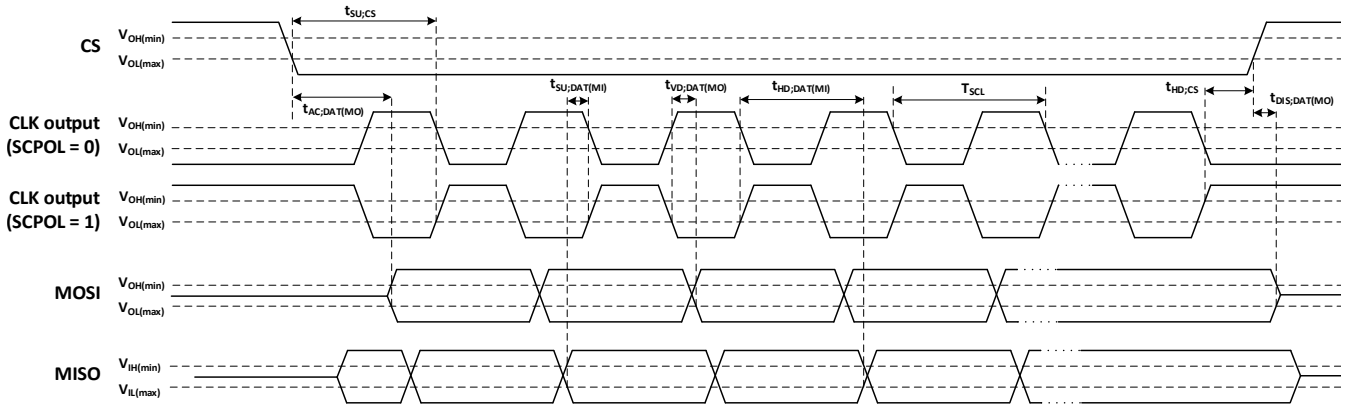


Figure 4-11 Timing diagram for master (SCPH = 1)

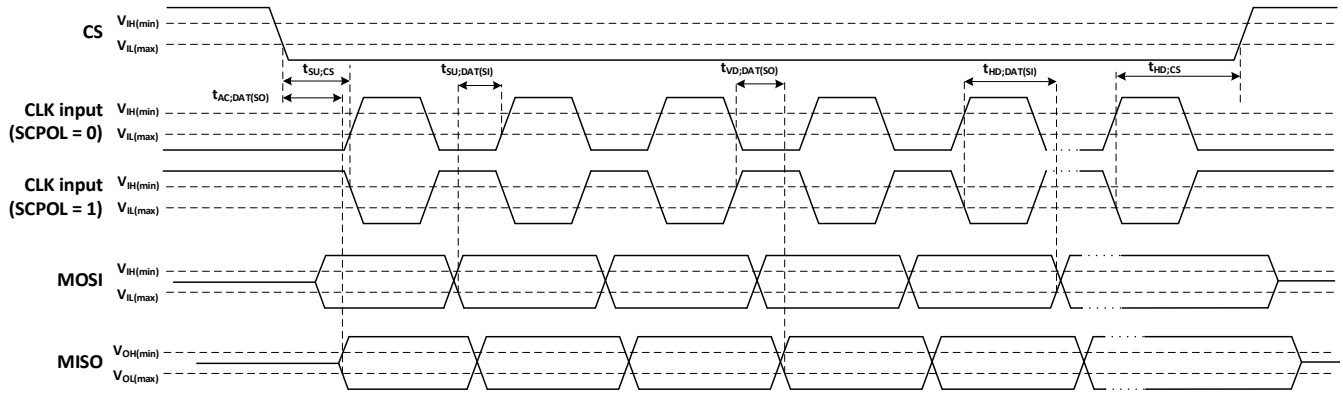


Figure 4-12 Timing diagram for slave (SCPH = 0)

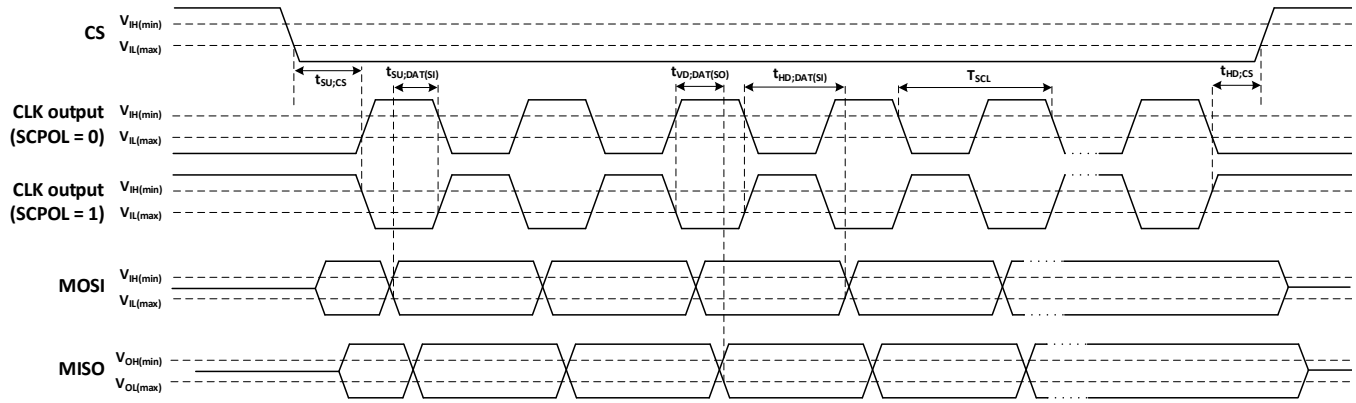


Figure 4-13 Timing diagram for slave (SCPH = 1)

4.15 I2C Characteristics

All measurements are tested under the following conditions:

- The maximum loading is 400pF (SS mode and FS mode), 100pF (HS mode).
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

Table 4-26 Timing data of I2C (FS/SS mode)

Symbol	Parameter	Standard mode (Cb=400pF max.)		Fast mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	-	100	-	400	kHz
$t_{HD;STA}$	Hold time START condition	4	-	0.6	-	µs
t_{LOW}	Low period of the SCL clock	Programmable		Programmable		µs
t_{High}	High period of the SCL clock					µs
t_r	Raise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	12	300	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	us
$t_{SU;DAT}$	Data set-up time	0.25	-	0.1	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4	-	0.6	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs

NOTE

- *Cb is the capacitive load for each bus line.*
- *The resistance value of the pull-up resistor needs to be calculated and determined according to the loading on the bus.*

Table 4-27 Timing data of I2C (HS mode)

Symbol	Parameter	High-Speed mode (Cb=100pF max.)		High-Speed mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	-	3.4	-	1.7	MHz
$t_{HD;STA}$	Hold time START condition	160	-	160	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	160	-	160	-	ns
$t_{HD;DAT}$	Data hold time	0	70	0	150	ns
$t_{SU;DAT}$	Data set-up time	10	-	10	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	160	-	160	-	ns
t_{high}	High period of the SCL clock	Programmable		Programmable		ns
t_{low}	Low period of the SCL clock					ns
t_{rCL}	Rise time of SCLH signal	10	40	20	80	ns

t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	20	160	ns
t_{rDA}	Rise time of SDAH signal	10	80	20	160	ns
t_{fCL}	Fall time of SCLH signal	10	40	20	80	ns
t_{fDA}	Fall time of SDAH signal	10	80	20	160	ns

NOTE

- *Cb is the capacitive load for each bus line.*
- *The resistance value of the pull-up resistor needs to be calculated and determined according to the loading on the bus.*

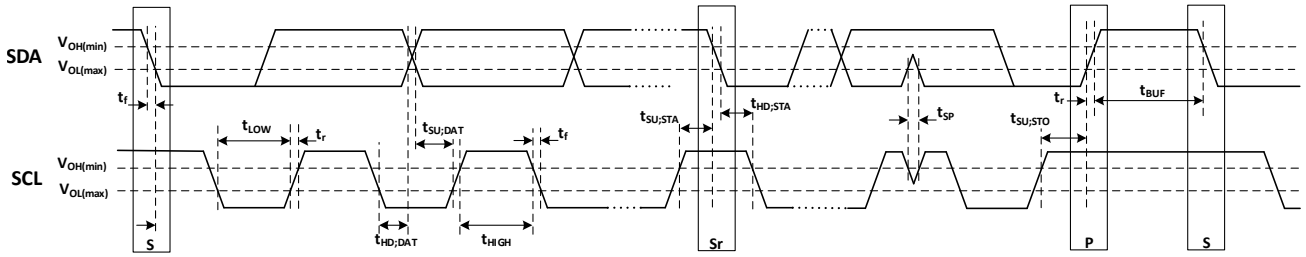


Figure 4-14 Timing diagram of I2C (FS/SS mode)

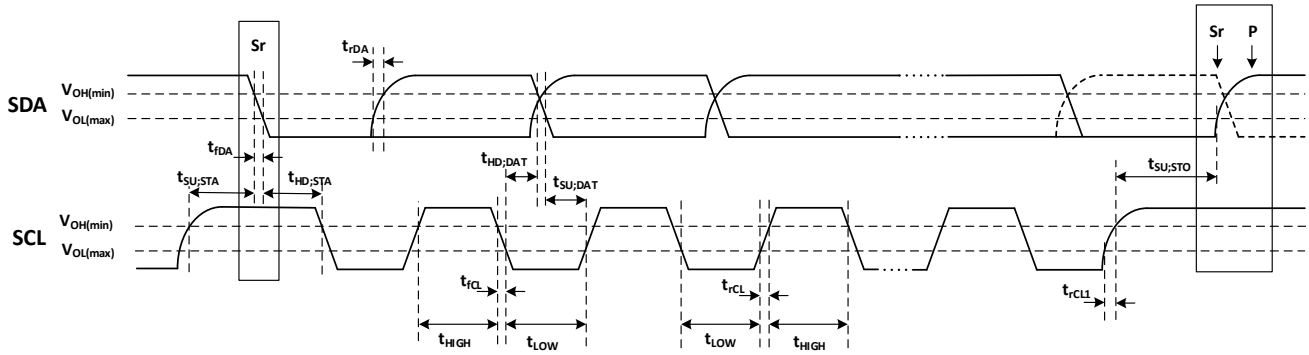


Figure 4-15 Timing diagram of I2C (HS mode)

NOTE

In HS mode, the first rising edge of SCLH signal after a repeated start condition is push-pull output instead of open-drain output.

4.16 UART Characteristics

All measurements are tested under the following conditions:

- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-28 Timing data of UART

Item	Conditions	Min.	Typ.	Max.	Unit
Transfer rate	TXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 2MHz OSC			115200	bps

NOTE

Total baud rate error shall be less than 3% in order to communicate correctly, which includes three parts: the error of real baud rate of Tx device and expected communication baud rate, the frequency drift of Rx IP clock, and the calculation baud error of Rx device. Users can enable the function of monitoring baud rate of Rx data to decrease the baud rate error.

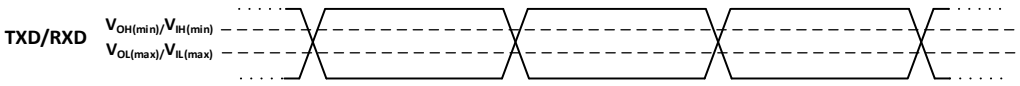


Figure 4-16 Timing diagram of UART

4.17 I2S Characteristics

The Inter-IC Sound (I2S) supports both master and slave operations. The following tables and diagrams provide timing characteristics for I2S.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-29 Timing data of dedicated I2S

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	I2S clock	Master	41	1953	41	1953	ns
		Slave	41	1953	41	1953	ns
Duty	Clock duty	Master	45	55	45	55	%
		Slave	35	65	35	65	%
$t_{SU;DAT(I)}$	Input data setup time	Master	11	-	16	-	ns
$t_{SU;DAT(I)}$/$t_{SU;WS}$	Input data/WS setup time	Slave	4	-	4	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Master	0	-	0	-	ns
		Slave	4	-	4	-	ns
$t_{VD;DAT(O)}$	Output data valid time	Master	-5	5	-5	5	ns
$t_{VD;WS}$	Output WS valid time	Master	-5	5	-5	5	ns
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	13	-	18	ns

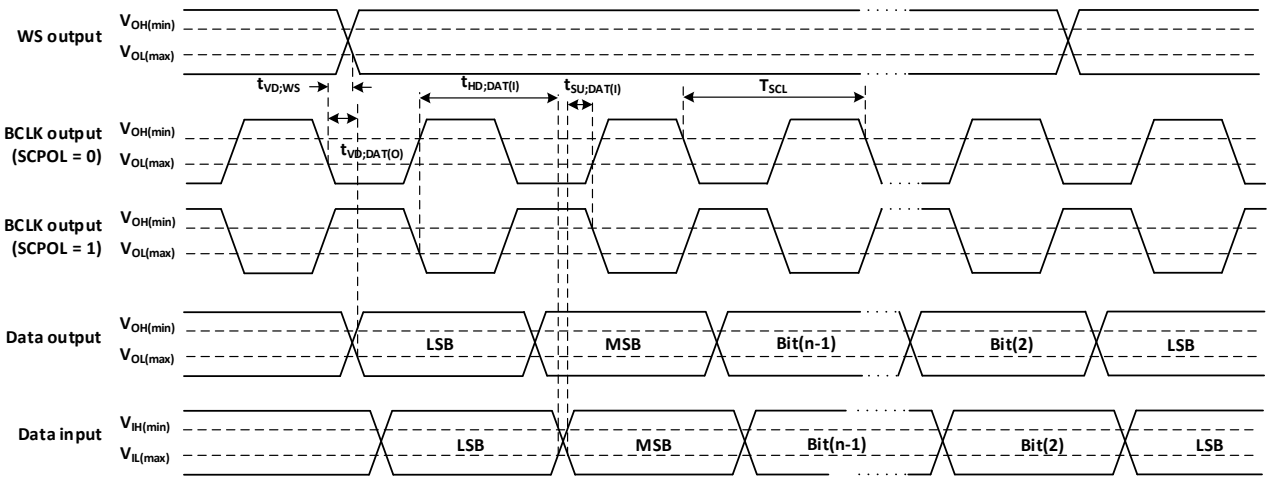


Figure 4-17 Timing diagram for I2S master

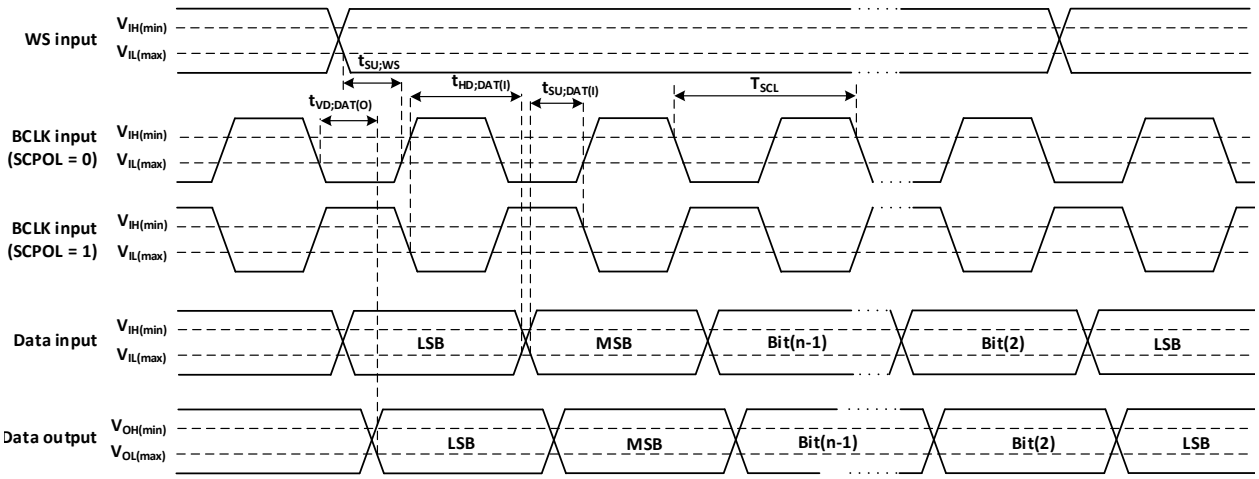


Figure 4-18 Timing diagram for I2S slave

4.18 DMIC Characteristics

The Digital Microphone (DMIC) supports only master operations. The following tables and diagrams provide timing characteristics for DMIC.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-30 Timing data of DMIC

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	DMIC clock period	Master	200	32000	20	32000	ns
Duty cycle	DMIC clock duty cycle	Master	45	55	45	55	%
$t_{SU;DAT(R)}$/$t_{SU;DAT(F)}$	Input data rising/falling edge setup time	Master	13	-	13	-	ns
$t_{HD;DAT(R)}$/$t_{HD;CS(F)}$	Input data rising/falling edge hold time	Master	2	-	2	-	ns

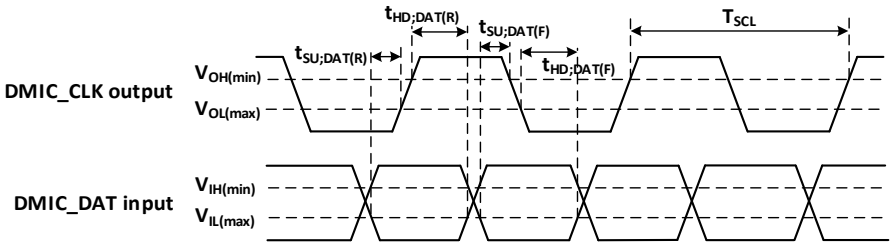


Figure 4-19 Timing diagram of DMIC

4.19 PDM Characteristics

The Pulse Density Modulation (PDM) supports only master operations.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-31 Timing data of PDM

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	PDM clock period	Master	150	400	150	400	ns
Duty cycle	PDM clock duty cycle	Master	45	55	45	55	%
$t_{VD;DAT(R)}/t_{VD;DAT(F)}$	Output data rising/falling edge valid time	Master	24	26	24	26	ns

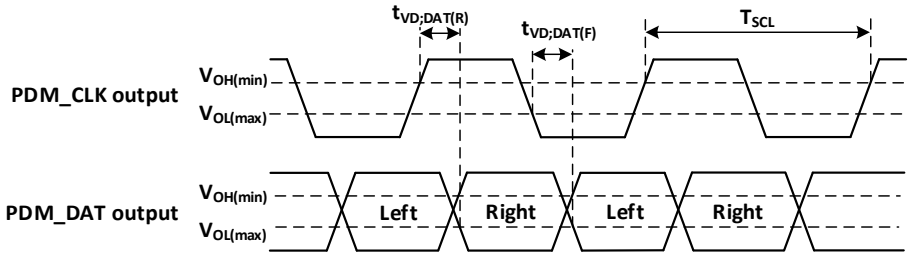


Figure 4-20 Timing diagram of PDM

4.20 Debug Interface Characteristics

The debug interface of RTL8726EA includes Arm standard bi-directional Serial Wire Debug (SWD) and cJTAG.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The junction temperature of IC is between -40°C and 125°C.
- The I/O ports are configured with high driving strength.
- The I/O operating voltage ranges from 2.97V to 3.63V or 1.7V to 1.95V.
- The process includes all corners.

NOTE

Refer to Section 4.8 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

4.20.1 SWD

Table 4-32 Timing data of SWD

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SWCLK clock period	Slave	50	-	50	-	ns
Duty cycle	Input clock duty cycle	Slave	30	70	30	70	%
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	11	-	17	ns
$t_{VD;DAT(I)}$	Input data setup time	Slave	2	-	2	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Slave	2	-	2	-	ns

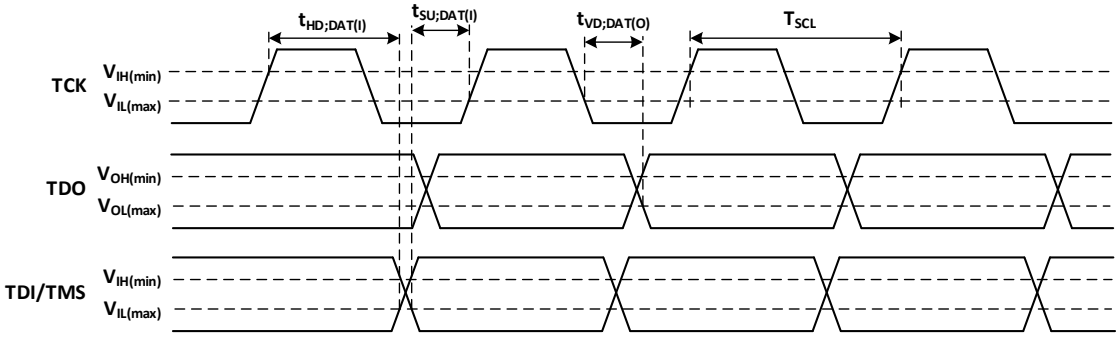


Figure 4-21 Timing diagram of SWD

4.20.2 cJTAG

Table 4-33 Timing data of cJTAG

Symbol	Parameter	Conditions	3.3V I/O		1.8V I/O		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	TCK clock period	Slave	50	-	50	-	ns
Duty cycle	Input clock duty cycle	Slave	30	70	30	70	%
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	11	-	17	ns
$t_{VD;DAT(I)}$	Input data setup time	Slave	2	-	2	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Slave	2	-	2	-	ns

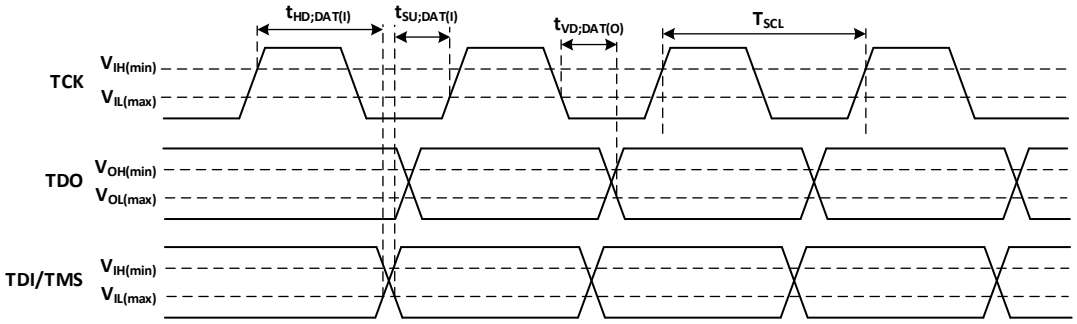


Figure 4-22 Timing diagram of cJTAG

5 Package Information

In order to meet environmental requirements, Realtek offers devices in different grades of ECOPACK® packages, depending on the level of environmental compliance.

5.1 QFN68 Package Outline

The QFN68 is a 68-pin, 8mm x 8mm quad flat no-leads package with 0.4mm pitch.

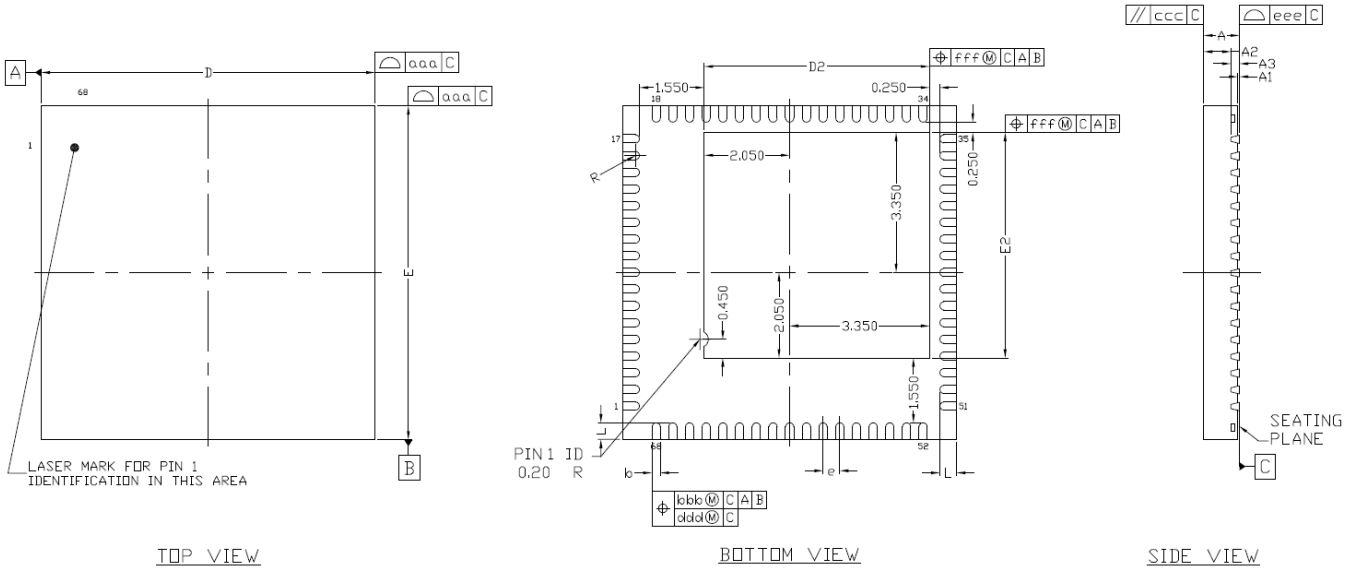


Figure 5-1 QFN68 package outline

Table 5-1 QFN68 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.800	0.850	0.900	0.031	0.033	0.035
A1	0.000	-	0.050	0.000	-	0.002
A2	-	0.650	0.700	-	0.026	0.028
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	8 BSC			0.315 BSC		
D2	5.300	5.400	5.500	0.209	0.213	0.217
E	8 BSC			0.315 BSC		
E2	5.300	5.400	5.500	0.209	0.213	0.217
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M.-1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

5.2 Thermal Characteristics

Table 5-2 Package thermal characteristics (QFN, 68-pin)

Symbol	Parameter[1]	Condition	Value[2][3]	Unit
θ_{JA}	Junction-to-ambient thermal resistance	16mm x 29mm 4-layer PCB with no air flow	61.7	°C/W
Ψ_{JT}	Junction-to-top center thermal characterization parameter	16mm x 29mm 4-layer PCB with no air flow	0.36	
Ψ_{JB}	Junction-to-board thermal characterization parameter	16mm x 29mm 4-layer PCB with no air flow	5.1	

NOTE

[1] Refer to EIA/JESD51-2, Integrated circuit Thermal Test Method Environment Conditions – Natural Convection (Still Air) for more information.

[2] These values are based on customized PCB systems designed by Realtek Semiconductor Corp. and will vary in function of board thermal characteristics and other components on the board.

[3] An ambient temperature of 85°C is assumed.

Revision History

Date	Revision	Release Notes
2025-03-20	4.6	● Updated the Bluetooth feature to support ISO ● Updated the ordering information
2024-10-31	4.5	● Updated the following sections: ■ *Power Domain* ■ *Power Mode* ● Updated the features of *WLAN MAC*
2024-06-17	4.4	● Updated the features of Bluetooth in *Table 1-1 General features* ● Updated *Table 4-2 Recommended operation conditions* ● Updated *Table 4-23 Timing data of QSPI Flash controller* ● Updated the following sections: ■ *General Features* ■ *Power Sequence* ■ *Maximum Power Consumption*
2024-04-19	4.3	● Added the section: *UART Characteristics* ● Updated the following sections: ■ *Thermal Sensor* ■ *Power Consumption Characteristics* ■ *SPI Characteristics* ■ *I2S Characteristics*
2023-12-22	4.2	● Updated the section: *SPI Characteristics* ● Updated *Table 1-1 General features* ● Updated *Table 4-1 Absolute maximum ratings* ● Updated *Table 4-13 WLAN 2.4GHz band transmitter performance* ● Updated the section: *RF Power Consumption*
2023-08-24	4.1	Updated the section: *General Analog-to-Digital Converter (ADC)*
2023-08-18	4.0	● Added the section: *Thermal Characteristics* ● Optimized the feature description of *WLAN Baseband* ● Updated *Table 4-2 Recommended operation conditions* ● Updated the note of *Table 4-8 I/O types* ● Updated *Table 4-22 ADC characteristics*
2023-05-30	3.0	● Optimized the content structure of Datasheet ● Added sections and values to the chapter: *Electrical Characteristics*
2022-09-21	2.0	● Updated the product description and features ● Added the section: *Unmanned Peripheral System (UPS)* ● Updated the section: *WLAN MAC*
2022-06-22	1.5	Updated the details
2022-05-05	1.4	● Updated the following sections: ■ *Power Structure* ■ *Pin Assignments* ■ *Pin Description* ● Optimized the pin names for easy understanding
2022-03-25	1.3	● Added the section: *Power Supply for Pins* ● Updated the description of CPUs
2022-02-25	1.2	● Updated *Figure 5-1 QFN68 package outline* ● Updated *Table 5-1 QFN68 package mechanical data* ● Added the following sections: ■ *RF Subsystem* ■ *WLAN Subsystem* ■ *Bluetooth Subsystem*
2022-01-14	1.1	Added the section: *Reset and Clock Control (RCC)*
2021-12-10	1.0	Initial release