RTL8730E Hardware Design Guide

This document provides the Hardware design guide and notes

Rev. 2.3

Jul. 2025

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document provides the Hardware design guide and notes for the RTL8730E (including RTL8730EAH/RTL8730ELH/RTL8730ELM series). Please refer to RTL8730E_PCB_Layout_and_Assembly_Guide.pdf for layout

2 Power Supplement

2.1 Power Structure

Only an external power supply is required for the RTL8730E. All the other required voltages can be converted and output by two three embedded DC-DC switching regulators (DCDC). Embedded DC-DC have voltage-scaling and mode-switching function, which can effectively reduce power consumption. It is suggested to use embedded DC-DC powering RTL8730E.

2.1.1 Power Structure A for all series of RTL8730E

Power structure A is applicable to all series of RTL8730E and is the default configuration of all RTK RTL8730E evaluation board.

- The DCDC_CORE outputs typical 0.8V, 0.9V or 1.0V for low voltage circuits including digital system, USB and memory controller, etc., and 0.8V, 0.9V or 1.0V is controlled by the software based on application requirements.
- The DCDC_MEM outputs typical 1.35V or 1.8V for embedded memory including PSRAM or DDR, and 1.35V or 1.8V is controlled by the software based on the type of embedded memory.
- The DCDC_AUD outputs typical 1.8V for audio and radio frequency (RF) circuits.

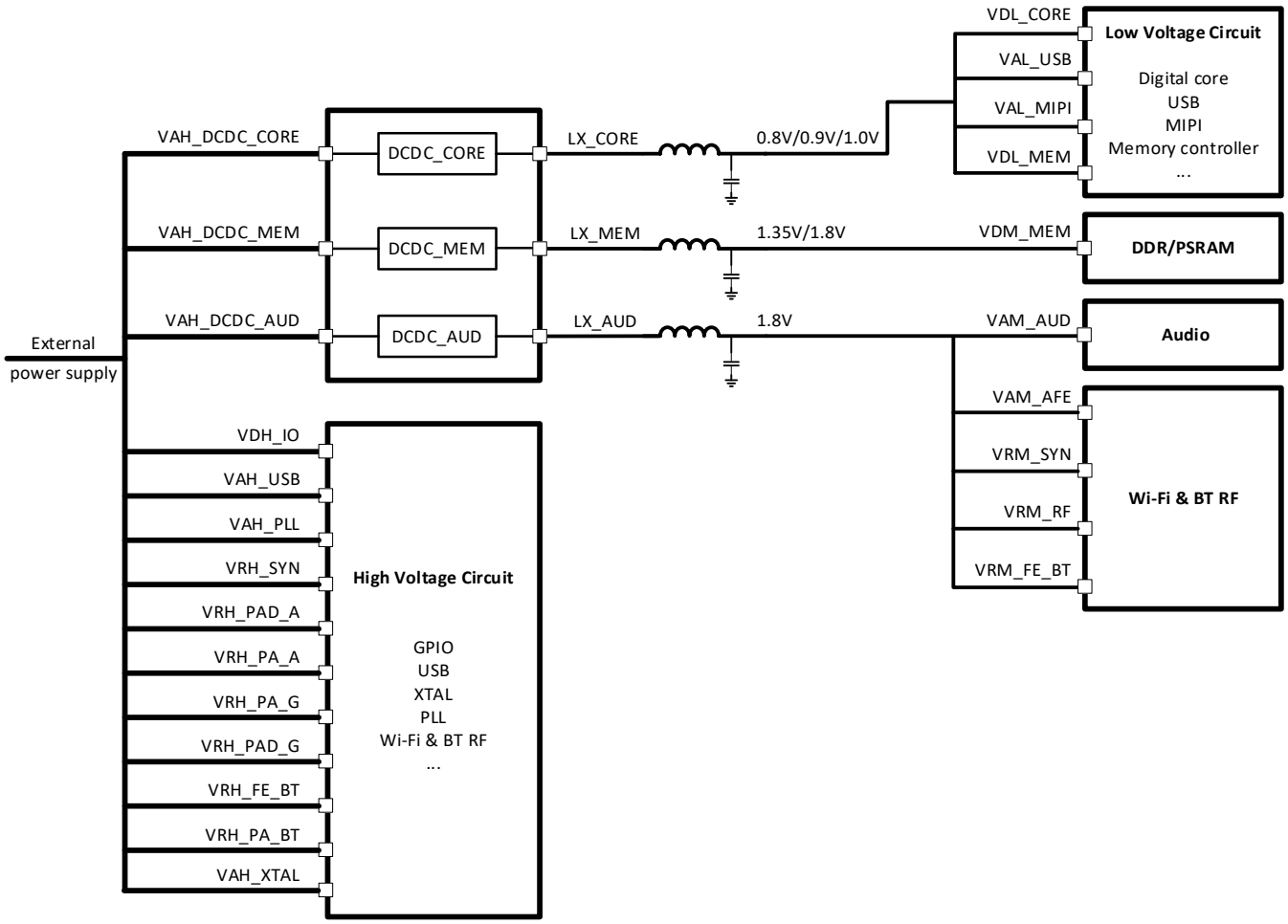


Figure 2-1 Power block diagram for all series of RTL8730E

2.1.2 Power Structure B for RTL8730ELH-VA3 and RTL8730EAH-VA3/VD3

Power structure B is applicable to RTL8730ELH-VA3 and RTL8730EAH-VA3/VD3. Compared to power structure A, DCDC_AUD related in and out capacitor and inductance can be saved in power structure B.

- The PSRAM, audio and RF circuits are powered by DCDC_MEM and the typical output voltage for DCDC_MEM is 1.8V.
- The DCDC_AUD is not used and the related circuit components are not needed.

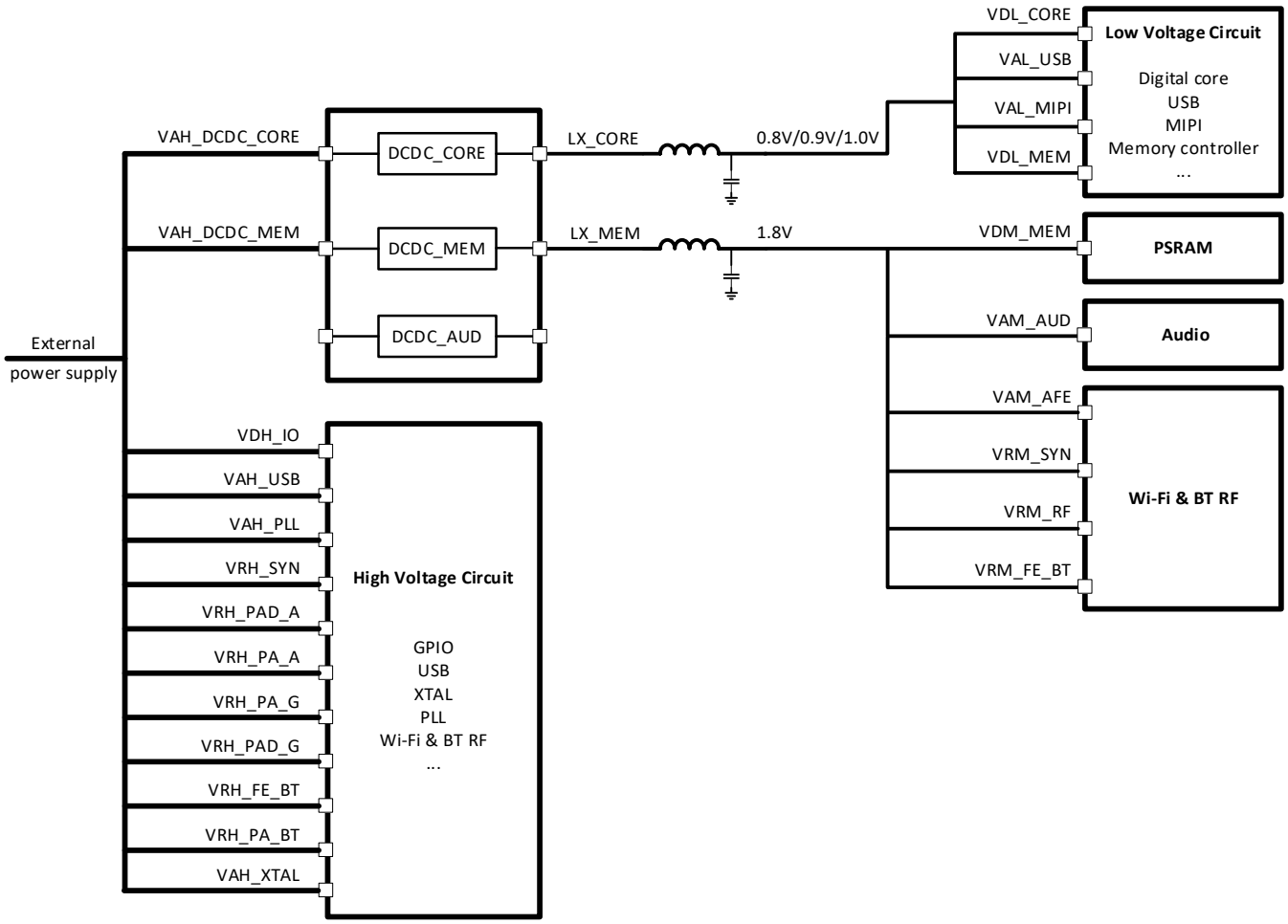
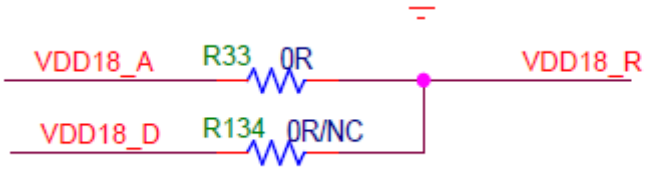


Figure 2-2 Power block diagram for RTL8730ELH-VA3 and RTL8730EAH-VA3/VD3

There is options in evaluation board EV730EA which can switch power structure from default A to B. In the figure below, VDD18_A is the output from DCDC_AUD, VDD18_D is the output from DCDC_MEM, VDD18_R is the power for RF and Audio circuits. VDD18_R is powered by VDD18_A by default which is power structure A. VDD18_R can also be powered by VDD18_D by removing R33 and adding R134 which is power structure B.



If power structure B is selected, related SW configuration needs to be adjusted.
In component\soc\amebad2\usrcfg\ameba_bootcfg.c , Boot_MemSwr_Only needs to be configured as ENABLE.

```
100: BOOT_RAM_DATA_SECTION
101: u8 Boot_MemSwr_Only = DISABLE;
102:
```

2.1.3 Power Supply for I/O Pins

Generally, VDH_IO is powered by typical 3.3V. But there two group of I/O that can also support 1.8V power supply.

- PA9~PA16 are powered by VDH_IO1 which support 1.8V/3.3V IO power
- PB25~PB31 and PC0 are powered by VDH_IO6 which support 1.8V/3.3V IO power

Typical 1.8V power output from DCDC_MEM and DCDC_AUD can be used to powering VDH_IO1 and VDH_IO6 if needed. Please note that output voltage of DCDC_MEM in RTL8730ELH-VA8 and RTL8730ELM-VA8 is 1.35V and don't use it to powering IO power.
Because embedded DCDC_MEM and DCDC_AUD have mode-switching function, which means it will switch between normal mode supporting higher power consumption and low power mode supporting lower power consumption. Mode-switching function is controlled by SW according to the state of RTL8730E. Addition safe maximum power current that can be provided by DCDC_MEM and DCDC_AUD to IO is 10mA. If more power current is needed, please use power from other power sources.

2.2 Capacitors and Inductance for Power Pins

Generally, for DCDC input and output, RF pins, audio pins, embedded memory power pins, large capacitors should be placed. For other power pins, 0.1uF capacitor is needed.

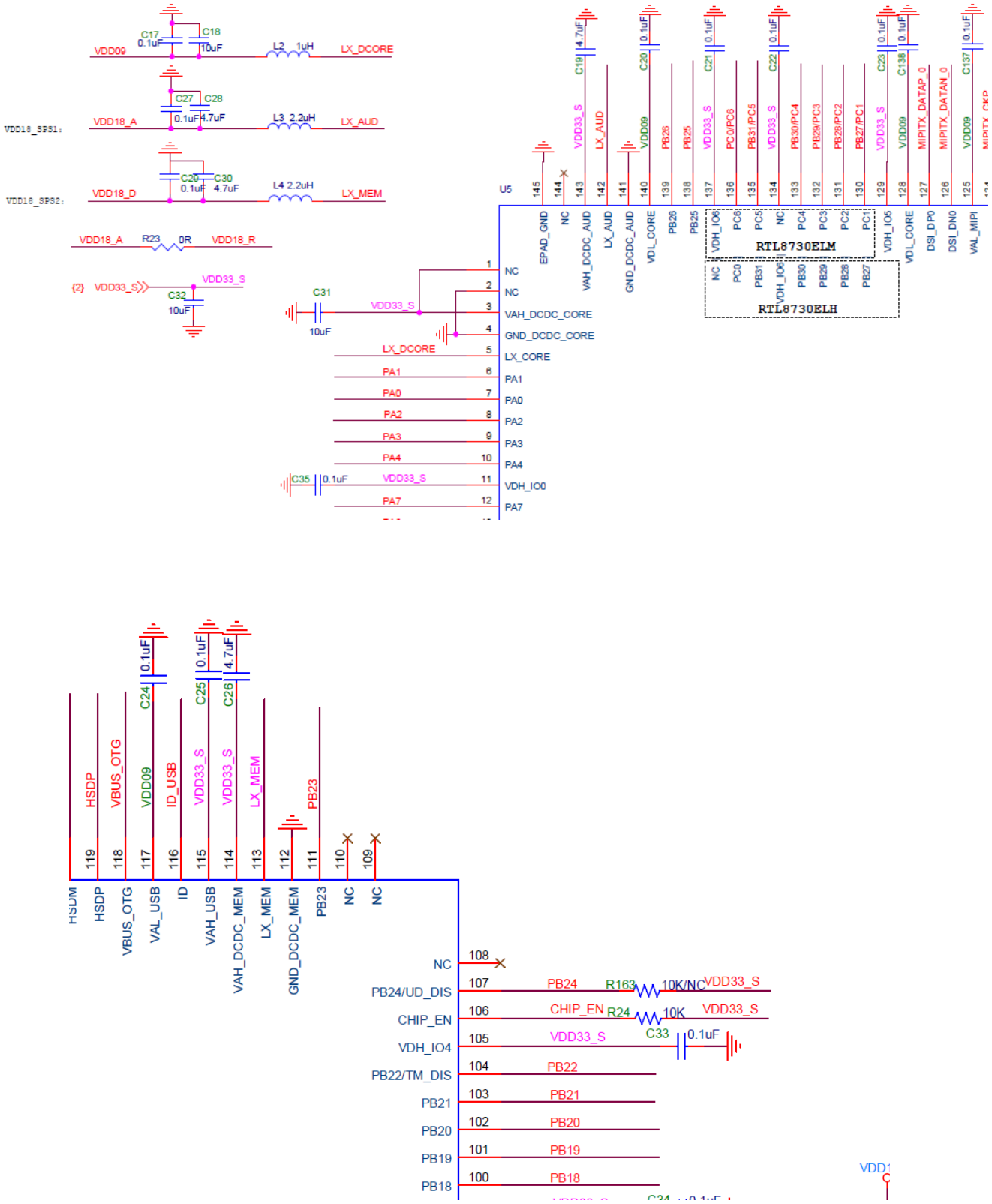
2.2.1 DCDC

Generally, tolerance of capacitors for DCDC needs to be within +/-20%. Suitable capacitor types need to be selected based on the actual operation temperature range.

- C31, C17/C18 are for DCDC_CORE input and output, capacitor 10uF and 0.1uF+10uF is recommended.
- C19, C27/C28 are for DCDC_AUD input and output, capacitor 4.7uF and 0.1uF+4.7uF is recommended.
- C26, C29/C30 are for DCDC_MEM input and output, capacitor 4.7uF and 0.1uF+4.7uF is recommended
- L2,L3,L4 is power inductor for DCDC regulator. You should chose the inductor carefully. The inductor specifications recommended are as follows.

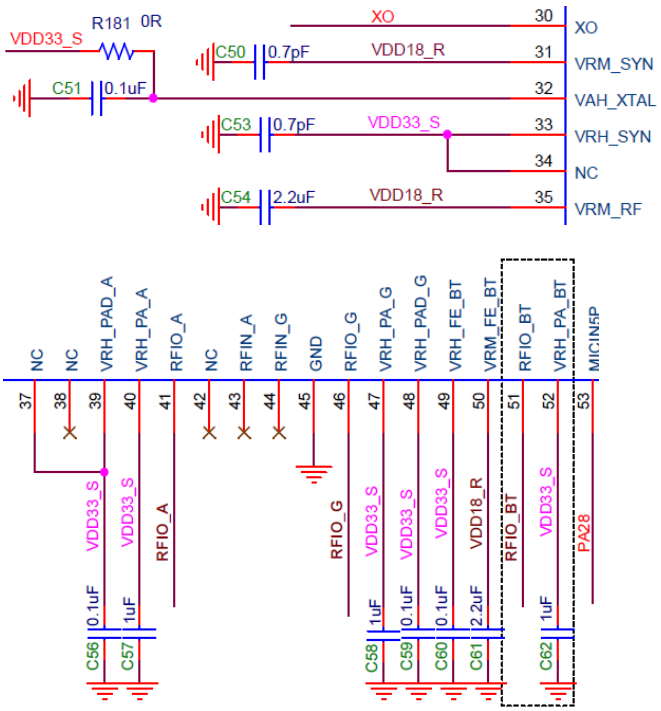
Table 2-1 Recommended specification for power inductance

	Inductance (uH)	**Tol. (%)**	**Saturation Current, ⊿L=30%(mA)**	**Temperature Current, ⊿T=40℃(mA)**	**Rdc(Ω) typ.**
L2	1	20	>= 1200	>= 1200	0.1
L3	2.2	20	>= 860	>= 860	0.1
L4	2.2	20	>= 1300	>= 1300	0.1



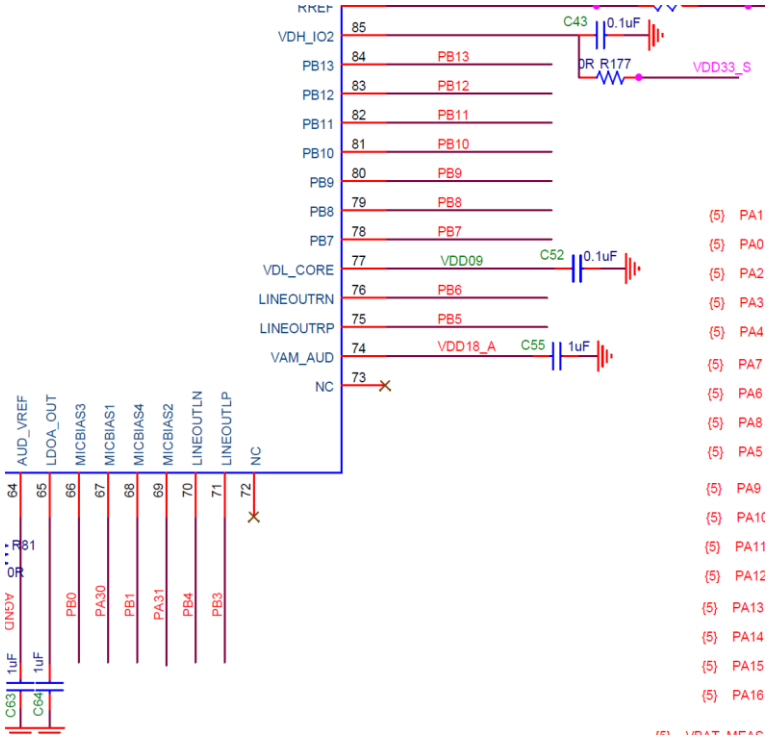
2.2.2 RF Pins

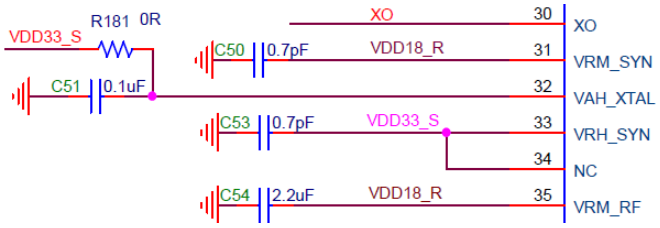
- For reduce VCO leakage radiation，the value of SYN bypass capacitors C50&C53 are recommended to 0.7pF .
- C54 and C61 is for WIFI and BT RF circuits. Capacitor 2.2uF is recommended.
- C57 is for WIFI 5G PA, C58 is for WIFI 2.4G PA and C62 is for BT PA. Capacitor 1uF is recommended.



2.2.3 Audio Pins

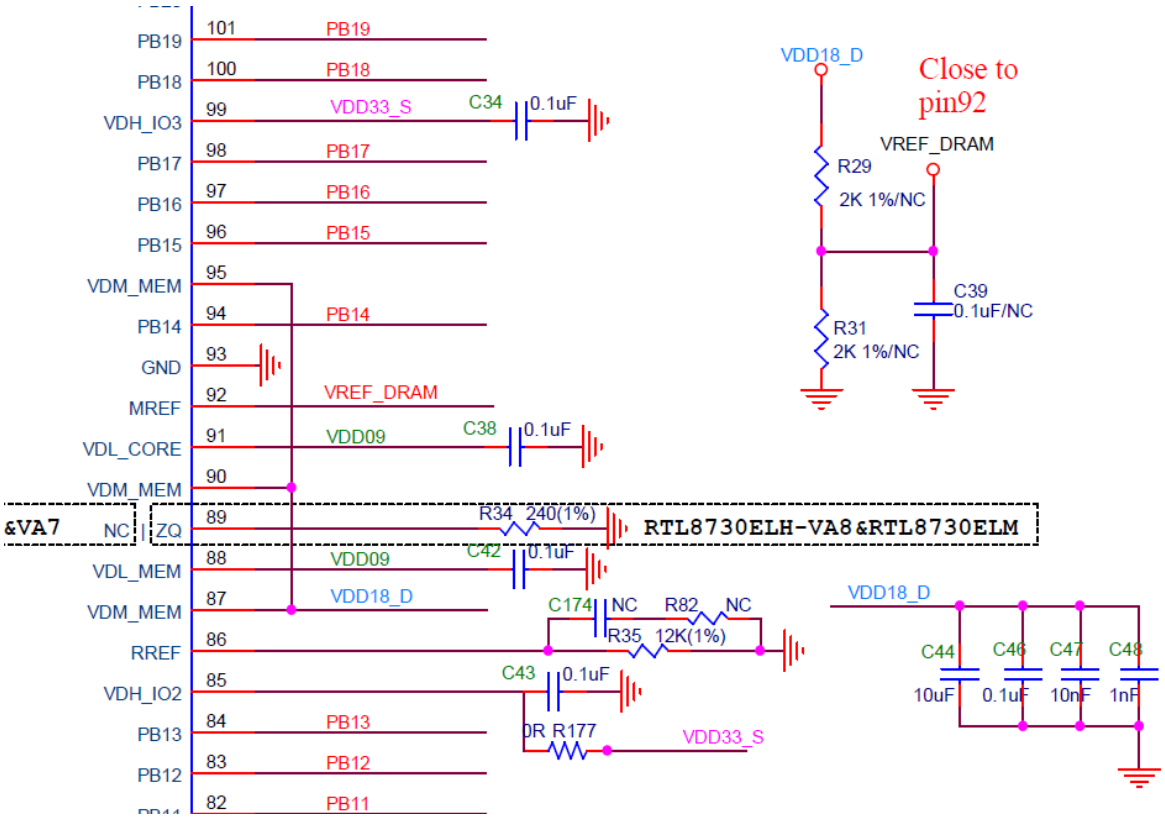
- C55, C63, C64 are for audio circuits input and output, capacitor 1uF is recommended.
- R177 and R181 are reserved resistors used to filter out possible noise to VDH_IO2 and VAH_XTAL, the noise on VDH_IO2 and VAH_XTAL can affect the performance of audio circuits.





2.2.4 Memory Pins

- VDM_MEM is the power supply pin for embedded PSRAM or DDR SDRAM in RTL8730E. C44, C46, C47, C48 are memory input power pin, capacitor 10uF, 0.1uF, 10nF, 1nF are recommended.
- MREF is the optional reference voltage for embedded DDR SDRAM only. R29, R31 and C39 are reserved to providing 1/2 VDM_MEM for MREF and can be left unmounted by default.
- For RTL8730ELH-VA3/RTL8730EAH-VA3/ RTL8730EAH-VD3, there is no need MREF for embedded PSRAM. R29, R31 and C39 are not needed.
- ZQ Pin needs an external reference resistor 240ohm which is 1% accuracy for internal ZQ calibration. ZQ pin is only used in RTL8730ELH-VA8/ RTL8730ELM-VA8. For the other part numbers, 240ohm is not needed.



2.3 External Voltage Regulator Module Recommendation

VXH[1] is the main power supply for Wi-Fi, BT, USB, embedded DC-DC switching regulators, etc. Recommended specification for external VRM is listed in Table 2-2.

- The output voltage of external voltage regulator module can be from 2.97 to 3.63V. Output voltage noise is included in output voltage range.
- The stability of the output power supply is important for RTL8730E. Suggested output voltage ripple should be under +/-100mV. Output voltage ripple should be considered in all possible working states such as WIFI initialization, WIFI TRX, etc. If the VXH is shared with

other high power consuming circuits, such as audio amplifiers, IR circuits, etc., output voltage ripple also needs to be under +/-100mV during the operation of these circuits.

- Continuous output current should be higher than 1A, which excluding power consumption in circuits other than RTL8730E.
- Suggested output voltage rise time needs to be not faster than 0.1ms, more specific power sequence can be found in datasheet.

Table 2-2 External VRM recommended specification

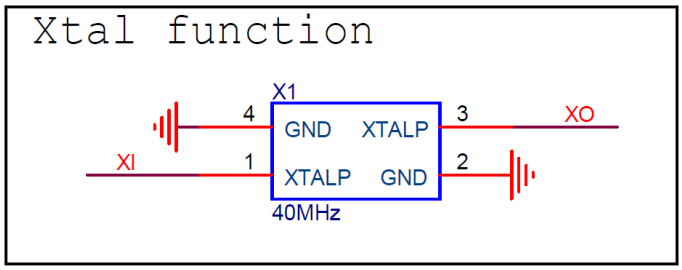
Symbol	Parameter	Operation conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	Including $V_{OUT-RIPPLE}$	2.97	3.3	3.63	V
$V_{OUT-RIPPLE}$	Output voltage ripple	Including all possible operation conditions[1]			+/- 100	mV
I_{OUT}	Continuous output current	Excluding power consumption in circuits other than RTL8730E	1			A
T_{RISE}	Output voltage rise time		0.1	1		ms

[1] VXH *refers to typical 3.3V power supply including VAH_DCDC_CORE, VDH_IO0, VAH_PLL, VRH_SYN, VAH_XTAL, VRH_PAD_A, VRH_PA_A, VRH_PAD_G, VRH_PA_G, VRH_FE_BT, VRH_PA_BT, VDH_IO2, VDH_IO3, VDH_IO4, VAH_DCDC_MEM, VAH_USB, VDH_IO5 and VAH_DCDC_AUD.*

3 Crystal Characteristics

The chip has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.

Please connect crystal XI/XO to main IC directly. There is no need to add extra capacitors on net XI/XO.



The characteristic requirements of external crystal are listed in Table 3-1 .

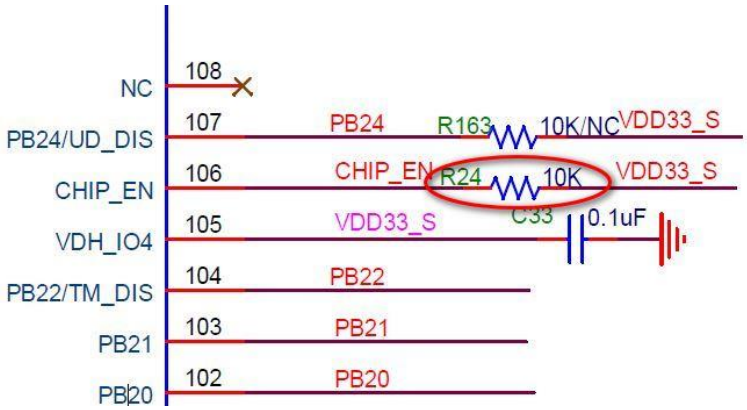
Table 3-1 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

4 CHIP_EN

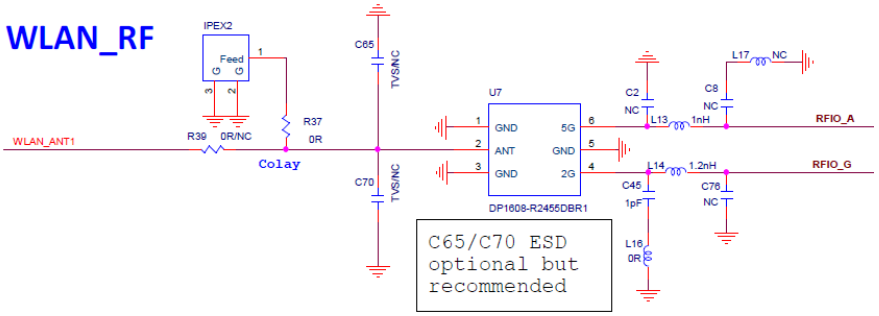
CHIP_EN is the enable pin of the whole chip, which can be used to reset the chip. CHIP_EN pin should be pull high with a 10K resistor by default.

If the chip needs to be reset through CHIP_EN pin, it is necessary to ensure that the CHIP_EN is pulled down by at least 0.1ms. For more specific sequences, please refer to the datasheet chapter4.4 Power Sequence.

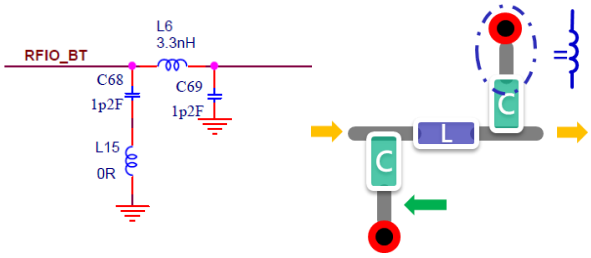


5 RF Circuits

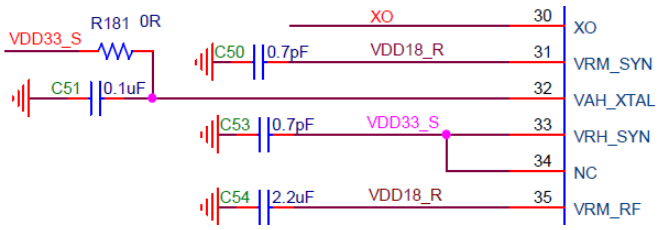
- RFIO need extra Pi matching to reduce TX 2nd&3rd harmonics before DPX for better EMI performance. Considering impedance matching, different DPX shall be matched with different Pi matching values.



- For WLAN and BT coexistence application，C8&L17 in RFIO_A、C45&L16 in RFIO_G、C68&L15 in RFIO_BT should be added to reduce interference. If pcb placement space is enough, L16 will be better to be placed between C76 and ground.
- There must be C-L-C pi-filter on BTG RF path for BT's TX harmonics suppression. The shunt capacitors shall be placed on the opposite sides of the RF path and there must be a short trace pulled from their GND pad to its grounding via. The distance of the two grounding via shall be ≧100mil for better harmonics suppression.



- TVS is used for protecting ESD, optional but recommended.
- Inside the chip, there is a balun. No DC block. Usually there is no need to add an external DC block for each RFIO pin. Because DC is 0. If you have external active component (SPDT or DPDT)and need to supply DC, a DC block is needed.
- For reduce VCO leakage radiation， the value of SYN bypass capacitors C50&C53 are recommended to 0.7pF .



- The recommended tolerance of the RF inductors is ±0.3nH or better, and tolerance of the RF capacitors is ±0.1pF or better.

6 I/O Characteristics

6.1 Features

The following electrical properties are configurable for standard I/O pins:

- Function ID
- Internal Pull-up/Pull-down Resistor
- Driving strength
- Schmitt trigger
- Shutdown & RESET
- Open drain mode

6.2 Functional Description

The I/O diagram is given in Figure 6-1. There are many kinds of I/Os in RTL8730E, different IOs have different configuration.

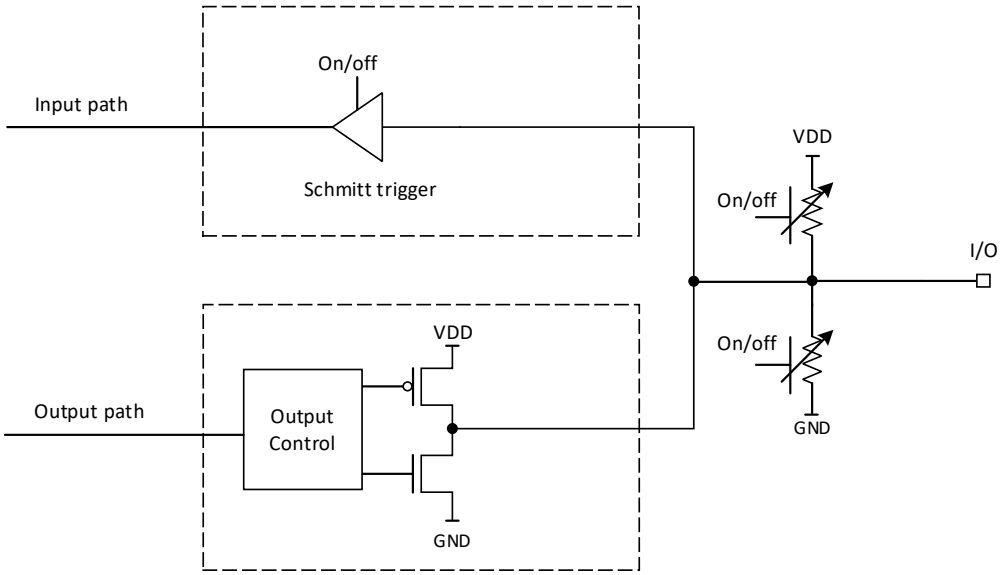


Figure 6-1 I/O diagram

6.2.1 I/O Types

All IOs are listed in Table 6-1. The HBM of all IOs are above 3.5KV.

Table 6-1 I/O types

Pin name	IO power pin	Driving(mA)[1]	Internal pull resistor (ohm)[2]	Internal pull resistor

		1.8V(±10%)	3.3V(±10%)	Min.	Typ.	Max.	**available in deep sleep mode[3]**
PA0~PA8[4]	VDH_IO0	-	4/8	40K	80K	120K	Yes
PA9~PA16[5]	VDH_IO1	4/8	8/16	2.3K/5K	4.7K/10K	7.1K/15K	Yes
PA17[5]	VDH_IO1	2/4	4/8	40K	80K	120K	Yes
PA18~PB6[6]	VAM_AUD	1/3	-	PU:185K PD:52K	PU:300K PD:100K	PU: 431K PD:165K	No
PB7~PB9[4]	VDH_IO2	-	4/8	40K	80K	120K	Yes
PB10~PB13[4]	VDH_IO2	-	8/16	2.3K/5K	4.7K/10K	7.1K/15K	Yes
PB14~PB20[5]	VDH_IO3	2/4	4/8	40K	80K	120K	Yes
PB21~PB22[4]	VDH_IO3/VDH_IO4[7]	-	8/16	2.3k/40K	4.7K/80K	7.1K/120K	Yes
PB23~PB24[4]	VDH_IO3/VDH_IO4[7]	-	8/16	40K	80K	120K	Yes
PB25~PC0[5]	VDH_IO6	2/4/8/10/12	4/8/46/20/24	12.5K/25K	25K/50K	37.5K/75K	Yes
PC1~PC7[4]	VDH_IO5	-	8/16	40K	80K	120K	Yes

NOTE

[1] The IO power supported by different IOs is different, and the driving capability is related to the IO power. Please refer to Table 6-3 for VOH&VOL.

[2] Except for PA18~PB6, the pull up and pull down values of other IOs in the table are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The range is ±50%.

[3] In deep sleep mode, since VAM_AUD is powered off, PA18~PB6 are in floating state and the internal resistors of these pins are unavailable. If circuit connected with these GPIOs needs to be pulled high or low state, external resistors on PCB are needed. In other mode except deep-sleep, internal resistors of all GPIOs are available.

[4] This Group only support 3.3V IO power.

[5] This Group support 1.8V/3.3V IO power.

[6] This Group support 1.8V IO power.

[7] The IO power pin of RTL8730ELH is VDH_IO4, and the IO power pin of RTL8730EAH is VDH_IO3.

6.2.2 IOCTRL Register

Each I/O pin has one IOCTRL register assigned to control the pin's electrical characteristics. IO Register base address 0x42008A00. For example, the register address of PA0 is 0x42008A00, the register address of PA1 is 0x42008A04. The bit[4:0] field in the IO register can be set to GPIO (typically value 00000) or a special function.

- For pins set to GPIO, the GPIO IP registers determine whether the pin is configured as input or output.
- For any special function, the pin direction is controlled automatically depending on the function.

For specific information about PINMUX function, please refer to the PINMUX documentation.

Table 6-2 IOCTRL Register Table

Offset	Bit	Access	INI	Symbol	Description
0000h	[17]	R/W	0h	gpio@_pd_slp	GPIO pull down enable when system is in sleep.
	[16]	R/W	0h	gpio@_pu_slp	GPIO pull up enable when system is in sleep.
	[15]	R/W	0h	gpio@_dis	GPIO shutdown, only when the gpio@_dis signals of this group of GPIOs are all 1, the group of GPIOs will be shutdown. 1. disable 0. enable
	[12]	R/W	1h	gpio@_smt	GPIO Schmitt control 1: enable Schmitt trigger 0: disable Schmitt trigger
	[11]	R/W	1h	gpio@_e2	GPIO driving Strength control.

					0: low 1: high
	[10]	R/W	0h	gpio@_pupdc	Some GPIO may have two type of PU/PD resistor, this bit can select it. 1: small resistor 0: big resistor
	[9]	R/W	0h	gpio@_pd	GPIO pull down enable when system is in active.
	[8]	R/W	0h	gpio@_pu	GPIO pull up enable when system is in active.
	[4:0]	R/W/ES	0h	gpio@_sel	GPIO PINMUX function id select

6.2.3 Function ID

Change the IO function ID through gpio@_sel in Table 6-2, please refer to the PINMUX documentation for details.

6.2.4 I/O Pull Resistor Control

The PU/PD of the IO in Active & Sleep mode is controlled by the PU&PD register. Allows selection of on-chip pull-up or pull-down resistors for each pin. For Specific information, please refer to the PU&PD register table.

Pull-up and Pull-down resistor's value is different between different IO. The resistor value is changed by controlling the gpio@_pupdc of register table (Table1-3). For IOs with only one resistance value, gpio@_pupdc is not valid.

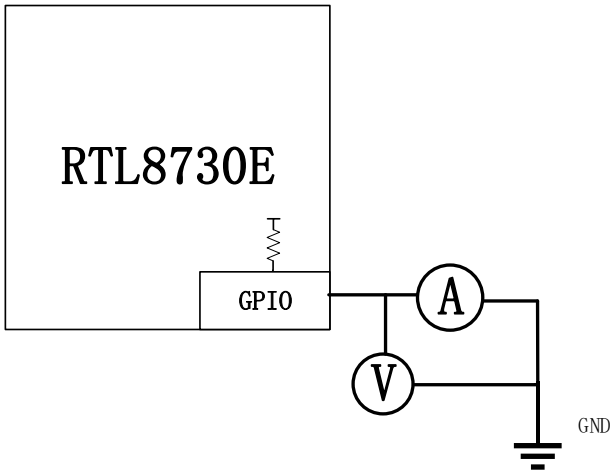


Figure 6-2 GPIO pull up resistor test

GPIO pull-up resistor test procedure:

(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 1 for gpio@_pu and 0 for gpio@_pd.
(3) For GPIOs with multiple pull-up resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is V_1.
(5) According to Figure 6-2, only connect the ammeter to test. At this time, the current value is I_1, and the pull-up resistor is $Rpu=V_1/I_1$.

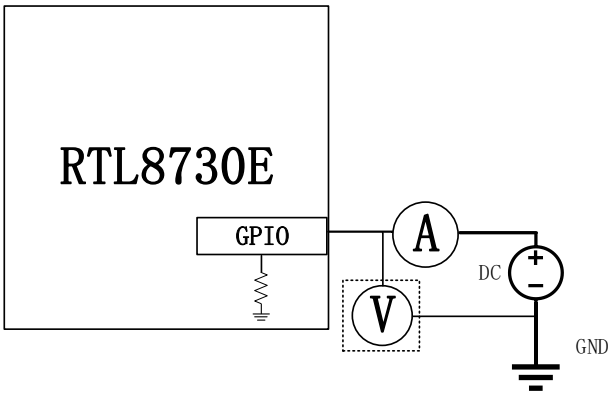


Figure 6-3 GPIO pull down resistor test

GPIO pull-down resistor test procedure:

(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 0 for gpio@_pu and 1 for gpio@_pd.
(3) For GPIOs with multiple pull-down resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is 0V.
(5) According to Figure 6-3, Use an external power supply to provide the same voltage (V_2) as the GPIO IO power, and measure the current (I_2) at this time, and the pull-up resistor is Rpd=V_2/I_2.

6.2.5 I/O Driving Strength

The I/O driving strength can be configured through gpio@_e2 in the IOCTRL register. IO driving strength is different between different IO types.

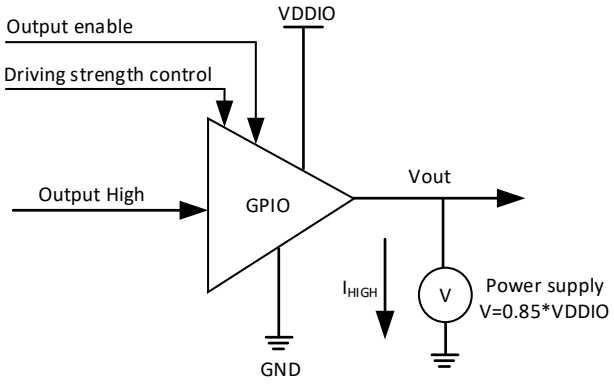


Figure 6-4 GPIO output high driving strength test

GPIO Output High Driving Strength test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.85*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2.
(4) I_{HIGH} is the driving Strength of GPIO output high.

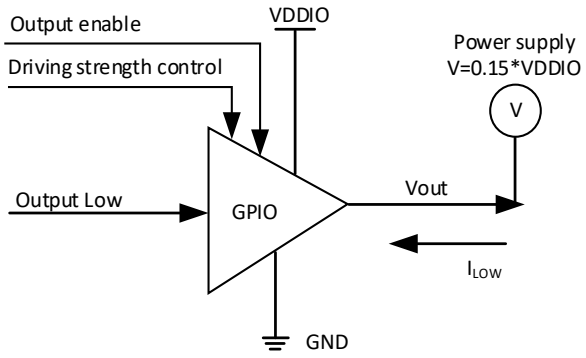


Figure 6-5 GPIO output low driving strength test

GPIO Output Low Driving Strength test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.15*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2.
(4) I_{LOW} is the driving Strength of GPIO output Low.

6.2.6 I/O Schmitt Trigger

The I/O pin contains a Schmitt trigger as a digital function, which can be selectively disabled by setting gpio@_smt in the IOCTRL register. Schmitt trigger is effective when GPIO is used as input function. The function of Schmitt trigger is to eliminate noise and jitter in the input signal and provide a stable output signal.

Figure 6-6 shows the pin voltage status seen by GPIO when Schmitt trigger is enable or disable when GPIO is in its input function. If the Schmitt trigger is disabled in IOCTRL register, VIH=VIL=0.5*VIO.

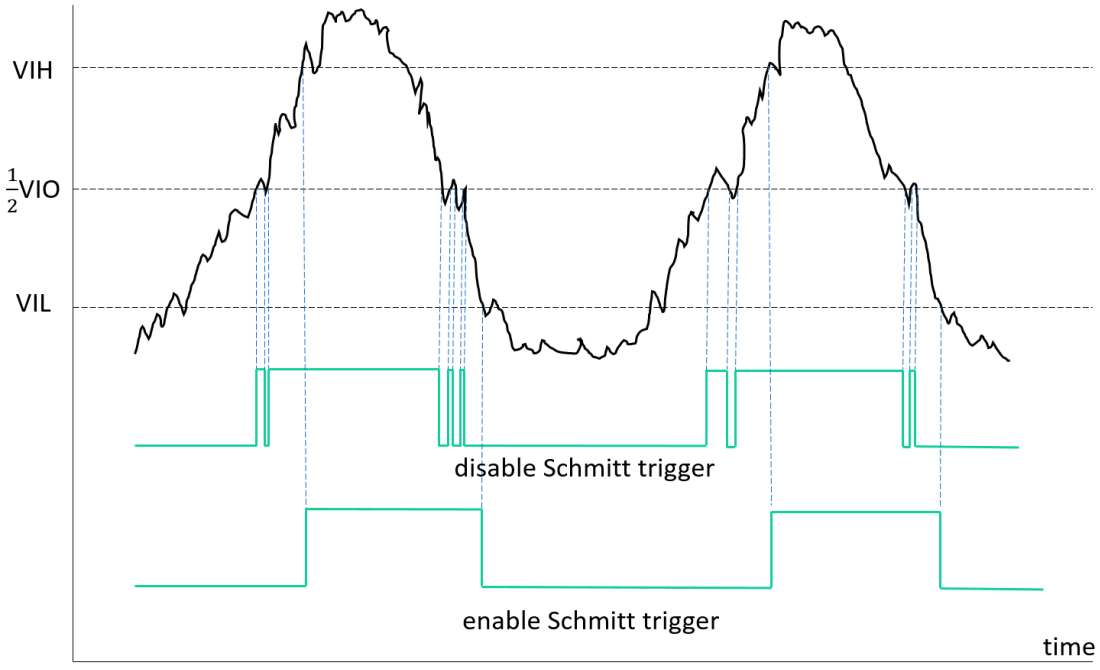


Figure 6-6 The voltage seen by GPIO when Schmitt trigger is enabled or disabled

The specifications of digital IO pin DC characteristics are shown in Table 6-3.

Table 6-3 Digital IO pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIL	IO input low level voltage	VIO=1.8V±10%	-0.3	-	0.35*VIO	V

		VIO =3.3V±10%	-0.3	-	0.8	
VIH	IO input high level voltage	VIO=1.8V±10%	0.65* VIO	-	-	
		VIO=3.3V±10%	2	-	-	
VOL	IO output Low level voltage	VIO=1.8V±10%,IOL Max	-	-	0.15*VIO	
		VIO=3.3V±10%,IOL Max	-	-	0.15*VIO	
VOH	IO output high level voltage	VIO=1.8V±10%,IOH Max	0.85*VIO	-	-	
		VIO=3.3V±10%,IOH Max	0.85*VIO	-	-	

NOTE

- *VIO is the power supply for IO pin.*
- *Refer to Table 6-1 for IO driving strength.*

6.2.7 I/O Shutdown & RESET

The power of I/O can be shut down through the GPIO_BIT_SHUT_DOWN bit in the IOCTRL register. You can use this function to conserve power.

For I/O shutdown, only when the whole group I/O shut down signals are all 1, the I/O SHDN will pull down to shut down the group I/O. Customer can also directly control the Group shutdown register and directly control the I/O shutdown of this group. For Specific information, please refer to the I/O SHDN&RSTB register table.

- When RSTB is set to 0, the I/O is in tri state. At this time, the level of the I/O is determined by the external pull-up and pull-down. If the external pull-down is connected, the I/O level is low. If the external pull-up is connected, the I/O level is high.
- When SHDN=1 and RSTB=1, the PU/PD state of the I/O is determined by register configuration.
- When RSTB=1, SHDN changes from 1 to 0, the state of I/O will latch the current state. At this time, the change of the I/O pull-up/pull-down register will not change the state of the I/O pull resistor.

Table 6-4 I/O SHDN&RSTB register

Address	Bit	Access	INI	Symbol	Description
0x42008000	[29]	R/W	0	LPGPIO_RSTB	1: Release LP GPIO RSTB33 (except GPIOF) 0: Global Assert LP GPIO RSTB33
	[28]	R/W	0	LPGPIO_SHDN	1: Global Enable LP GPIO (except GPIOF) 0: Shutdown LP GPIO Note: Default value must be fixed after AON PMC done.
	[23]	R/W	1	GROUP_A_RSTB	1: Enable group A GPIO 0: Reset GPIO
	[22]	R/W	1	GROUP_B_RSTB	1: Enable group B GPIO 0: Reset GPIO
	[21]	R/W	1	GROUP_C_RSTB	1: Enable group C GPIO 0: Reset GPIO This is for audio GPIO, may not use
	[20]	R/W	1	GROUP_D_RSTB	1: Enable group D GPIO 0: Reset GPIO
	[19]	R/W	1	GROUP_E_RSTB	1: Enable group E GPIO 0: Reset GPIO
	[18]	R/W	0	GROUP_F_RSTB	1: Enable group F GPIO 0: Reset GPIO
	[17]	R/W	1	GROUP_G_RSTB	1: Enable group G GPIO 0: Reset GPIO

	[16]	R/W	1	GROUP_H_RSTB	1: Enable group H GPIO 0: Reset GPIO
	[15]	R/W	1	GROUP_A_SHDN	1: Enable group A GPIO 0: Shutdown GPIO
	[14]	R/W	1	GROUP_B_SHDN	1: Enable group B GPIO 0: Shutdown GPIO
	[13]	R/W	1	GROUP_C_SHDN	1: Enable group C GPIO 0: Shutdown GPIO This is for audio GPIO, may not use
	[12]	R/W	1	GROUP_D_SHDN	1: Enable group D GPIO 0: Shutdown GPIO
	[11]	R/W	1	GROUP_E_SHDN	1: Enable group E GPIO 0: Shutdown GPIO
	[10]	R/W	0	GROUP_F_SHDN	1: Enable group F GPIO 0: Shutdown GPIO
	[9]	R/W	1	GROUP_G_SHDN	1: Enable group G GPIO 0: Shutdown GPIO
	[8]	R/W	1	GROUP_H_SHDN	1: Enable group H GPIO 0: Shutdown GPIO

NOTE

- *GROUP_A: PA0~PA8*
- *GROUP_B: PA9~PA17*
- *GROUP_C: PA18~PA31 & PB0~PB6*
- *GROUP_D: PB7~PB13*
- *GROUP_E: PB14~PB20*
- *GROUP_F: PB21~PB24*
- *GROUP_G: PB25~PB31 & PC0*
- *GROUP_H: PC1~PC6*

6.2.8 Open Drain Mode

The I/O is default to push pull mode, and can be configured to implement open drain mode. For more details, refer to the software APIs.

6.3 I/O Internal Pull Control Configuration

Each I/O has an Internal Pull-up and Pull-down Resistor. Please refer to section 6.2 for details. This section describes how to configure it. During the process of boot, sleep and deep-sleep, I/O pull control is needed, and the chip will load the I/O internal pull status of each I/O from the “pinmapcfg.c” file.

The correct configuration of pinmap can achieve low power consumption. Otherwise, the unsuitable configuration may lead to leakage.

Principles for I/O internal control configuration:

(1) If the I/O is not used, it is recommended to set it to pull down.
(2) If I/O is used as input, it cannot be left floating. please refer to the following chapters for configuration of different functions.
(3) If I/O is used as output, please refer to the following chapters for configuration of different functions.

In the SDK, customers should set the internal pull status of I/O according to the above rules.

In the “pinmapcfg.c” file, PMAP_TypeDef pmap_func[] should be configured. In which,

- Pin Name: indicates the I/O.
- Func PU/PD: is used to configure the I/O internal pull status when the IC is in active mode.
- Slp PU/PD: is used to configure the I/O internal pull status when the IC is in sleep mode.

The following configuration is only applicable to RTK EVB, and customers need to configure it according to the external circuit.

```
const PMAP_TypeDef pmap_func[]=
```

```
{
//Pin Name      Func PU/PD          Slp PU/PD
{_PA_0,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_1,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_2,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_3,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_4,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_5,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_6,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_7,         GPIO_PuPd_KEEP,     GPIO_PuPd_DOWN},
{_PA_8,         GPIO_PuPd_KEEP,     GPIO_PuPd_DOWN},
{_PA_9,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_10,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_11,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_12,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_13,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_14,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_15,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_16,        GPIO_PuPd_UP,       GPIO_PuPd_UP},
{_PA_17,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_18,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_19,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_20,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_21,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_22,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_23,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_24,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_25,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_26,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_27,        GPIO_PuPd_KEEP,     GPIO_PuPd_DOWN},
{_PA_28,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_29,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_30,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PA_31,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_0,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_1,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_2,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_3,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_4,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_5,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_6,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_7,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_8,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_9,         GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_10,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_11,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_12,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_13,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_14,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
{_PB_15,        GPIO_PuPd_UP,       GPIO_PuPd_DOWN},
```

```
{_PB_16,      GPIO_PuPd_UP,      GPIO_PuPd_DOWN},
{_PB_17,      GPIO_PuPd_UP,      GPIO_PuPd_DOWN},
{_PB_18,      GPIO_PuPd_DOWN,    GPIO_PuPd_DOWN},
{_PB_19,      GPIO_PuPd_DOWN,    GPIO_PuPd_DOWN},
{_PB_20,      GPIO_PuPd_DOWN,    GPIO_PuPd_DOWN},
{_PB_21,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_22,      GPIO_PuPd_DOWN,    GPIO_PuPd_DOWN},
{_PB_23,      GPIO_PuPd_DOWN,    GPIO_PuPd_DOWN},
{_PB_24,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_25,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_26,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_27,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_28,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_29,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_30,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PB_31,      GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_0,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_1,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_2,       GPIO_PuPd_UP,      GPIO_PuPd_DOWN},
{_PC_3,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_4,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_5,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PC_6,       GPIO_PuPd_UP,      GPIO_PuPd_UP},
{_PNC,        GPIO_PuPd_KEEP,    GPIO_PuPd_KEEP},
```

There are four states of the I/O.

- GPIO_PuPd_UP: Indicates that the I/O is through the internal resistor pulled up to VDDIO.
- GPIO_PuPd_DOWN: Indicates that the I/O is through the internal resistor pulled down to GND.
- GPIO_PuPd_NOPULL: Indicates that the I/O does not have an internal pull-up or pull-down configured.
- GPIO_PuPd_KEEP: Indicates that the I/O will maintain the last status.

The following section illustrates the recommendation of I/O status configurations according to the function of different pins.

6.3.1 Normal GPIO

When a pin is used as a normal GPIO connecting with external circuit, the GPIO PU/PD status depends on the state of the external circuit. If the GPIO is used to driver LED, and pin status is ‘External pull up’, the GPIO status need to be ‘PULL UP’ in sleep and DSLP mode. Configure the state of the internal PU/PD according to the GPIO external circuit.

Table 6-5 Normal GPIO status

I/O Type	Pin Status	active PU/PD	Sleep PU/PD
Input	External Pull UP	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP / GPIO_PuPd_NOPULL
Input	External Pull Down	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL
Input	Floating	GPIO_PuPd_DOWN	GPIO_PuPd_DOWN
Output	Output High	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP
Output	Output Low	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN

6.3.2 LOGUART Pin

The pins PB23 and PB24 are LOGUART function by default. The status is listed in Table 6-6.

Table 6-6 LOGUART IO status

Pin Function	Pin Name	Func PU/PD	Slp PU/PD

UART_LOG_RXD	PB23	GPIO_PuPd_UP	GPIO_PuPd_KEEP
UART_LOG_TXD	PB24	GPIO_PuPd_UP	GPIO_PuPd_KEEP

6.3.3 ADC & Cap-touch Pin

For PA0~PA8, if customer need to configure it for ADC or cap-touch function, customers need to configure IE to 0 first, and configured as internal no pull.

Table 6-7 GPIO IE Register Table

address	Bit	Access	INI	Symbol	Description
0x420082F8	[8:0]	R/W	1FFh	ADC/ Cap-Touch GPIO input enable	PA0~PA8 IE signals

If the customer needs to configure other functions, IE needs to be set to 1. For other configurations, please refer to section 6.3.1.

6.3.4 SWD Pin

When a pin is configured as SWD function, the IO status is listed in Table 6-8.

Table 6-8 SWD IO status

Pin Function	Func PU/PD	Slp PU/PD
SWD_DATA	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SWD_CLK	GPIO_PuPd_UP	GPIO_PuPd_KEEP

If the SWD pin (PA13&PA14) needs to be used as a non-SWD function, in addition to switching the function id of the GPIO, the SWD function needs to be disabled.

Table 6-9 SWD pin function

address	Bit	Access	INI	Symbol	Description
0x42008BF8	[0]	R/W	1h	SWD_PMUX_EN	1: Enable SWD pin (PA13&PA14) mux enable function 0: Disable

6.3.5 Flash Pin

When a pin is configured as SPI_FLASH function, the IO status are listed in Table 6-10.

Table 6-10 Flash pin IO status

Pin Function	Func PU/PD	Slp PU/PD
SPI_DATA_X	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CS	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CLK	GPIO_PuPd_DOWN	GPIO_PuPd_KEEP

6.3.6 Audio Pin

(1) The PA18~PB6 is used as the audio function by default.
(2) If configured as audio function, the internal pull-up or pull-down function is invalid.
(3) In deep-sleep mode, since VAM_AUD is powered off, PA18~PB6 are in floating state and the internal resistors of these pins are unavailable.

If the audio pin needs to be used as a non-audio functions, customers need to configure the audio pin IE to 1 first.

Table 6-11 Audio pin IE Register Table

address	Bit	Access	INI	Symbol	Description

0x42008B20	[20:0]	R/W	0h	Audio pin input enable	Audio share GPIO (PA18-PB6) input enable.

If audio pin needs to be used as a non-audio functions, audio operations need to be muted. The IO power of the audio pin is 1.8V. Refer to Table 6-12 for the process of audio pin mute, which is implemented by software API. Please refer to Chapter 8 for details.

Table 6-12 Mute configuration

Step	Mute control	Register configuration
1	Enable Function	Sets Register 0x4200820C bit[25]=1'b1,bit[26]=1'b1
2	Enable clock	Sets Register 0x42008218 bit[24]=1'b1
3	Clock selection	Sets Register 0x42008224 bit[13] =1
4	Mute MIC	Sets Register 0x4100C110 bit[16:19]=4'b1111, 4100C114 bit[0:3] = 4'b1111, 4100C114 bit[11:10] = 2'b11

6.4 I/O Pins Output Description

If customers need to use I/O to drive other devices, such as LEDs, they should first set the I/O to output 1 or 0, and then set the I/O to output mode. Because if you set the I/O to output mode without first setting output 1 or 0, the I/O will output 0 first, which may cause the LED light to flash due to the incorrect status of the I/O output.

After the system enters sleep mode (PG or CG), the status of the I/O output will maintain the status before sleep. For example, before sleep, the I/O is set to output 1. After the system enters PG or CG, this I/O will still remain output 1 unchanged.

However, if the system enters deep sleep, the status of the I/O output set under active will become invalid. For example, if the I/O in active is set to output 1, and the system enters deep sleep, the I/O will not be able to maintain the output 1 state.

7 PINMUX

7.1 Introduction

RTL8730E provides a PINMUX circuit to maximize the user's freedom of use under limited pin-out conditions. Each pin can be connected to different internal IP circuits through configuration. For the specific correspondence between each pin and IP circuit, refer to the provided PINMUX document.

Before you use the chip for further development, please read the following precautions about PINMUX to avoid inconvenience to your use due to unexpected behaviors.

7.2 Trap pin

During power on, the chip will latch several pins conditions to decide whether enter into different mode. The trap pins and their descriptions are as below.

Table 7-1 Descriptions of trap pins

IO name	Trap pin name	Active level	Descriptions	Note
PB22/TM_DIS	test_mode_b	Low	Enter RTK test mode	
PB24/UD_DIS	uart_download_b	Low	Enter flash download mode	Download flash content in this mode through LOGUART.
PB21[1]	Boot_sel	-	Select boot from NAND or NOR flash	Boot_sel = 1, boot from NOR flash Boot_sel = 0, boot from NAND flash

NOTE

[1].PB21 used as Boot_sel function is only valid for RTL8730ELM-VA7&VA8

The trap pins need to select the external pull-up and pull-down voltages according to the IO power supply.

7.3 Wake pin

PB21, PB22, PB23, PB24 are directly connected to the wake up circuit which is used to wake up system from deep-sleep state. When you need to use other functions on this pin, please disable the wake up function（FUNC_ID 30）.

7.4 Function mux

For functions whose ID number among 0-29, each pin can only be connected to a fixed signal of a certain IP. The functions that can be configured on each pin are very limited, but a dedicated design can maximize the performance of each IP.

Take PA0 as an example. If you configure function ID of PA0 to 1, then the pin will be directly connected to the UART2_RXD signal of the UART2 IP via PINMUX.

Also if you configure function ID of PA0 to 18, then the pin will be directly connected to the ADC0 signal of the AUX ADC IP via PINMUX.

Please refer to the PINMUX document for the specific function distribution available on each pin.

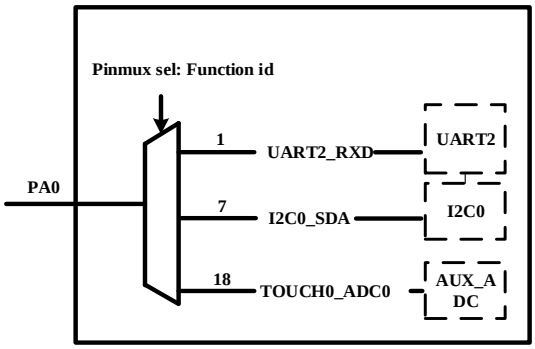


Figure 7-1 Schematic diagram of PINMUX connection of PA0

7.5 Usage limitation

7.5.1 BT interfere PA4/5/15/16

During normal use of BT, unexpected interference may be seen on PA4, PA5, PA15 and PA16, which may affect the normal communication of these IOs. This interference is more obvious when these IOs are in a weak driving state.

If RTL8730E BT function is enable, it is suggested:

- Avoid using PA4, PA5, PA15 and PA16
- If PA4, PA5, PA15 and PA16 are used, try to avoid configuring these IOs pinmux function in weak driving state, such as IO input, ADC input, I2C function, etc. It’s ok to configure these IOs in output pinmux functions.

8 Audio

8.1 Audio Hardware Application

Audio codec supports three input ways: line-in, AMIC-in and DMIC-in; and one output way which can be configured as line-out and headphone out. Microphone array smart voice application is also introduced.

8.1.1 Line-out

Line-out supports two output modes: differential and single-ended. Users can select the wanted mode by setting the related registers.

8.1.1.1 Line-out Differential Mode

In this mode, both N-end and P-end drive the available analog audio signal. This application is mainly used to provide clean audio for external power amplifiers (Class-AB/Class-D).

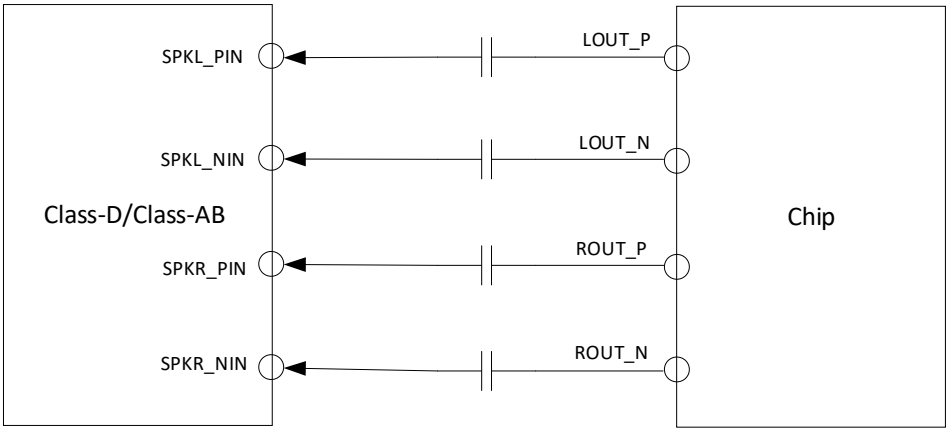


Figure 8-1 Differential mode connection with audio power amplifiers

8.1.1.2 Headphone-out Single-ended Mode

In this mode, the circuit designer needs to place a capacitor to the P-end output path for analog audio signal pick-up. No N-end output is required.

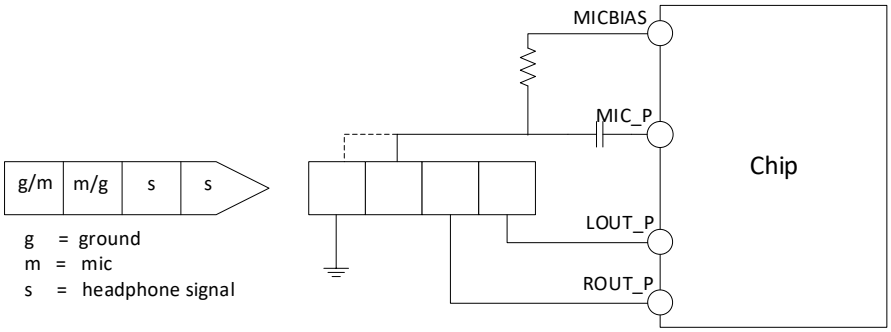


Figure 8-2 Single-ended mode connection with headphone jack

8.1.2 Line-in

Line-in has 0dB gain preamplifier, its input signal often has a large output power. It often connects to the audio output of equipment such as

electric guitar, electronic organ, and synthesizer.

Connect the left channel of line-in signal to MICIN_L, and the right channel to MICIN_R accordingly.

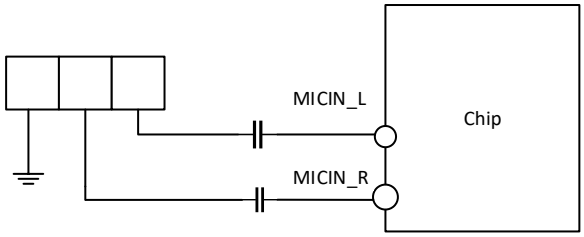


Figure 8-3 Line-in mode connection

8.1.3 AMIC-in

The amplitude of the signal collected by analog microphone (AMIC-in) is very small, a preamplifier is necessary, AMIC-in supports differential mode and single-ended mode.

8.1.3.1.1 AMIC-in Single-ended Mode

Connect MIC_P with a single-ended analog microphone, while MICBIAS provides the microphone bias voltage.

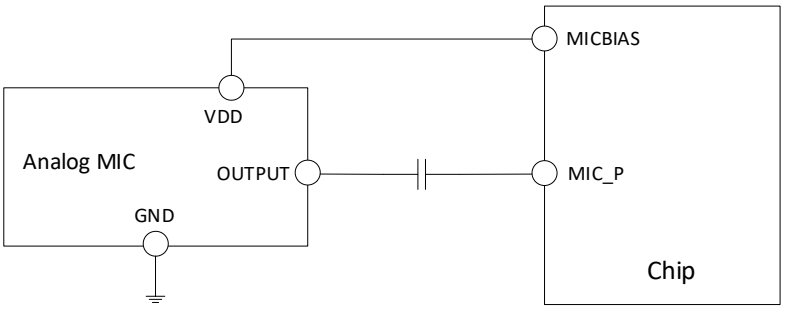


Figure 8-4 AMIC-in single-ended mode connection

8.1.3.2 AMIC-in Differential Mode

Connect MIC_P/MIC_N with a differential analog microphone, while MICBIAS provides the microphone bias voltage.

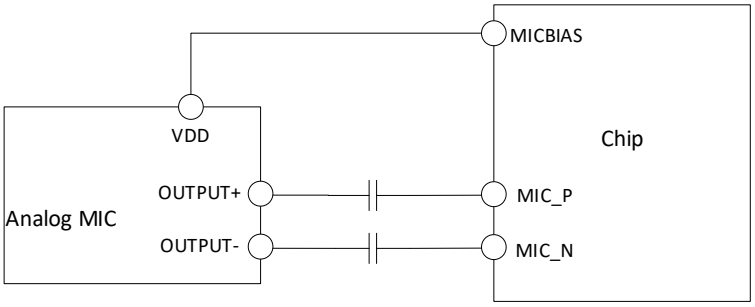


Figure 8-5 AMIC-in differential mode connection

8.1.4 DMIC-in

Digital microphone (DMIC) records audio data. It is integrated with ADC internal, and can directly output digital signal. DMIC-in supports mono mode and stereo mode.

8.1.4.1 DMIC-in Mono Mode

Tie the L/R of a digital microphone to ground or VDD if only one digital microphone is placed.

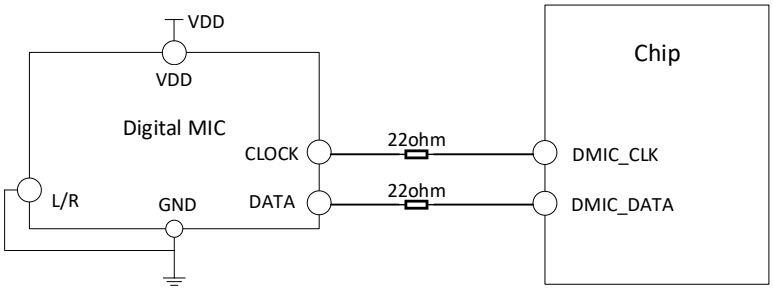


Figure 8-6 DMIC-in mono mode connection

For layout design，DMIC_CLK and DMIC_DATA should add ground isolation on both sides of the routing.

Figure 8-7 DMIC-in layout

8.1.4.2 DMIC-in Stereo Mode

Tie the L/R of two digital microphones to ground and VDD respectively if a stereo microphone is needed. The two microphones share the DMIC_DATA according to the rising/falling edge.

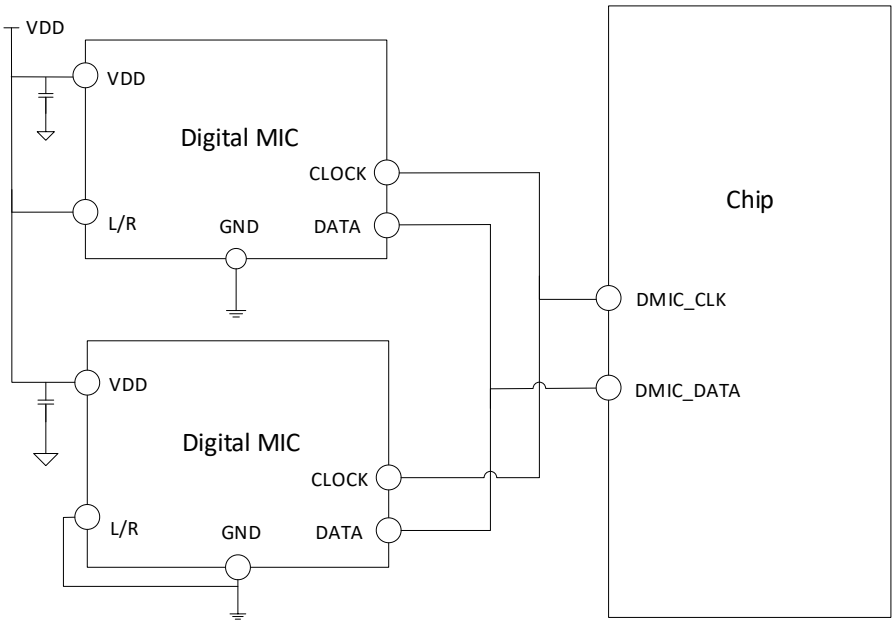


Figure 8-8 DMIC-in stereo mode connection

8.1.5 Microphone Array

8.1.5.1 Two-microphone Smart Voice Application

In this application, two ADCs are used to collect the speaker's voice, and one ADC is used to collect the reference sound of echo cancellation.

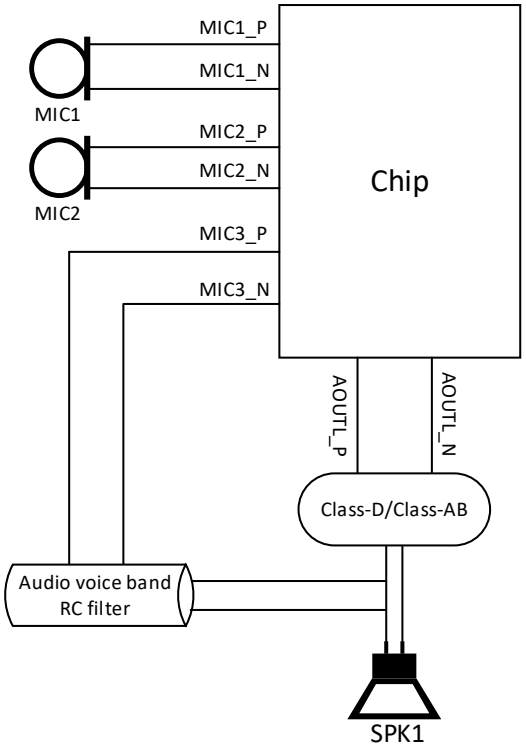


Figure 8-9 Two-microphone smart voice application

8.1.5.2 Four-microphone Smart Voice Application

In this application, four ADCs are used to collect the speaker's voice, and one ADC is used to collect the reference sound of echo cancellation.

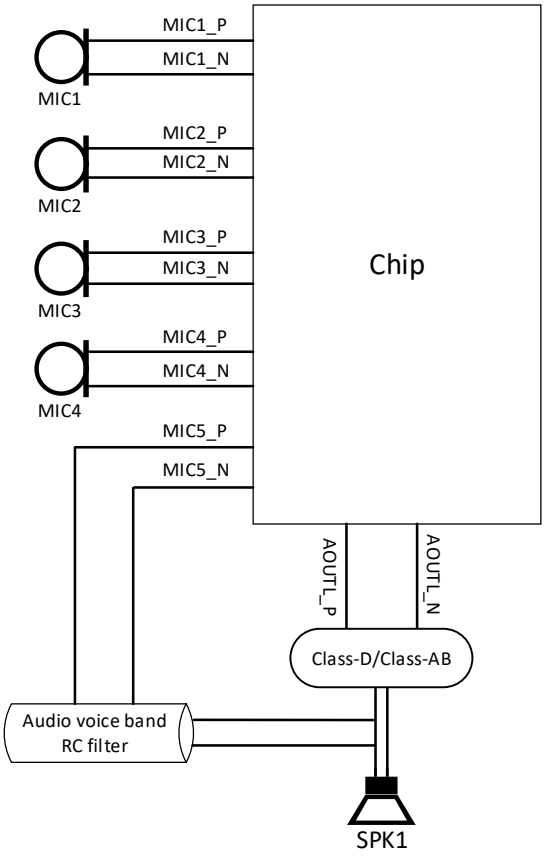


Figure 8-10 Four-microphone smart voice application

8.1.6 I2S Data Pin

The data paths of SPORT 2/3 are shown in Figure 8-11 to Figure 8-12 respectively.

- For I2S TDM mode: Only SD_O_0 and SD_I_0 can be used.
- For I2S Multi-IO mode: SD_O_0/1/2/3 and SD_I_0/1/2/3 all can be used. By default, use SD_O_0/1/2/3 and SD_I_0/1/2/3 in order according to the number of channels.

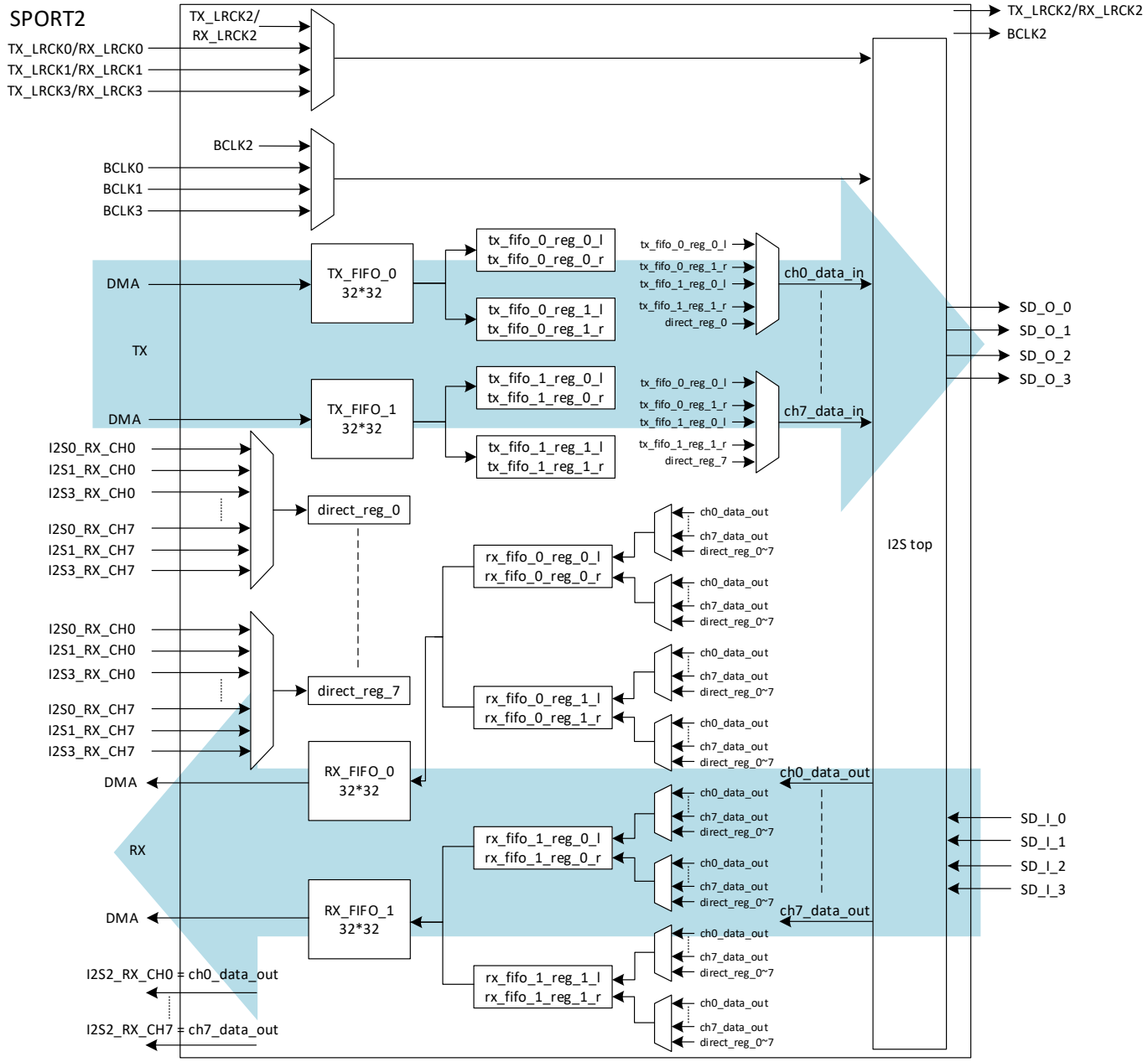


Figure 8-11 SPORT2 data path

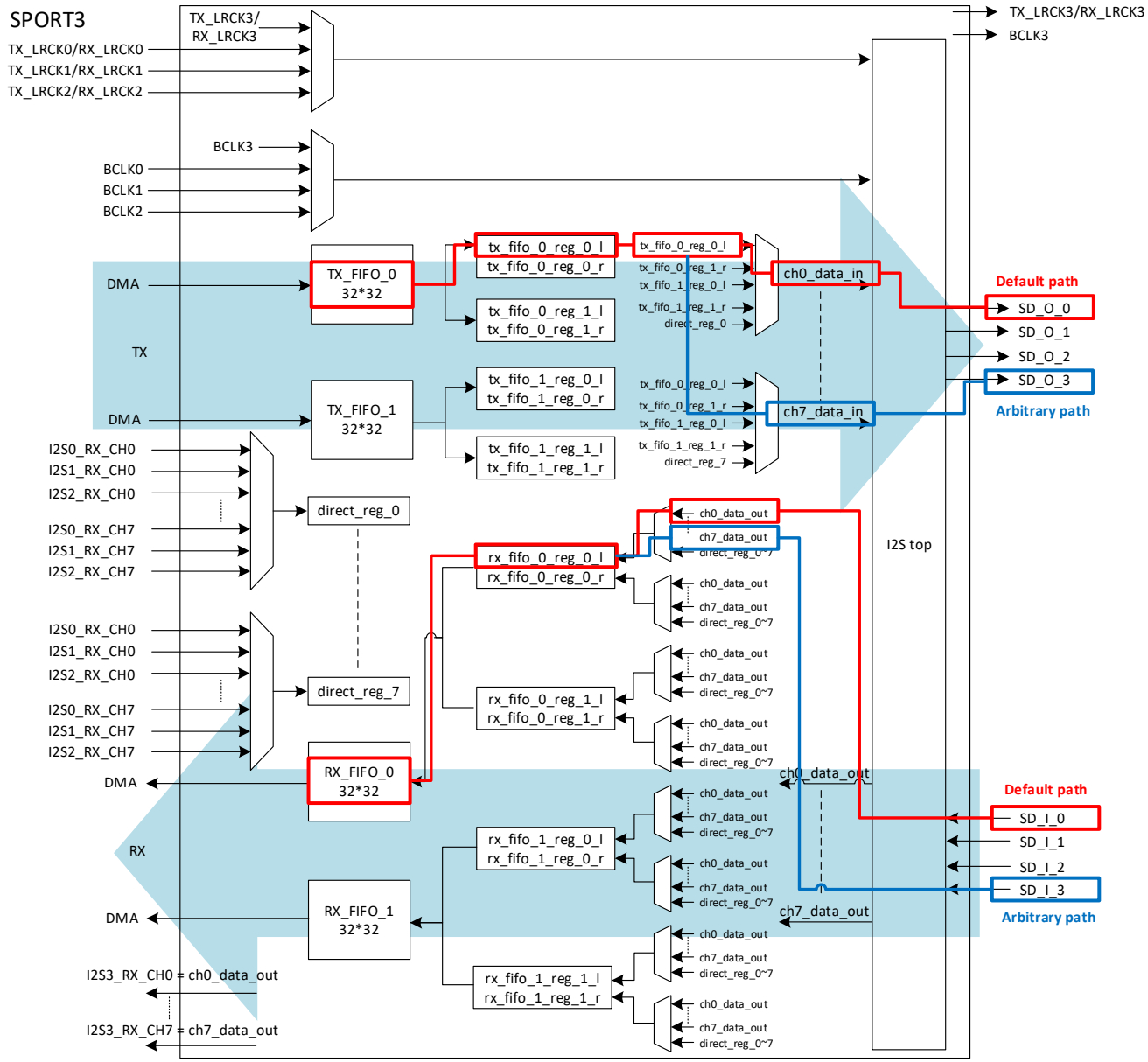


Figure 8-12 SPORT3 data path

As shown in Figure 8-12, the default path is red line and the arbitrary path is blue line. For arbitrary path, default order can be changed by the following interfaces:

- SD_O: AUDIO_SP_TXCHNSrcSel(u32 index, u32 fifo_num, u32 NewState)
- SD_I: AUDIO_SP_RXFIFOSrcSel(u32 index, u32 fifo_num, u32 NewState)

8.1.7 Audio Pad

Audio pad can be used as digital path or analog path, and Audio pad share status can be changed by the interface:

```
APAD_InputCtrl(u8 PinName, u32 NewState)
```

- ENABLE: enable digital path
- DISABLE: disable digital path

8.1.7.1 AOUT Pad

If AOUT pad (PB3~PB6) are used as digital I/O functions, HPO should be powered down.

When audio playback is running , HPO will be powered on. Users can call the following interface to power down HPO.

```
AUDIO_CODEC_SetHPOPowerMode(u32 channel, u32 powermode)
```

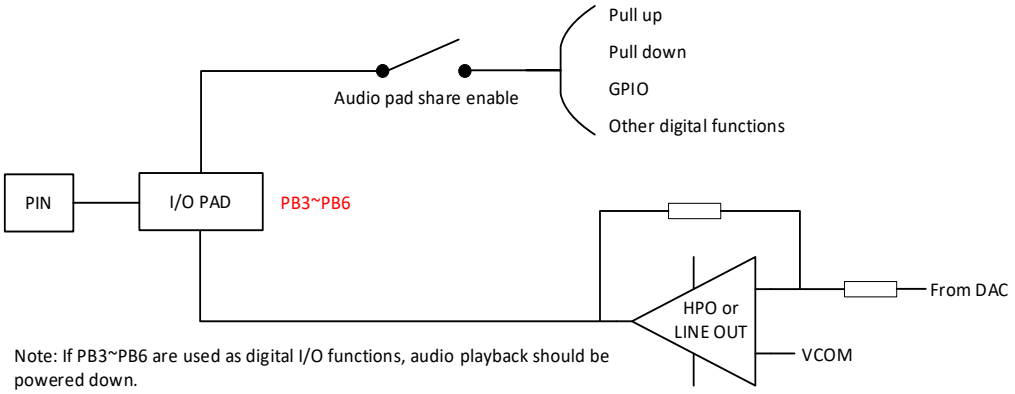


Figure 8-13 AOUT pad

8.1.7.2 MICBIAS Pad

If MICBIAS pad (PA30~PA31 and PB0~PB2) are used as digital I/O functions, MICBIAS should be powered down.

When audio record is running , MICBIAS will be powered on. Users can call the following interfaces to power down MICBIAS.

```
AUDIO_CODEC_SetMicBiasPowerMode(u32 powermode)
AUDIO_CODEC_SetMicBiasPCUTMode(u32 amic_num, u32 pcut_mode)
```

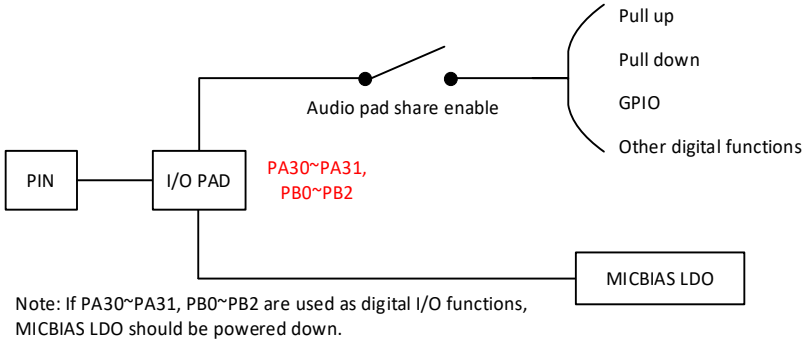


Figure 8-14 MICBIAS pad

8.1.7.3 MIC Pad

If MIC pad (PA18~PA29) are used as digital I/O functions, MICBST should be mute.

When audio record is running , MICBST will be unmute. Users can call the following interface to mute MICBST.

```
AUDIO_CODEC_SetMicBstChnMute(u32 amic_sel, u32 type, u32 newstate)
```

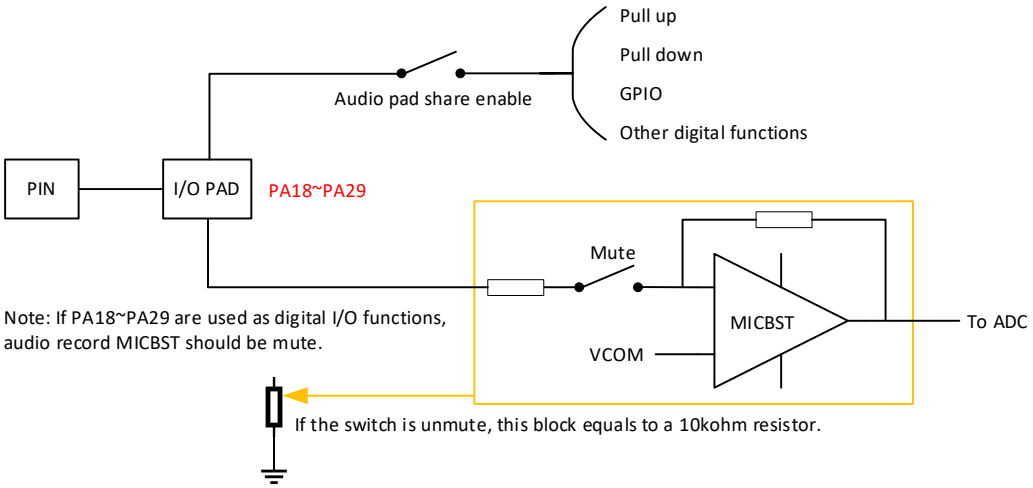


Figure 8-15 MIC pad

8.2 Hardware Design Guide

8.2.1 Headphone-out

The headphone-out connection of audio codec is illustrated in Figure 8-16. The capacitors between 3.5mm jack and IC should be 47uF tantalum capacitors rather than ceramic capacitors. The reason is that the capacitance value of ceramic capacitors may decrease when bias voltage is applied to them, which causes audio performance bad.

The value of the 47uF capacitor can be modified. The 47uF capacitor and the external headphone impedance (16ohm or 32ohm) form a high-pass filter with a cutoff frequency of f=1/2πRC, R=16 or 32. The value of C can be modified according to the requirements for low-frequency response.

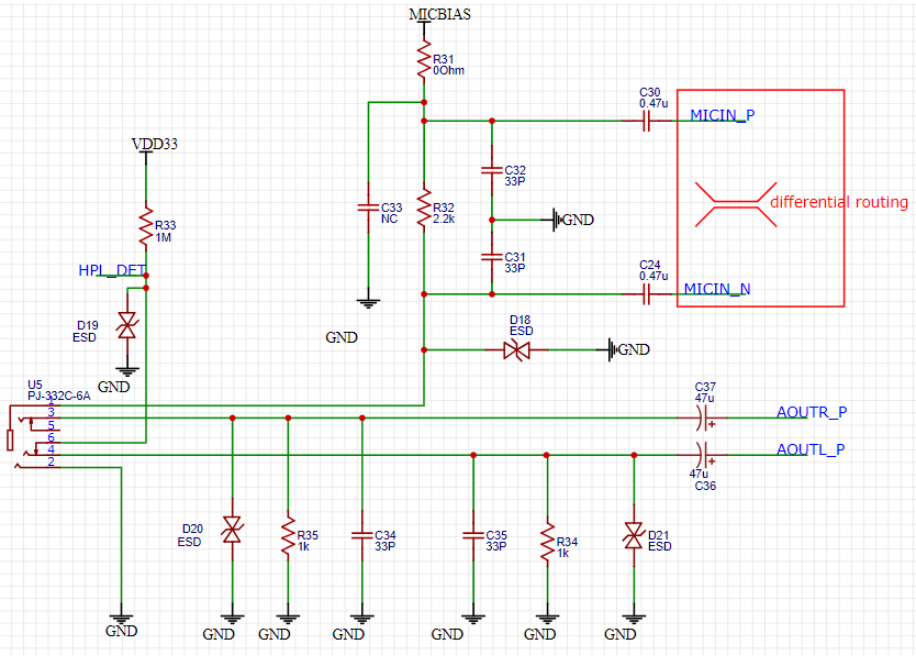


Figure 8-16 Line-out connection

HPL_DET is used to monitor the insertion of headphones, HPL_DET is high when headphones are plugged in, and low when no headphones are plugged in.

8.2.2 ECM AMIC-in

The ECM (electret microphone) AMIC-in connection of audio codec is illustrated in Figure 8-17. The capacitor between analog microphone and IC should be 0.47uF. A larger capacitance value makes a longer period needed for capacitor charging.

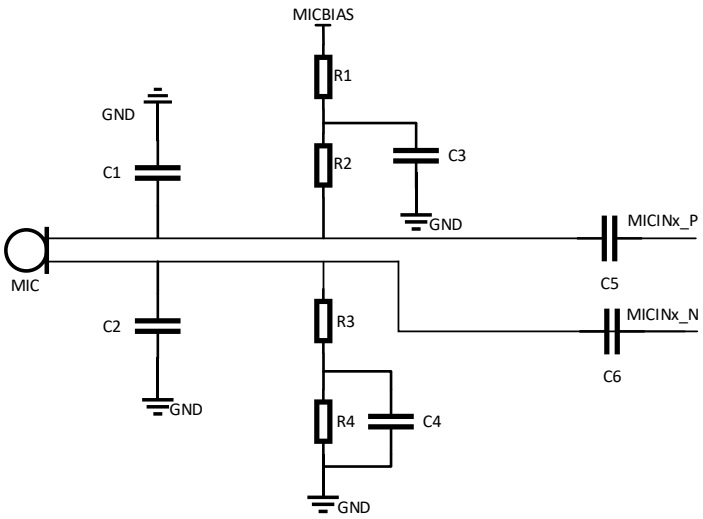


Figure 8-17 AMIC-in connection

MICBIAS connects to the positive side of microphone through R1/R2/R3/R4 resistors to offer bias voltage.

- Connect the negative side of microphone to MICN through a 0.47uF capacitor at differential mode.
- The value of the capacitor C5/C6 can be selected larger, in order to obtain a lower frequency audio signal. Fc=1/2*pi*5K*C5
- R4/C4 and R1/C3 are two low pass filter and are used to suppress noise on the power supply and ground. The values of these components need to be determined after actually testing the circuit board

8.2.3 AEC reference circuit

The following reference circuit is used in the intelligent voice application circuit. SPK_P/N is the output circuit of the power amplifier, and MICINx_P/N is the microphone amplifier input.

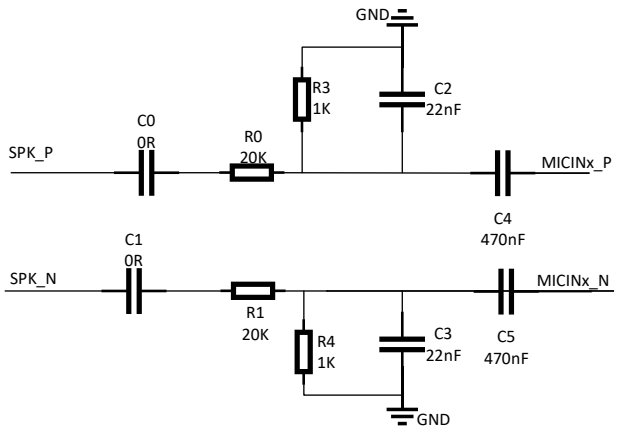


Figure 8-18 AEC reference circuit

- Vaec is AEC reference circuit output,Vspk is AEC reference circuit input，Vaec=Vspk*R3/(R0+R3)
- R0/R3/C2 are low pass filter,-3dB Cut-off Frequency:f=1/2π（R0//R3）C2
- C0/C1 select 0.1uF for low power application

- The capacitance value of C4/C5 can be modified. This capacitance forms a high-pass filter with the 10Kohm input impedance of the MICIN amplifier. The cut-off frequency Fc=1/2*pi*10K*C
- R0/R3 is a voltage divider circuit. Its value can be adjusted according to the maximum output amplitude of the power amplifier and the maximum allowable input amplitude of MICIN (1.5vpp). The corresponding C2 should also be adjusted based on the cut-off frequency in f=1/2π（R0//R3）C2. The adjustment method of R1/R4/C3 is the same

8.2.4 Power

The power connection of audio codec is illustrated in Figure 8-19:

- The capacitor between VREF_AUDIO and ground should be 1uF.
- The capacitor between AVCC or AVCC_DRIV and ground should be 1uF or a little larger to keep voltage stable.

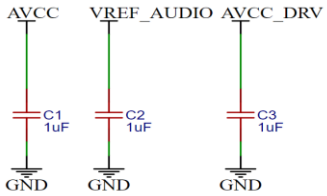


Figure 8-19 Power connection

8.2.5 I2S layout

Reserve 22ohm resistors on the CLK and DATA paths of I2S. If the layout space allows, increase ground isolation for CLK and DATA as much as possible.

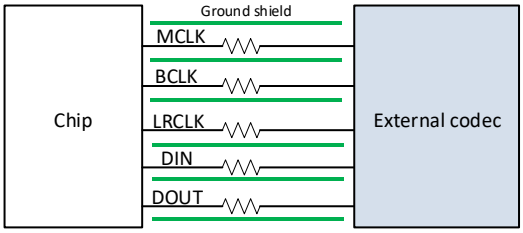


Figure 8-20 I2S layout

8.2.6 Intelligent voice application suggestions

8.2.6.1 Microphone unit performance requirements

- MIC recommends that silicon microphones are preferred for better consistency.
- MIC recommends the following parameters:
  - Sensitivity: analog silicon microphone -38dBV ~ -42dBV/±1.5dBV;
  - Signal-to-noise ratio (SNR): ≥60dB
  - Total harmonic distortion (THD): ≤ 1% (1kHz)
  - Acoustic overload point (AOP): ≥120dB SPL
  - Free field spectrum (within 100-10kHz) response fluctuation < 3dB

8.2.6.2 Speaker performance requirements

Choose speakers with low harmonic distortion.

Recommendation: 100 ~ 200Hz THD≤5% at rated power, 200 ~ 8000Hz THD≤3%

8.2.6.3 Structural design suggestions

- When designing the speaker cavity, avoid abnormal sound and vibration caused by structural resonance. When the speaker cavity is installed in the whole machine, it must be treated with shock absorption. The cavity must be at least 2mm away from other components, and the speaker diaphragm, passive diaphragm and other components must be at least 5mm away.
- It is recommended that the speaker and microphone be placed in different cavities, and the cavities are sealed with good performance sealing materials to prevent crosstalk inside the structure.
- MIC must be internally soundproofed with the SPK sound cavity to prevent the sound emitted by SPK from being directly transmitted to the MIC through the internal space of the machine. Silicone is generally used for sound insulation and shock absorption. The hardness of silicone needs to be designed according to the actual structure and the compression amount. Generally, it is required to be as soft as possible. MIC should be away from interference (exhaust fan) or vibration (speaker vibration, structural vibration) to avoid structural vibration causing a greater impact on MIC.
- For electret microphones, the protection of the microphone should be considered during the structural design and production process to avoid the loss of microphone consistency caused by extrusion. The microphone needs to be isolated from the solid surface by a silicone cover to reduce the vibration and sound transmission of the shell and to seal it.

The air tightness and distortion test methods of the speaker can be obtained from RTK after the machine is installed.

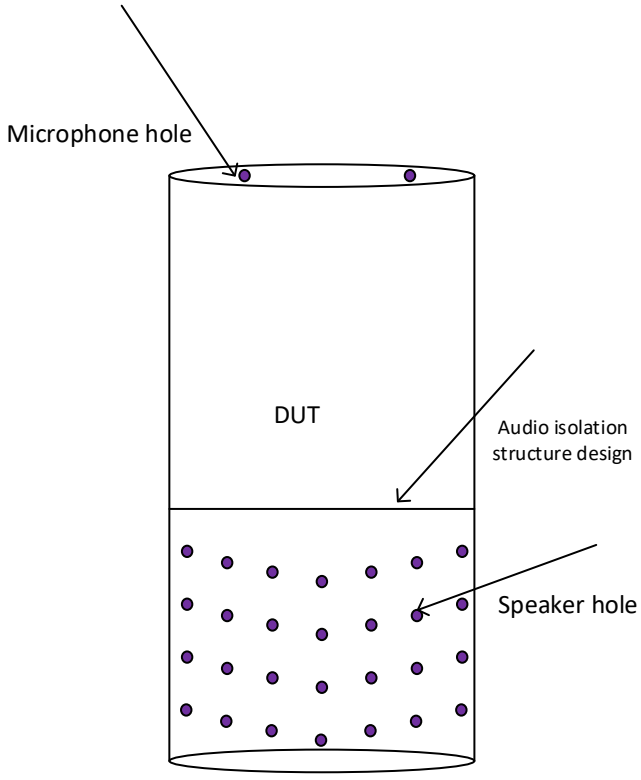


Figure 8-21 Speaker structure design reference diagram

8.2.6.4 Machine audio test method

The airtightness test audio document is as follows， password is RTK

https://drive.google.com/file/d/1GWCvCMDbhgdsBnC-_mbdv-CpNqg87NyR/view?usp=sharing

- External airtightness test process

1. Use an external speaker to play white noise at an appropriate volume, and use the microphone on the DUT to record. Record the state where the clay does not plug the microphone hole and the state where the microphone hole is plugged. The audio energy recorded in the

two states must differ by more than 15dB.

- Internal airtightness test:

Use the DUT speaker to play white noise at the maximum volume, and use the microphone on the DUT to record. Record the state where the clay does not plug the microphone hole and the state where the microphone hole is plugged. The audio energy recorded in the two states must differ by more than 15dB.

- Confirmation of speaker distortion:

Use the speaker on the DUT to play the swept frequency audio, and use the microphone on the DUT to record. The distortion of the recording file must meet the following requirements: 100 ~ 200Hz THD≤5% at rated power, 200 ~ 8000Hz THD≤3%

Sweep frequency audio file path， password is RTK

https://drive.google.com/file/d/1NyBgWgtf87HBCK5eW3rjHei0r04xcFzX/view?usp=sharing

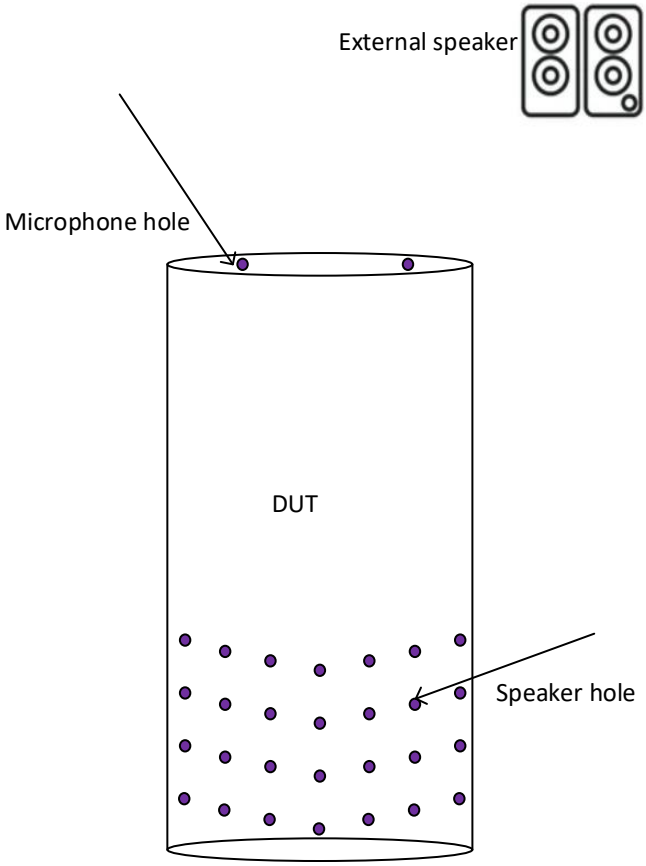


Figure 8-22 test scenario

9 General Purpose ADC

The General purpose ADC (GP-ADC) and Capacitive Touch Sensor multiplexes pin. The signal sampling of Capacitive Touch Sensor itself is also done through GP-ADC, and both of them are sensitive analog signal sensors, so we need to pay special attention to interference.

9.1 Input Range

The full amplitude range of the voltage measured by the external channel is 1.8 V instead of 3.3 V and that of BAT_MEAS Channel is 5 V.

9.2 Net Arrangement

GP-ADC has multiple channels that use a set of fixed pins of IC. Care should be taken to avoid using GPIO in the same group of GP-ADC as high-speed signal ports (I2C, SPI, etc.), as shown in Figure 9-1. If unavoidable, it is necessary to set it reasonably on the software to ensure that the high-speed signal has no action while GP-ADC sampling.

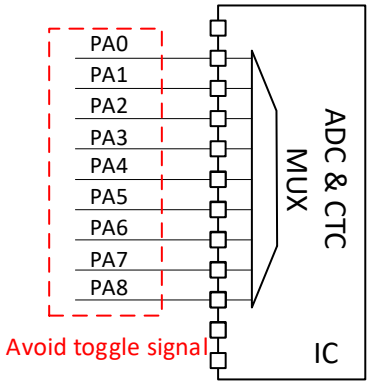


Figure 9-1 GP-ADC net arrangement

In addition, even if the high-speed signal is not arranged in the same set of the GP-ADC GPIO, it should not be arranged adjacent to the pin of the GP-ADC.

9.3 Input Impedance

In order to measure the voltage of 0 to 1.8V, a voltage divider is added to the front end of the GP-ADC. The resistance is fixed and cannot be modified, and the accurate resistance value can be obtained by reading the calibration value written in each IC.

Due to the divider resistor, the input resistance of the GP-ADC will be affected by it, and the typical value is 491kohm. It is necessary to pay attention to this situation in application. Take Figure 9-2 as an example, when the external resistance R2 of GP-ADC is about equal to the internal resistance R, there will be a deviation in the voltage collected by GP-ADC. If R2 is a thermistor, the temperature measurement may be inaccurate.

NOTE

Some products GP-ADC contain a battery dedicated channel for battery voltage detection, which receives 5V input voltage, the internal input resistance is about 150 kohm, and it is not calibrated. In application, it is noted that the source resistance should be much less than 150 kohm.

Therefore, when designing the external circuits, we should consider:

(1) R2 should be sufficiently small (less than 1 / 100 of R) to minimize the impact of internal resistance.
(2) If the requirements (1) cannot be met, the Rin value of the IC can be obtained through the API and incorporated into the circuit design.

Typically GP-ADC normal channel are used to measure the voltage of different sensor, such as NTC thermistor. The simplified block is as follows:

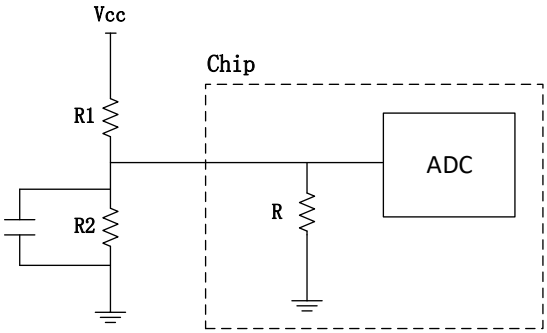


Figure 9-2 simplified application block

NOTE

VCC voltage needs to be less than or equal to 1.8 V.

There is a 500 kohm resistor to ground inside the chip which will affect the accuracy of GP-ADC with the combination of peripheral circuit. The ideal input voltage to GP-ADC is:

$$V_{\text{ideal}} = V_{\text{cc}} \times R_2 / (R_1 + R_2) = 3.3 \times \frac{R_2}{R_1 + R_2}$$

But the actual input voltage to GP-ADC is:

$$V_{\text{actual}} = V_{\text{cc}} \times \frac{R_2 // R}{R_2 // R + R1} = V_{cc} \times \frac{R_2}{R_2 + R_1 \times R_2 / R + R_1}$$

Compare the two formals, Vactual is smaller than Videal due to the impact of internal R. And the greater the ratio of R1xR2/R is, the greater the error between Vactual and Videal is. What's more, the resistance of internal R vary differently in multi chips which also can impact the accuracy.

For better accuracy, internal R should be calculated and its resistance value will be stored in OTP.

After calibration, if R2 is NTC thermistor, the actual resistance of R2 is:

$$R_2 = \frac{R_1 \times V_{\text{adc}}}{V_{cc} - V_{adc} - V_{adc} \times \frac{R_1}{R}}$$

By the way, it's optional for customers to choose another GP-ADC channel to measure the voltage of Vcc, which can reduce the impact that Vcc changes while GP-ADC Vref doesn't change:

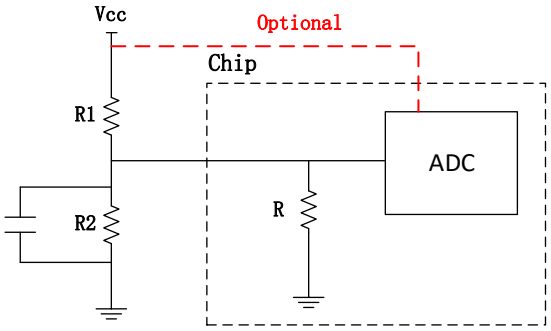


Figure 9-3 Optional application block

(3) R will be connected to the circuit only when the GP-ADC is sampling. Therefore, at the moment when the ADC sampling is turned on, the circuit will be switched, and the parallel C of R2 may slow the transient process of the circuit. There are usually two ways to solve

this problem:

a) When the requirement for sampling rate is not high, it can be sampled at intervals, and the interval time needs to exceed the circuit time constant. In this case, the instantaneous value of sampling is the voltage at the beginning of switching, that is, the voltage of the capacitor C. in this case, the circuit design requires that C be greater than 10nF.

b) when the sampling rate is strict and interval sampling is not acceptable, a delay can be added before each sampling of a group of data, which should be greater than 5 times the circuit time constant, and pay attention to clear the conversion result FIFO before reading the data.

9.4 ADC Calibration Principle

To improve the linearity of the input / output characteristics of the ADC, each IC will implement a nonlinear calibration of the ADC in the factory. With the nonlinear calibration, the gain and offset error of the ADC can also be reduced.The user can use the API to directly obtain the exact voltage conversion results that have been calibrated.

After calibration, each IC can find its own value of A, B and C and store them in one time program (OTP). The A and C are stored in the form of binary complement, while B is stored as an unsigned integer. When acquiring ADC code, use the following formula to get the current voltage with unit as mV, here parameter x is ADC code:

$$y = ax^2 + bx + c = \left(\frac{A}{2^{26}}\right)x^2 + \left(\frac{B}{2^{15}}\right)x + \left(\frac{C}{2^6}\right)$$

For example, if A, B, and C read from OTP are 0xff66, 0x6f91, and 0x53f, and ADC code is 1800. The original A is 0x809a, parameter a = -(0x9A)/2^26, parameter b = (0x6f91)/2^15, and parameter c = (0x53f)/2^6. So, the current voltage y = 1582mV.

Users can obtain the calibrated results directly through API: ADC_GetVoltage or ADC_GetVBATVoltage.

9.5 User Key Circuit

User Key circuit uses ADC sampling voltage to identify multiple key states using a single channel, and the pull-up voltage needs to be no more than 1.8V as shown in Figure 9-4.

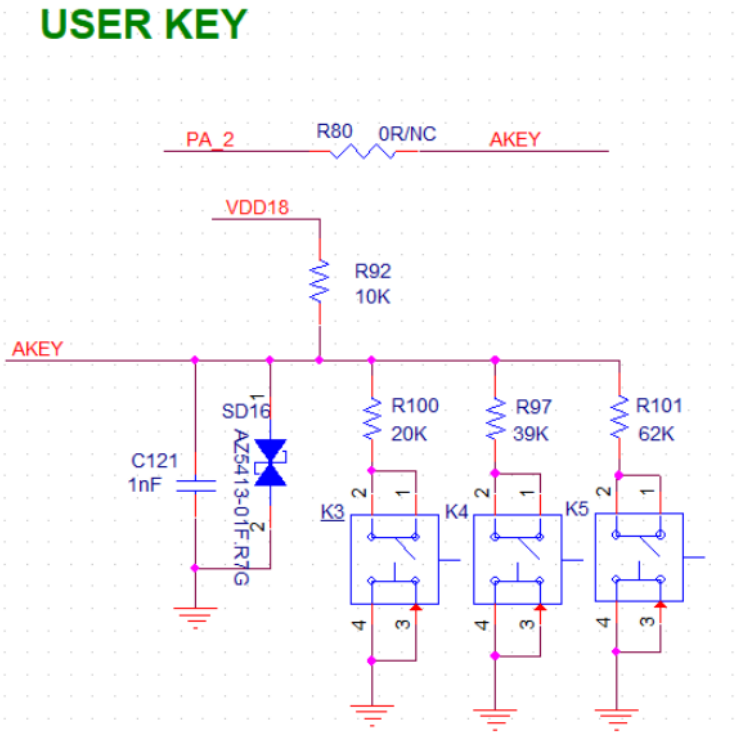


Figure 9-4 EVB - User Key circuit

Or change the voltage divider so that the sampling voltage of ADC is no more than 1.8V. Such as Figure 9-5.

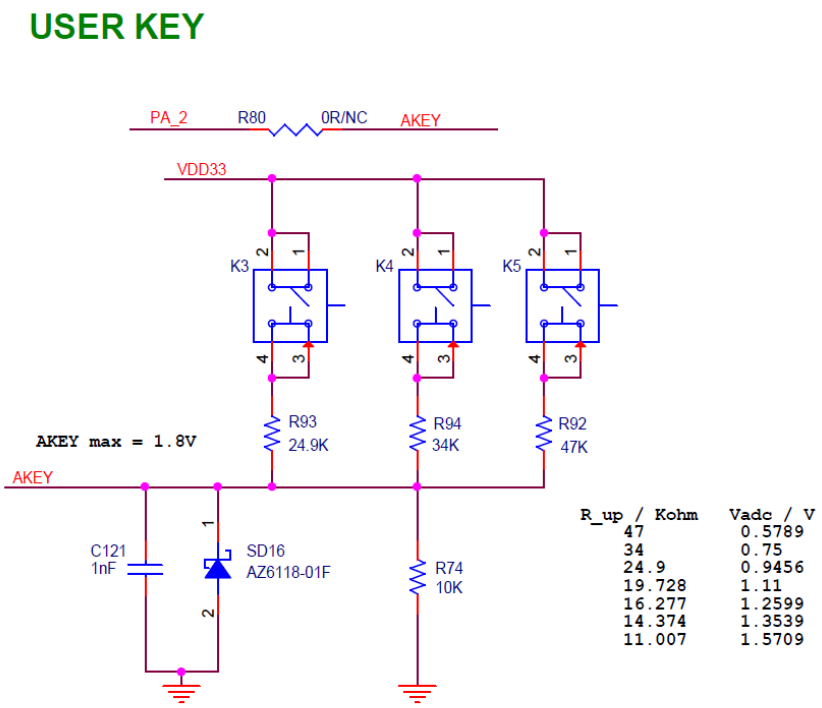


Figure 9-5 User Key circuit example

10 Capacitive Touch Sensor

10.1 Net Arrangement

- It is not recommended to reuse Capacitive Touch Sensor pins with other functions. High-speed signal lines (I2C, SPI, etc.) should not appear in the same group of Capacitive Touch Sensor pins. If unavoidable, it needs to be set reasonably on the software to ensure that Capacitive Touch Sensor works with no high-speed signal action
- It is suggested to keep the Capacitive Touch Sensor away from high speed signal and switching power net
- To prevent crosstalk, if only some Capacitive Touch Sensor channels are used, select channels at intervals and disable unselected channels
- Do not design a pull-up or pull-down voltage on the signal line
- Do not design bypass capacitors on the signal line

NOTE

Capacitive Touch Sensor's layout has a great impact on performance. For specific layout rules, please refer to layout guide.

10.2 Series Resistance

A resistor is connected in series in each Capacitive Touch Sensor channel (placed near the chip). This resistor and the parasitic capacitance on the signal path form a simple RC filter, which can partially filter out the noise interference and improve the ESD resistance. Due to the different circuit design, the resistance usually can not be accurately selected. The filter effect is poor when the resistance is too small, and the sensitivity is reduced because the resistance is too large. It is recommended to choose a resistance of 47-560 ohms.

In addition to using series resistance to improve ESD resistance, the TVS of each sensor channel should be connected in parallel to attenuate the impact of surge current on the sensor, but the junction capacitor of this TVS should not exceed 0.6 pF.

10.3 Button LED Design

When the button is made into a hollowed-out type, a LED can be added in the middle, and the light and darkness of the LED can be used to judge the situation of touching and leaving the finger. It is suggested that the power supply of LED should add RC filter to slow down the change rate of the level edge.

10.4 Max Input Voltage

The Capacitive Touch Sensor is an analog circuit, an ADC sample the input net continuously. The max input voltage of the input net is 0.85V. In particular, the use of too large Mbias can cause a charging voltage exceeding 0.85V, which may cause damage to the ADC.

11 USB

11.1 Introduction

The USB supports On-The-Go (OTG) and USB 2.0 specification. USB host does not support hub-insert detection.
It has the following features:

- Supports OTG1.3.
- Supports three speed modes:
  - High-Speed (HS, 480Mbps) mode.
  - Full-Speed (FS, 12Mbps) mode.
  - Low-Speed (LS, 1.5Mbps) mode only in USB host mode.
- Uses UTMI 16-bit MAC-PHY interface.

11.2 Device Mode Only

11.2.1 Insertion Detection

It is recommended to use GPIO to detect whether the device is plugged into the host.
The device often has the coexistence of USB power supply and battery power supply. When the USB is plugged in, the system detects a high level, and the system can automatically cut off the battery power supply to save unnecessary power consumption. Another advantage of this structure is that the USB can be in the power off state when the host is not connected, and the USB initialization is performed after the USB is detected to save power.

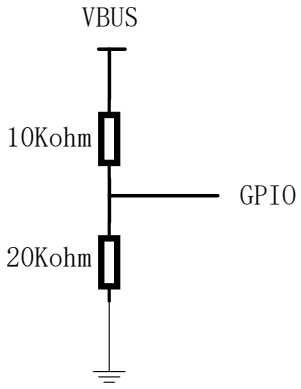


Figure 11-1 Insert detection structure

11.2.2 Type A

The software configures the force device mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- The VBUS comes from external host. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface shell and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.
- It is recommended to reserve a footprint for a capacitor to ground on both DP and DM close to the USB interface.

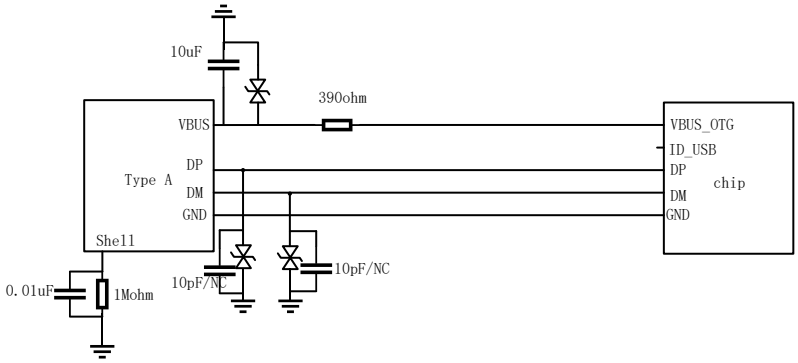


Figure 11-2 Device mode with USB type A interface

11.2.3 Micro AB

The software configures the force device mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- The VBUS comes from external host. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The DP/DM is connected in series with a resistor to prevent D+/D- signal overshoot with VBUS. The resistance is generally 2.5ohm and placed close to the USB interface. It is recommended to reserve a footprint for a capacitor to ground on each trace close to the USB interface.
- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.

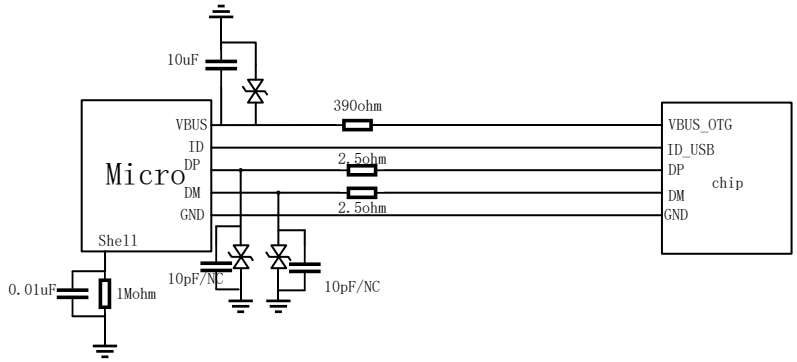


Figure 11-3 Device mode with USB micro interface

11.2.4 Type C

The software configures the force device mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- CC1/CC2 should be pull down with 5.1kohm to GND respectively.
- The VBUS comes from external host. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of

power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.

- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.
- It is recommended to reserve a footprint for a capacitor to ground on both DP and DM close to the USB interface.

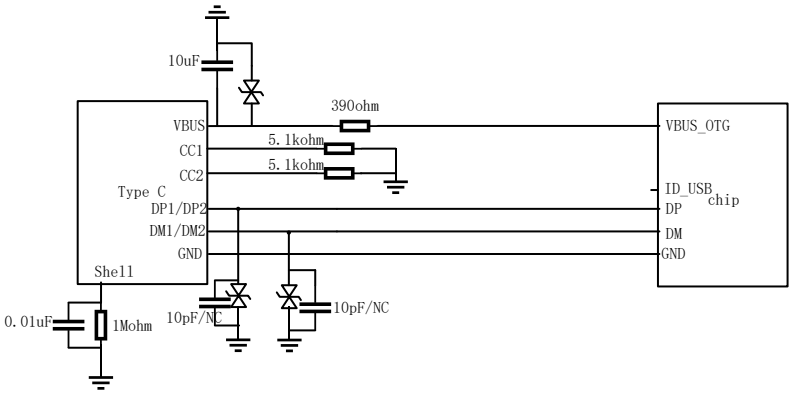


Figure 11-4 Device mode with Type C interface

11.3 Host Mode Only

11.3.1 Type A

The software configures the force host mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- The VBUS should come from chip. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.
- It is recommended to reserve a footprint for a capacitor to ground on both DP and DM close to the USB interface.

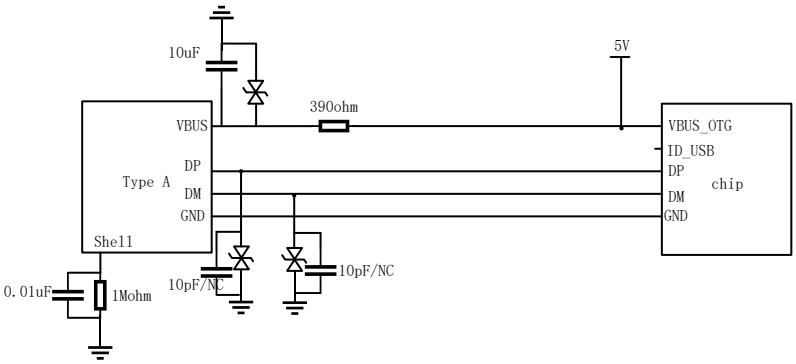


Figure 11-5 Host mode with USB type A interface

11.3.2 Micro AB

The software configures the force host mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- The VBUS should come from chip. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The DP/DM is connected in series with a resistor to prevent D+/D- signal overshoot with VBUS. The resistance is generally 2.5ohm and

placed close to the USB interface. It is recommended to reserve a footprint for a capacitor to ground on each trace close to the USB interface.

- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.

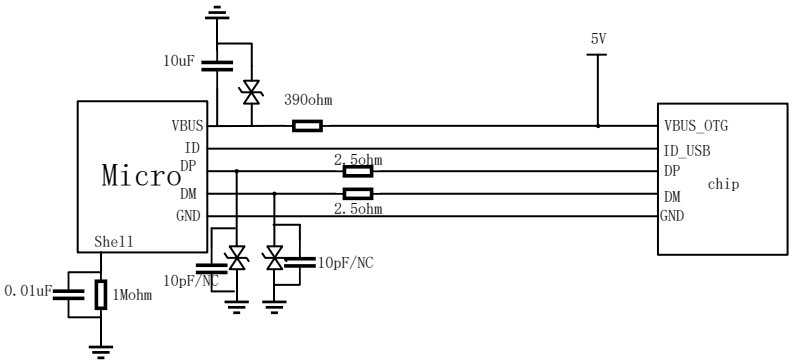


Figure 11-6 Host mode with micro USB interface

11.3.3 Type C

The software configures the force host mode. Pins ID_USB and VBUS_OTG can be floating or not, which will not cause leakage.

- CC1/CC2 should be pull up with 56kohm±20% to 5.0V respectively.
- The VBUS should come from chip. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.
- It is recommended to reserve a footprint for a capacitor to ground on both DP and DM close to the USB interface.

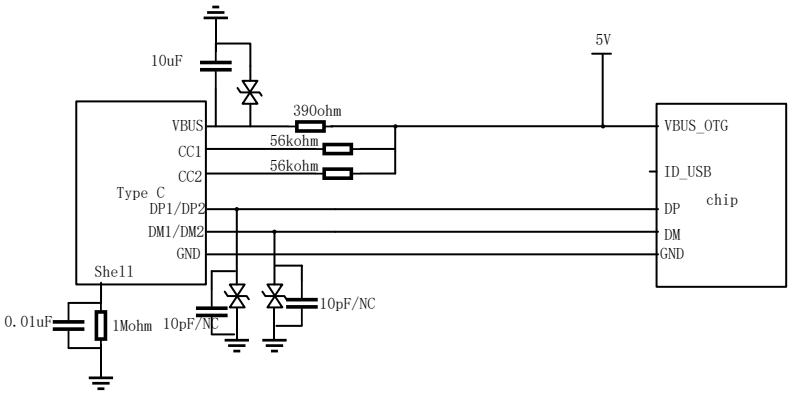


Figure 11-7 Host mode with Type C interface

11.4 OTG mode

11.4.1 Micro AB

It is recommended to use micro/mini USB interface for OTG function.

- The power switching module to control VBUS is necessary. It is self-powered in host mode and external-powered in device mode. As is shown in figure 8, if EN is low voltage, the chip acts as a USB device, VBUS is disconnected with 5V on chip. If EN is high voltage, the chip acts as a USB host, VBUS outputs 5V and supplies external devices.
- A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The DP/DM is connected in series with a resistor to prevent D+/D- signal overshoot with VBUS. The resistance is generally 2.5ohm and

placed close to the USB interface. It is recommended to reserve a footprint for a capacitor to ground on each trace close to the USB interface.

- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.

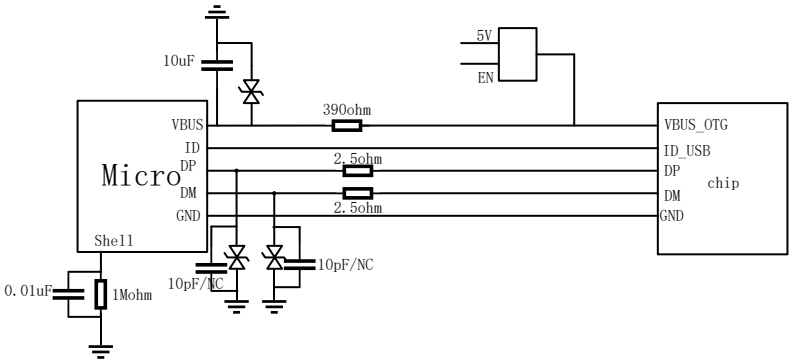


Figure 11-8 OTG mode with micro USB interface

11.4.2 Type C

- Type C interface requires a CC Logic chip to switch the pull-up and pull-down resistors. Other ICs, such as TUSB320, can be used to achieve the conversion between CC logical and ID.
- The power switching module to control VBUS is necessary. It is self-powered in host mode and external-powered in device mode. As is shown in Figure 11-9, if EN is low voltage, the chip acts as a USB device, VBUS is disconnected with 5V on chip. If EN is high, the chip acts as a USB host, VBUS outputs 5V and supplies external devices.
- A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in. The 390ohm resistor in series between VBUS and VBUS_OTG is also used to reduce power spike to VBUS_OTG.
- The TVS device should be put closely with USB interface to avoid chip damage or breakdown caused by ESD (Electro-Static discharge).
- The resistor and capacitor network between interface GND and ground can isolate the signal and reduce EMI and RFI emissions. The resistor and capacitor network should be as close to the USB connector as possible.
- It is recommended to reserve a footprint for a capacitor to ground on both DP and DM close to the USB interface.

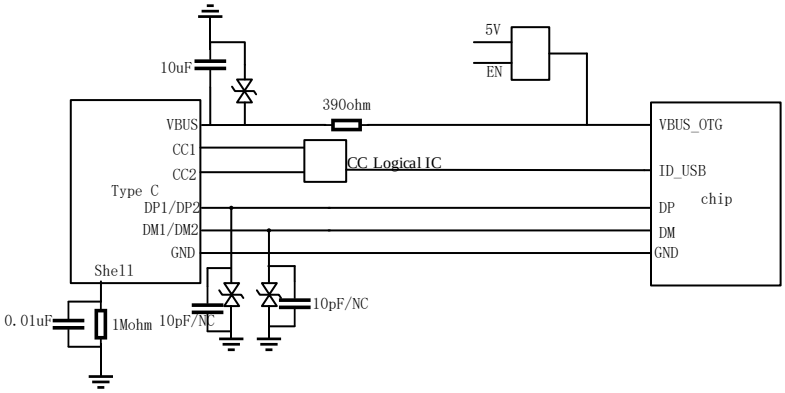


Figure 11-9 OTG mode with Type C interface

11.5 ESD Protection Requirements

DP/DM/VBUS need to be connected to ESD diode. The selection rules for ESD diode are as below:

- Working voltage (Vrwm) : The reverse working voltage (VRWM) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 2.0 data lines, the typical operating voltage 3.3V. This translates to a working voltage of greater than or equal to 3.3V. For VBUS, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.
- Parasitic capacitance: Since the signal speeds for USB 2.0 can reach up to 480Mbps, a low-capacitance ESD diode with less than 4pF is recommended to support the signal speed.
- Breakdown voltage (Vbr): The reverse working voltage (Vrwm) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected.

- Clamping voltage (Vc): The clamping voltage of the ESD diode is dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
- IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 2.0, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.

12 MIPI DSI

When using MIPI DSI, the VDH_IO5 (3.3V) and VAL_MIPI (0.9V/1.0V) power supplies of the chip need to be ensured to be correct. It is necessary to ensure that the backlight power supply of the external display screen is correct. Figure 12-1 is the reference circuit of the MIPI display used with Realtek EVB. For the layout of the MIPI circuit part, please refer to the layout guide document.

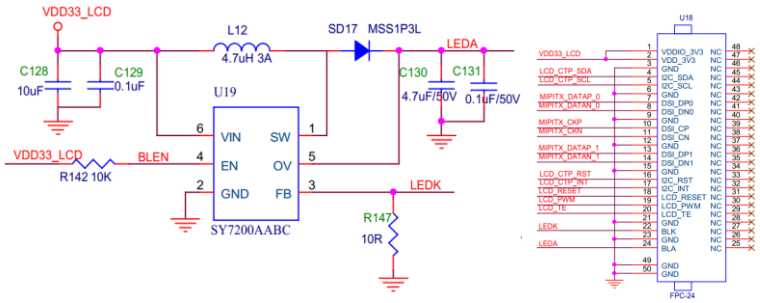


Figure 12-1 MIPI DSI peripheral circuit reference design

13 External Flash

13.1 Introduction

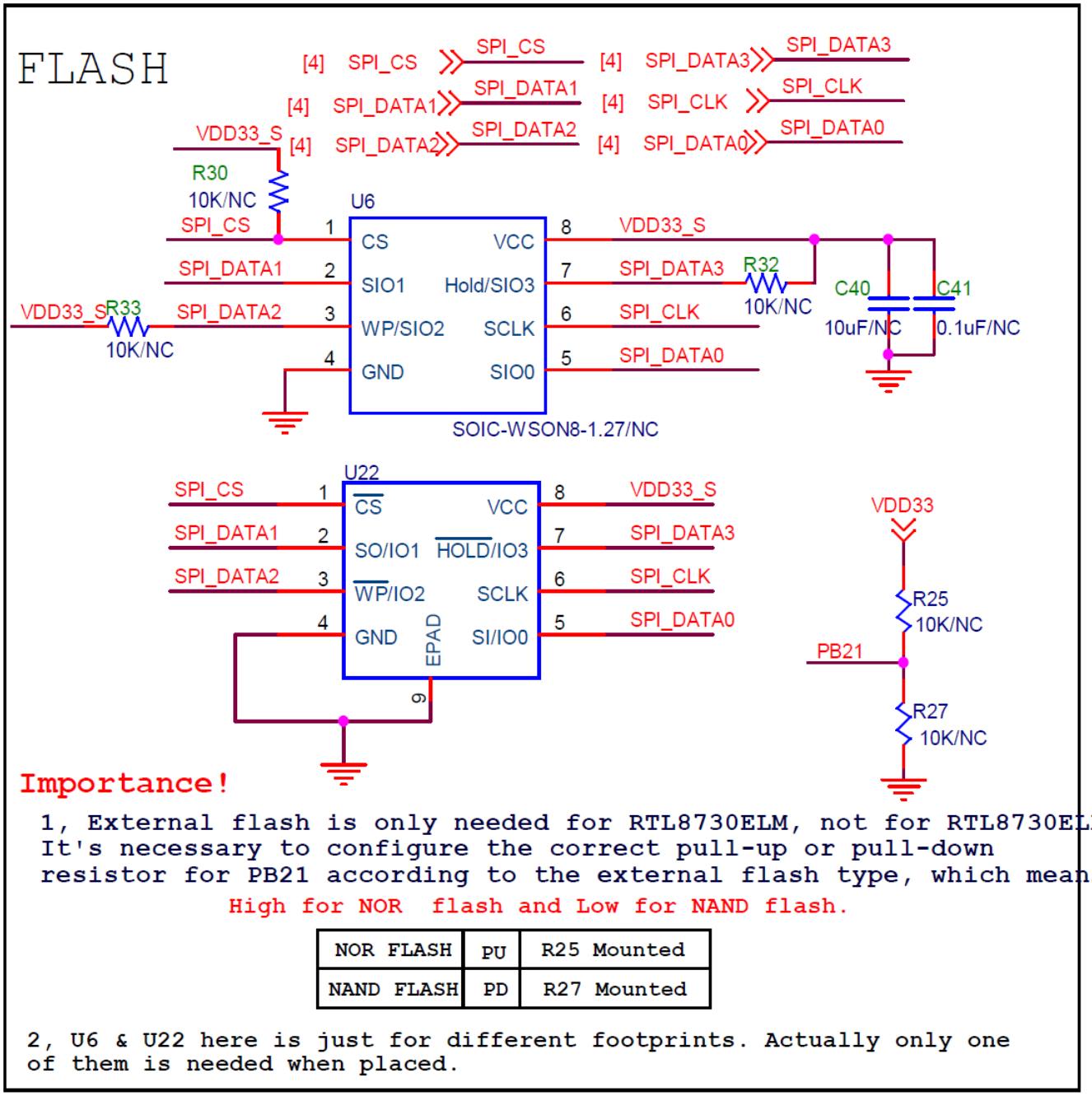
The SPIC is used to communicate with SPI Flash Devices (Flash). Flash SPI can only be configured as master with Max. Baud rate: 100MHz.

13.2 Flash Selection Requirements

- Specific part numbers RTL8730ELM-VA8, RTL8730ELM-VA7 and RTL8730EAM-VA6 need external flash. All the other part numbers including RTL8730ELH&RTL8730EAH have embedded NOR/NAND flash.
- Flash SPI in RTL8730E can only operate in typical 3.3V. Users need to select flash with adaptive operating voltage range.
- The compatible flash can be found in Flash AVL. If the expected flash to be used is not in AVL, please contact RTK for more information.

13.3 Schematic Reference Design

- External flash is only needed for RTL8730ELM and RTL8730EAM, not for the other types of RTL8730E.
- When external flash is needed, the chip needs to get the type of external flash based on the status of PB21 during power on. Logic high represents NOR flash and logical low represents NAND flash. It's necessary to configure the correct pull-up or pull-down resistor for PB21
- U6 and U22 here is just for different type footprints of flash. Only one of them is needed in actual use.
- CS, WP and Hold pins reserve pull-up 10K resistors to avoid bus floating. In RTK EVBs, these resistors are not mounted while using internal pull-up resistors in RTL8730E.
- VCC for external flash requires a filtering capacitor connected to ground, usually one large and one small capacitor connected in parallel, such as 10µF and 0.1µF.



14 I2C

14.1 Introduction

The I2C has the following features:

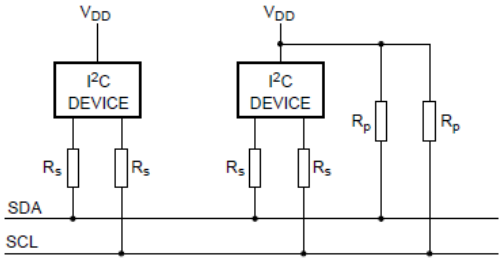
- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three speed modes:
  - Standard Speed (SS), up to 100Kbps
  - Fast Speed (FS), up to 400Kbps
  - High Speed (HS), up to 3.4Mbps and up to 1.7Mbps
- Master or Slave I2C operation

14.2 Schematic Reference Design

- Part of the pads used for I2C can switch to 4.7K pull-up resistor internally (PA19~PA27, PA30, PA31, PB0~PB12). However, the internal pull-up resistance value of other pads is too large and not suitable for I2C communication. Suggest users to reserve pull-up resistors externally to adjust the resistance value according to their own needs.
- Different speed modes have requirements for the maximum allowable load of the I2C bus. In standard, fast and 1.7M high speed modes, the bus load cannot exceed 400pF, and in 3.4M high speed mode, the bus load cannot exceed 100pF.
- Calculation method for pull-up resistance of I2C bus:
  The voltage value of IO Power determines the minimum value of pull-up resistance. When IO Power is 3.3V, the minimum allowable value of pull-up resistance is 1K, and when IO power is 1.8V, the minimum allowable value of pull-up resistance is 0.5k. The size of the bus load determines the maximum allowable pull-up resistance, and the calculation formula is as follows:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

  In the formula, t_r represents the maximum signal rise time allowed under different speed modes (Standard: 1000ns, Fast: 300ns, High Speed: 80ns), and C_b represents the bus load.
- The I2C protocol also defines resistors Rs connected in series on SDA and SCL lines. The function of this resistor is to effectively suppress interference pulses on the bus from entering the slave device and improve reliability. The selection of this resistor is generally around 100~200 Ω. This resistor is not necessary and can be used in harsh noise environments.



15 General SPI

15.1 Introduction

- RTL8730E supports Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol.
- Master or slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps

NOTE

1. When the chip is configured as Master, SPI supports transmission with a maximum baud rate of 50Mbps. But when the chip is configured as Slave, whether it can support a maximum baud rate of 50Mbps is controlled by the connected master. Due to the path delay and pad delay of internal signals in the master and slave devices, as well as some delays that may be introduced by pads or PCBs, the connected master needs to support delayed sampling function in order to correctly receive data sent by the slave at 50Mbps baud rate.

2. Dedicated SPI has many groups and does not allow cross group use between signal lines.

15.2 Schematic reference design

Generally, four signal wires (CS, CLK, MISO, and MOSI) can be directly connected to external device. You can pull CS pin up to Vcc by a 10K resistor, so that the CS pin has a certain high level state to avoid bus floating.

16 SWD

16.1 Introduction

Debug Interface supports Arm® standard bi-directional Serial Wire Debug (SWD) to pass data to and from the debugger and the target system in a highly efficient and standard way. It provides a probe interface consisting of two signals—TCK and TMS. The TMS signal is bidirectional and carries control information to the adapter and data in both directions. The TCK signal (max baud rate: 20MHz) is sourced from the probe.

16.2 Schematic reference design

- It is recommended to connect a 22R damping resistor in series at the source of both SWDIO and SWDCLK signals to suppress signal reflection.
- It is recommended to connect one ESD protection device in parallel on each of the SWDIO and SWDCLK signal traces, as manual hot swapping is required during debugging.
- According to the SWD standard, it is recommended to configure the SWD data pad to pull-up state after power on.

16.3 Application note

PA13 and PA14 are default configured as SWD interface but users can configure relevant register to switch these two ports to normal GPIO. If users use PA13 and PA14 for other functions except SWD and connect the two ports to external circuits, it is recommended that users avoid SWD toggle behavior with a risk of misidentification before switching off the SWD function from the two ports.

17 SDIO Host

17.1 Introduction

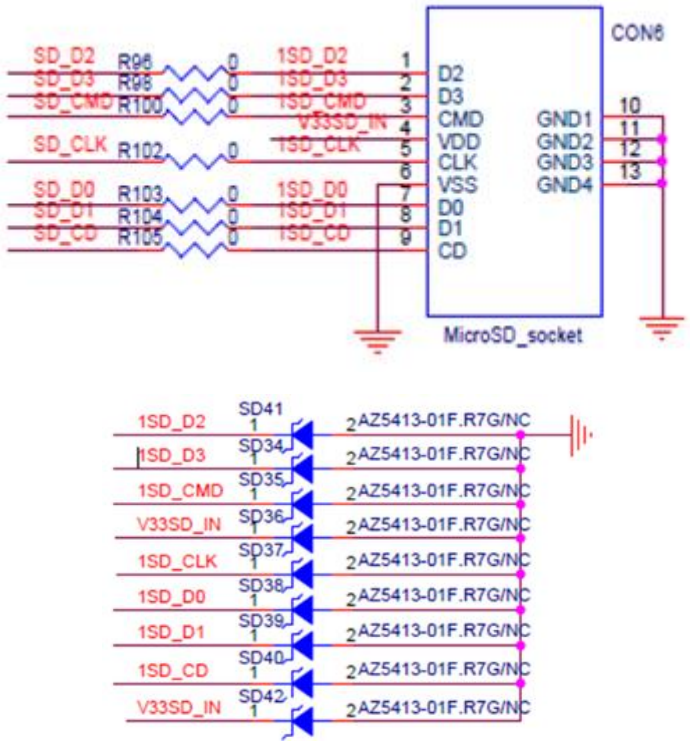
The SD/MMC card interface is responsible for access SD memory card and eMMC device. It features:

- Compliance with SD memory card specifications version 2.0 and Multi-Media Card (MMC) system specification version 4.5.
- SD
  - 1-bit and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
  - Card detect with debounce function
- eMMC
  - 1-bit mode and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
- 3.3V or 1.8 V operating voltage

17.2 Schematic reference design

17.2.1 MircoSD

- Each SD card cable (power and signal lines) needs to be connected to an ESD diode. The selection rules for ESD diodes are as follows:
  - The working voltage V_{RWM} of the ESD diode is greater than the highest operating voltage of the circuit.
  - The parasitic capacitance of the ESD diode is required to be less than 30pF.
  - The breakdown voltage V_{BR} of the ESD diode is greater than the highest operating voltage of the circuit.
  - The clamping voltage Vc should be less than the maximum peak voltage that the protected chip can withstand.



- The four data cables from D0 to D3, as well as the CMD cable, need to be externally pulled up to IO Power. The pull-up resistance is generally between 10K and 100K.

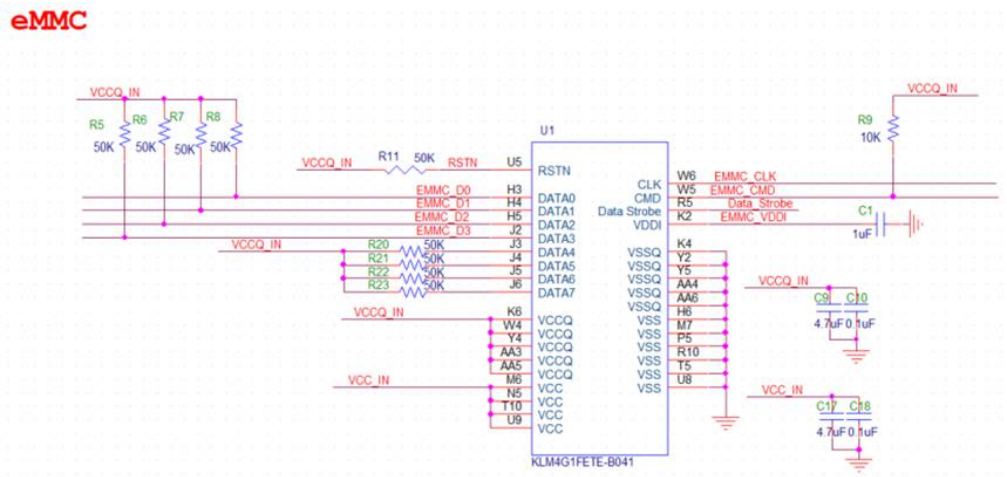
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be adjusted by users according to their needs, usually between 0~47 Ω. The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value.

- The VDD of the SD card requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.

17.2.2 EMMC

The schematic design considerations related to external EMMC chips are recommended to refer to the reference design of actual EMMC chips. This section is based on Samsung's EMMC Board Design Guide.

- The VSSQ and VSS pins of the EMMC chip are all grounded, and VCCQ is connected to IO power. VCC is power supply for the internal memory of the EMMC chip.



- To avoid bus floating, it is recommended to reserve 50K pull-up resistor to VCCQ for the four data pins from Data0 to Data3. Although Data4 to Data7 cannot be used, it is also recommended to reserve 50K pull-up resistor to VCCQ (if the chip end has already done internal pull-up, these pull-up resistors can be removed). CMD pins must be pulled up to VCCQ with 10K resistor.
- For the RSTN pin, since the chip does not use H/W reset, this pin does not need to be connected to the chip side. However, 50KΩ must be pulled up to the RSTN pin, as it must be in a high level state for the EMMC chip to function properly.
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance solder pad at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be selected by customers according to their needs, usually between 0~47 Ω. The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value.
- The VCCQ and VCC of the EMMC chip both need to be connected to the ground with a set of decoupling capacitors, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF. If the VCCQ of EMMC is from the same source as VCC, only one set of decoupling capacitors is needed.
- The VDDI pin needs to be connected to ground with a capacitor to prevent EMI interference and stabilize the output of the internal regulator of the EMMC chip. Suggested capacitance value is 1μF~4.7μF.
- If the chip supports DDR400 mode, the data strobe pin requires an external pull-down resistor of 10K~100K. Since our chip does not support DDR400, we cannot use this pin, so we can float it, connect an external pull-up resistor or an external pull-down resistor

Revision History

Date	Version	Description
2024-05-15	R1.0	Initial release
2024-07-12	R2.0	Update I/O characteristic, PINMUX, Audio content
2024-07-23	R2.1	Corrected the description of trap pin PB21, Update external flash content
2024-11-18	R2.2	Add chapter 8.2.2/8.2.3/8.2.6/16.3
2025-07-23	R2.3	Add chapter 7.5 Usage limitation. ADD BT interfere PA4/5/15/16 description.