RTL8721FA/RTL8721FC/RTL8721FL
PCB Layout and Assembly Guide

This document provides the PCB layout and assembly guideline

Rev. 01

Sept. 2025

Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

DISCLAIMER

Please Read Carefully:
Realtek Semiconductor Corp., (Realtek) reserves the right to make corrections, enhancements, improvements and other changes to its products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

Reproduction of significant portions in Realtek data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Realtek is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions.

Buyers and others who are developing systems that incorporate Realtek products (collectively, "Customers") understand and agree that Customers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Customers have full and exclusive responsibility to assure the safety of Customers' applications and compliance of their applications (and of all Realtek products used in or for Customers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Customer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Customer agrees that prior to using or distributing any applications that include Realtek products, Customer will thoroughly test such applications and the functionality of such Realtek products as used in such applications.

Realtek's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation kits, (collectively, "Resources") are intended to assist designers who are developing applications that incorporate Realtek products; by downloading, accessing or using Realtek's Resources in any way, Customer (individually or, if Customer is acting on behalf of a company, Customer's company) agrees to use any particular Realtek Resources solely for this purpose and subject to the terms of this Notice.

Realtek's provision of Realtek Resources does not expand or otherwise alter Realtek's applicable published warranties or warranty disclaimers for Realtek's products, and no additional obligations or liabilities arise from Realtek providing such Realtek Resources. Realtek reserves the right to make corrections, enhancements, improvements and other changes to its Realtek Resources. Realtek has not conducted any testing other than that specifically described in the published documentation for a particular Realtek Resource.

Customer is authorized to use, copy and modify any individual Realtek Resource only in connection with the development of applications that include the Realtek product(s) identified in such Realtek Resource. No other license, express or implied, by estoppel or otherwise to any other Realtek intellectual property right, and no license to any technology or intellectual property right of Realtek or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Realtek products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of Realtek Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from Realtek under the patents or other Realtek's intellectual property.

Realtek's Resources are provided "as is" and with all faults. Realtek disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any epidemic failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights.

Realtek shall not be liable for and shall not defend or indemnify Customer against any claim, including but not limited to any infringement claim that related to or is based on any combination of products even if described in Realtek Resources or otherwise. In no event shall Realtek be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of Realtek's Resources or use thereof, and regardless of whether Realtek has been advised of the possibility of such damages. Realtek is not responsible for any failure to meet such industry standard requirements.

Where Realtek specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Customers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any Realtek products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death. Such equipment includes, without limitation, all medical devices identified by the U.S.FDA as Class III devices and equivalent classifications outside the U.S.

Customers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Customers' own risk. Customers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Customer will fully indemnify Realtek and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's

non-compliance with the terms and provisions of this Notice.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

Contents **4**

1 Introduction **6**

2 Power **6**

2.1 Switch Regulator Layout 6
2.2 Power Trace Routing 6

3 Crystal **8**

4 RF **8**

5 Shielding **9**

6 Flash **9**

7 SDIO **9**

8 USB **10**

9 LCDC **10**

10 Cap Touch Controller (CTC) **10**

10.1 Key Performance Parameters 10
10.1.1 Sensitivity *10*
10.1.2 Signal-to-Noise Ratio *10*
10.1.3 Crosstalk *10*
10.2 Board layers (PCB) 11
10.3 Overlay 12
10.4 GND 12
10.5 Sensor Trace 12
10.5.1 Trace *12*
10.5.2 Via number and position *13*
10.5.3 Series resistor *14*
10.6 Sensor Interface 14
10.6.1 Button *14*
10.6.2 Spring *14*

11 General Analog-to-Digital Converter (ADC) **15**

12 RMII **16**

12.1 Placement 16
12.2 Signal and Trace Routing 16

13 Audio **17**

14 Land Pattern and Assembly **17**

14.1 Guideline for E-pad land patterns 17
14.1.1 The E-pad Design *17*
14.1.2 Solder Mask Guidelines for E-pad *17*
14.1.3 Paste Mask Guidelines for E-pad *17*
14.1.4 Center pad hole specification *18*
14.2 Signal I/O pad design 18
14.2.1 Guidelines for perimeter land patterns *18*
14.2.2 Solder Mask guidelines for perimeter lands *18*
14.3 Stencil Design Guidelines 19
14.3.1 Stencil Type and Thickness *19*

14.3.2 Solder Paste Type(s) *19*
14.4 Oven temperature profile 19
Revision History **22**

1 Introduction

This document is suitable for RTL8721FA, RTL8721FC, and RTL8721FL.

2 Power

2.1 Switch Regulator Layout

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, LX, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- The input bypass capacitor CIN must be placed as close as possible to the VAH_DCDC pin and avoid vias between CIN and VAH_DCDC pin.
- LX pin is noise node switching with high frequency voltage swing and should be kept at small area. These feedback, analog, digital components and PCB trace keep away from the LX node to prevent stray capacitive noise pickup.
- Make VAH_DCDC, VOUT, and ground bus connections as wide as possible. These power trace length, width, and vias need to depend on recommend operating input and output current. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- VAM_LDOC is feedback pin for DCDC. Make sure there is a capacitor between the inductor L1 output and the FB pin VAM_LDOC and avoid vias between capacitor and VAM_LDOC pin.
- For better thermal performance, design a wide and thick plane for E-PAD or add a lot of vias to connect ground layer plane.

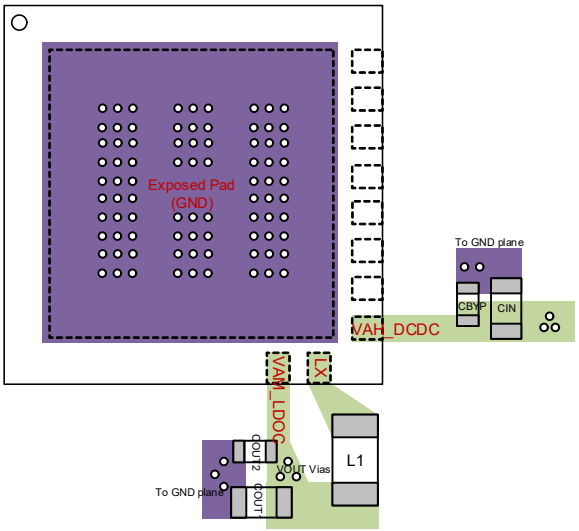

Figure 2-1 Switch Regulator Layout Reference of QFN Package

2.2 Power Trace Routing

- The path of the power trace is recommended using star routing as shown in Figure 2-2 for better noise isolation among circuit blocks. It is strongly recommended that the power trace for PA and DCDC (VRH_PA_G for 2.4G, VRH_PA_A for 5G, VRM_RF for BT, VAH_DCDC for DCDC) is routed separately.

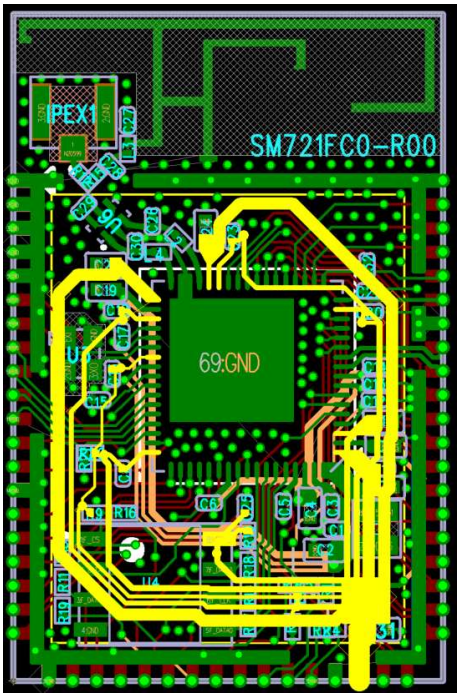

Figure 2-2 Star Routing

- The power trace should be wide enough for lower IR drop.
- Max current for every power pins is shown as follows, as a reference for determining the trace width.
- Generally, the width of VRH_PA_G/VRH_PA_A shall be ≧20mil.

Table 2-1 Max. Current of Power Pins

Pin No.				Pin name	Pin type	Description	Max. Current(mA)
RTL8721FAF	RTL8721FAM	RTL8721FCM	RTL8721FLM				
1	1	1	1	VAH_DCDC	P	Power input for DCDC	300
2	2	2	2	LDOM_OUT	P	Power output of LDOM	100
3	3	3	3	VAH_LDOM	P	Power input for LDOM	120
-	-	4	4	VAH_RTC	P	Power input for RTC	5
7	7	8	8	VAL_USB	P	Power input for USB	50
8	8	9	9	VDL_CORE	P	Power input for the digital core domain	350
11	11	16	24	VAH_ADC	P	Power input for the ADC	5
12	12	17	25	VDH_IO0	P	Power input for the digital I/O	50
-	-	-	26	VDH_IO1	P	Power input for the digital I/O	50
19	19	29	42	VRH_PAD_A	P	Power input for RF circuit	50
20	20	30	43	VRH_PA_A	P	Power input for RF circuit	450
25	25	35	49	VRH_PA_G	P	Power input for RF circuit	450
26	26	36	51	VRM_RF	P	Power input for RF circuit	150
27	27	37	52	VRH_SYN	P	Power input for RF circuit	50
28	28	38	53	VRM_SYN	P	Power input for RF circuit	50
31	31	41	56	VAH_XTAL	P	Power input for XTAL	20
32	32	42	57	VAM_AFE	P	Power input for RF AFE	50
37	37	51	76	VDH_IO2	P	Power input for the digital I/O	50
38	38	58	87	VDL_CORE	P	Power input for the digital core domain	350
45	-	-	-	VDH_FLASH	P	Power input for Flash	50
-	45	65	97	VDM_PSRAM	P	Power input for PSRAM	50
46	46	66	98	LDOC_OUT	P	Power output of LDOC	350
47	47	67	99	VAM_LDOC	P	Power input for LDOC	350
48	48	68	100	LX	P	DCDC output	600

3 Crystal

- The high speed (≥10 KHz) signal traces shall be keep far away from XI/XO pins and trace.
- Place an intact GND plane with shortest distance connected to the E-PAD under the whole crystal routings. If the GND can't be connected to E-PAD directly, there should be noisy current flowing on this GND plane.
- If the dielectric core of the PCB is too thin(ex: ≦3mil), the high parasitic capacitance on XI/XO routings may dominates the crystal frequency, then the GND under the routes shell be removed, and the high speed signal traces on the lower layers shall be kept far out of the empty (under crystal block) area.
- Signal and power trace near XI/XO should be isolated by ground.
- The crystal should be kept out in top layer.
- Keep whole XI/XO traces in the same layer.

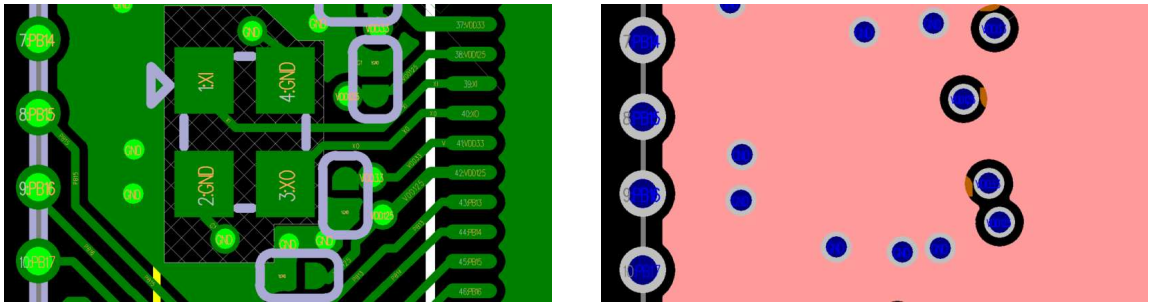

Figure 3-3-1 Crystal Layout-TOP Layer, GND Layer

4 RF

- The characteristic impedance of RF trace should be 50Ω.
- Placing more GND vias along the RF trace is recommended.

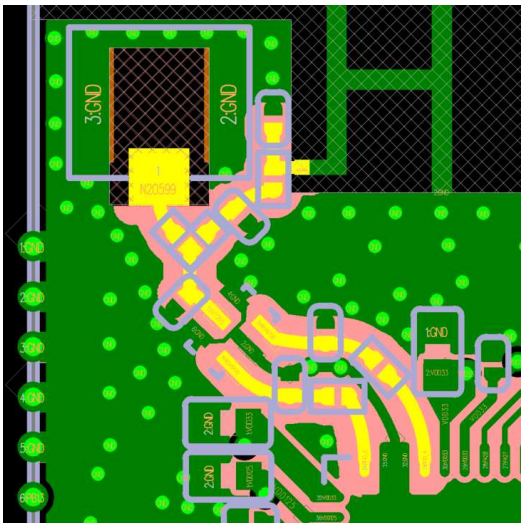

Figure 4-1 RF Trace

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces. The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

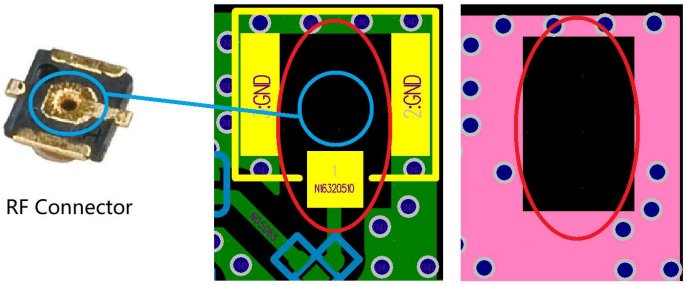

Figure 4-2 Keep-out for RF connector

5 Shielding

- Considering the EMC design, must comply with the following design rules:
  - For good shielding case grounding, there must be GND via placed on/around the soldering pads and the recommended via spacing is a≤1.5mm.
  - The open gap is recommended b≤2mm.
  - Use separated shielding cases if the other circuit blocks need to be shielded as well.
  - The shielding cover soldering on PCB is recommended If do use joint shielding case (frame + cover), make sure that the cover touches the compartment frame firmly.
  - Height: if possible, the inner height suggestion≥maximum component height + 0.5mm.

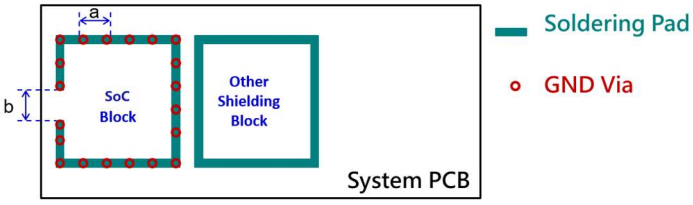

Figure 5-1 Shielding Layout

6 Flash

- Place the matched resistance close to the transmitting side.
- Flash should be placed as close to SOC as possible.
- Suggest placing the flash signal traces on the same layer without drilling vias to avoid EMI issues.
- The data and clock traces should be length-matched and surrounded by ground plane or trace. The error between each data trace and clock trace should be controlled within 900mil.
- Ensure that the spacing between traces is greater than three times the trace width and reference plane is intact. Avoid placing signal traces close to high frequency signals.
- The trace width of VCC (power supply) should be reasonably selected according to the current size.

7 SDIO

- The data and clock traces should be length-matched and the error between each data trace and clock trace should be controlled within 900mil. The clock trace should be surrounded by ground traces.
- To control the load of layout, the length of each signal trace should not be too long and should be controlled within 6 inch.
- Ensure that the spacing between traces is greater than three times the trace width and reference plane is intact. Avoid placing signal traces close to high frequency signals.
- Place the matched resistance close to the transmitting end.
- The capacitors on the signal traces or power traces should be placed close to the interface position.

8 USB

- D+ and D- are wired in a differential manner, and through the continuous reference plane layer to ensure the consistency of impedance, the differential impedance of the signal trace is Z=90Ω±15%.
- The USB interface specifies a current of 500mA, but the VBUS trace must be able to withstand a current of 1A to prevent overcurrent events.
- The traces of D+ and D- must be of the same length, and the length error should not exceed 150mil. Instead of right angles, obtuse angles or arc traces are required. The maximum number of vias is 3, please minimize the use of vias to reduce signal reflection and impedance.
- The distance between the USB signal and other CLK or differential signal traces should be >20mil;
- If ESD protection devices and common mode inductors are required, they should be as close to the interface as possible；
- Avoid wiring the USB data signal traces under or near crystal oscillators, crystals, clock signal generators, power inductors, mounting holes, magnetic devices or ICs.

9 LCDC

- Place the matched resistor close to the transmitting end.
- Keep trace lengths matched (especially for R/G/B data traces within the same byte), to minimize skew. The length mismatch between data and clock traces should be kept under 2000mil.
- Ensure a solid ground plane beneath data and clock traces to provide a low-impedance return path, and it is recommended to evenly distribute ground vias around data and clock traces.
- Keep data and clock traces away from noisy and sensitive signals (e.g., RF, XTAL, power, switching circuits), maintain 3x trace width spacing between parallel RGB traces to reduce coupling.
- Use decoupling capacitors near the LCD connector.

10 Cap Touch Controller (CTC)

- In a typical Cap-Touch application, sensors are constructed with traces on a FR4/FR2 or flexible printed circuit (FPC). Cap-Touch layout design is an important step in the design phase, following the PCB layout design guidelines can help your design achieve higher noise immunity, lower parasitic capacitance (CP), and higher signal-to-noise ratio (SNR). The following factors must be considered during layout.

10.1 Key Performance Parameters

10.1.1 Sensitivity

- The ratio of the change in the sensor sampled value when touched to the base value. The smaller the parasitic capacitance (CP) and the larger the touch capacitance (CF), the easier it is for the controller to detect a touch event (higher sensitivity). During design, increasing the sensor area, reducing the touch gap, shortening the trace length, and keeping the traces and sensors away from the copper pad can all improve sensitivity. The parasitic capacitance of the line from the IC to the sensor end to ground should not exceed 16pF.

10.1.2 Signal-to-Noise Ratio

- The ratio of the change in the sensor sampled value when touched to the peak-to-peak value of the noise sampled value when the sensor is idle. The signal-to-noise ratio should be greater than 5:1. Increasing sensitivity and suppressing ambient noise can improve the signal-to-noise ratio.

10.1.3 Crosstalk

- When adjacent touch sensor channel traces are arranged parallel and adjacent to each other without a ground shield between them, crosstalk is likely to occur between channels. Specifically, when a touch occurs, the sampled value of one channel changes significantly, while the sampled value of the adjacent channel also changes significantly. Shielding and good PCB grounding can attenuate crosstalk.

- Typically, low system sensitivity makes threshold setting difficult, while setting the threshold too low can easily lead to false triggers. Improving the signal-to-noise ratio and mitigating crosstalk require special attention. Filters can be used to improve the signal-to-noise ratio, but these filters can also delay system response. Therefore, the design of a Cap-Touch system requires comprehensive consideration of multiple aspects, minimizing adverse factors in all links to improve overall system performance.

10.2 Board layers (PCB)

- Sensor pads or sensor interfaces should be on the top (or bottom) side and surrounded by the hatched ground;
- All other components (ICs, VDD and GND traces, other signal traces) should be on the bottom (or top) side, and sensor traces are connected to the sensor pads or sensor interfaces by vias;
- Do not place the trace under the sensor button, and it is recommended not to be placed on the sensor layer for a long distance to prevent mis-touch caused by fingers touching the trace;

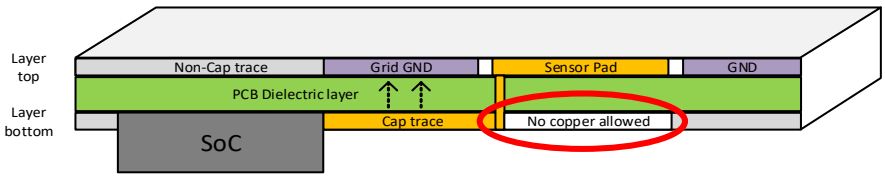

Figure 10-1 two-layer PCB

- Copper foil near sensors or traces increases parasitic capacitance. It is recommended to hollow out the area directly below the sensor without copper filling. If electromagnetic interference coupling near the sensor is unavoidable, a gridded ground plane should be installed on the same layer and directly below the sensor and traces to reduce RF radiation and interference.
- It is not recommended to lay solid copper foil directly below or on the same layer near the sensor, as this will significantly reduce sensitivity.
- For four-layer or multi-layer PCB. There should be no GND copper foil (including grid ground) on the layers directly below the sensor, because in the stacked structure of most PCBs, the distance between the first and second layers is relatively close, and the distance between each layer is not greater than the spacing between two layers of the board.

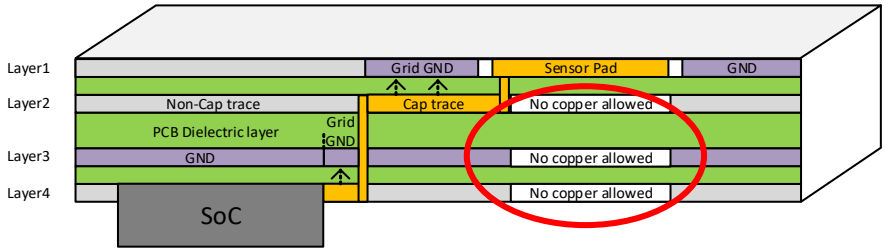

Figure 10-2 four-layer PCB

- Thin PCB application: when the thickness of PCB is less than 1.0mm or FPC soft board PCB application, the opposite of sensor should not lay GND to reduce the parasitic capacitance;
- Reliable grounding: The GND of the Cap-Touch component should be reliably grounded to prevent "dead copper" grounding;
- Connector: If the sensor button and the SoC are not on the same PCB layout, the FPC usually needs to connect two PCB. To minimize parasitic capacitance, it is recommended to select a small package pad connector (no copper or grid laying under the connector), and the length of the FPC should be shortened as far as possible;

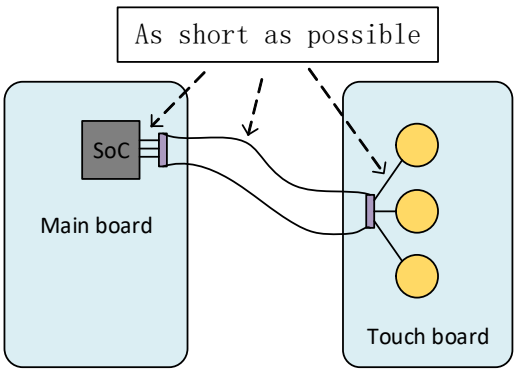

Figure 10-3 Connection of two boards

10.3 Overlay

- Covering the sensor with a non-conductive dielectric layer can adapt to more applications and reduce hazards such as ESD;
- The presence of the covering layer will significantly reduce the sensitivity, so laying a thicker covering layer may reduce the touch experience;
- Generally, the finger capacitance is directly proportional to the dielectric constant of the cover layer and is inversely proportional to the thickness of the cover layer. It is recommended to use materials with a higher dielectric constant, while the thickness of the cover layer should be as small as possible;
- As the air dielectric constant is very low, it is best to use glue to fix the air gap between the sensor and the cover layer.
- The thickness of the overlay shall not exceed 3.0mm, and it is recommended to be within 2.0mm. Touch sensitivity may be severely reduced unless a larger diameter sensor PAD is used;

10.4 GND

- The distance between the sensor button (or pad) and the floor on the same layer is at least 1.5 mm;

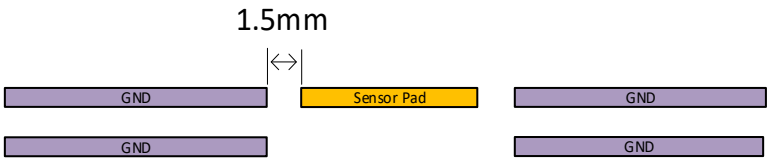

Figure 10-4 Gap between PAD and GND

- Copper is not recommended to lay under the sensor. If copper must be laid, choose grid copper. The grid site specification near the sensor is (Example Value):
  - Top layer (sensor in the same layer): 25% (7 mil line width, 45 mil spacing), see Figure 10-5;
  - Opposite layer: 17% (7 mil line width, 70 mil spacing).
- It is not recommended to have a large area of solid copper foil near the sensor button, which can be made by grid laying copper transition, and the width of the transition zone is at least 2 mm;

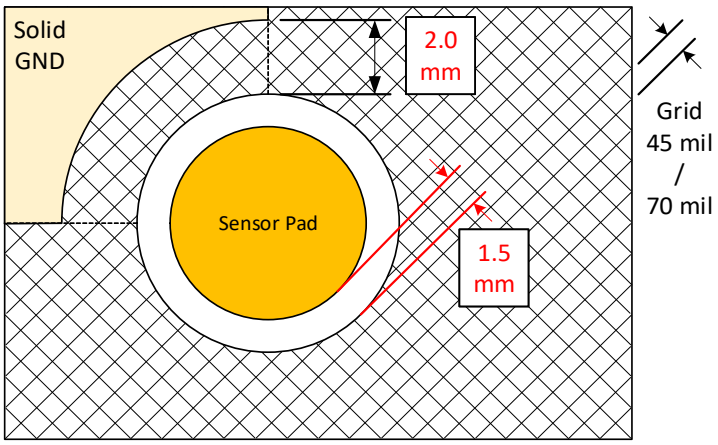

Figure 10-5 GND grid

- The distance between the sensor trace and the grid laying of the same layer is at least 0.5 mm. Likewise, the GND at the bottom layer of the trace should also be a grid.

10.5 Sensor Trace

10.5.1 Trace

Sensor trace connects IC and touch PAD, which is also the main way to introduce interference.

- Stay away from high-speed signals (RF, I2C, SPI, etc.) and high-power and high-noise trace (switching power supplies, etc.) as far as possible, and pay special attention to avoid parallel lines with them. If it is unavoidable, it is necessary to ensure that the intersection is at right angles;

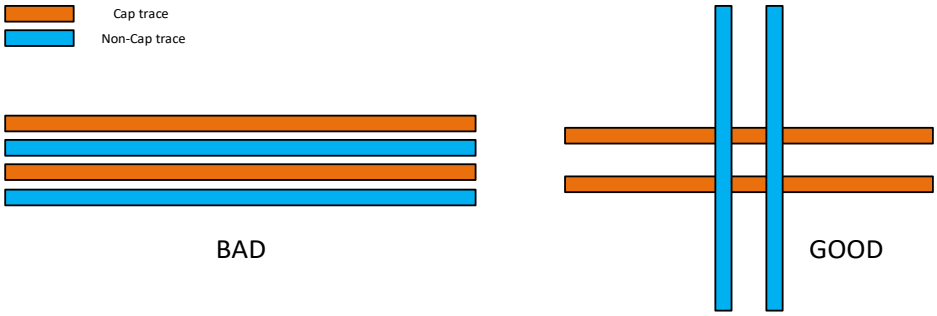

Figure 10-6 trace intersection

- If the sensor trace cannot be avoided parallel to the high-speed signal trace, GND with enough vias needs to be laid between the two to shield;

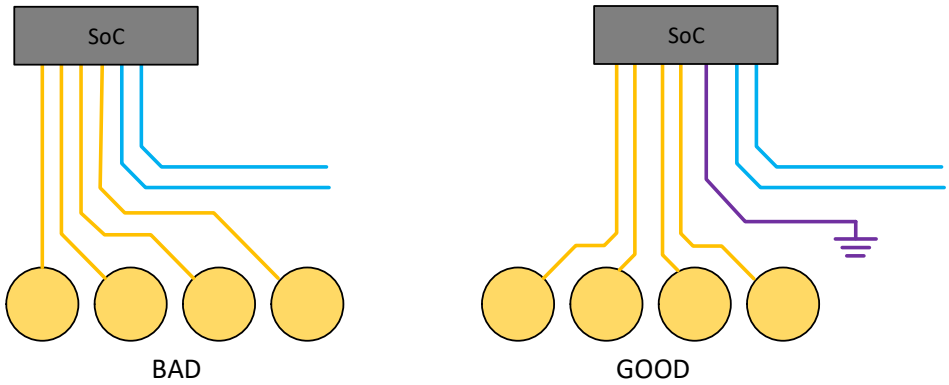

Figure 10-7 trace arrangement

- In order to prevent crosstalk, the parallel trace between the two adjacent channels is as far away as possible or lay GND between them. If only some of the all channels are used, the number of channels can be selected at intervals, and the software disables the unselected channels. If it is unavoidable, the distance between adjacent trace should be more than 3 times its trace width;
- The trace should be short and fine as far as possible, usually the maximum length on the PCB is < 30 cm, it is recommended that the trace width of 5 ~ 6 mil. Like other signal lines, the corners should not be right angles or sharp angles;
- The gap between the trace and GND is 0.5mm;
- The other layers of the PCB overlap area use a grid ground with the same specifications as the sensor buttons. One detail: When drawing the grid ground line, note that the "lines" that make up the grid cannot overlap with the trace of sensor, see Figure 10-8.

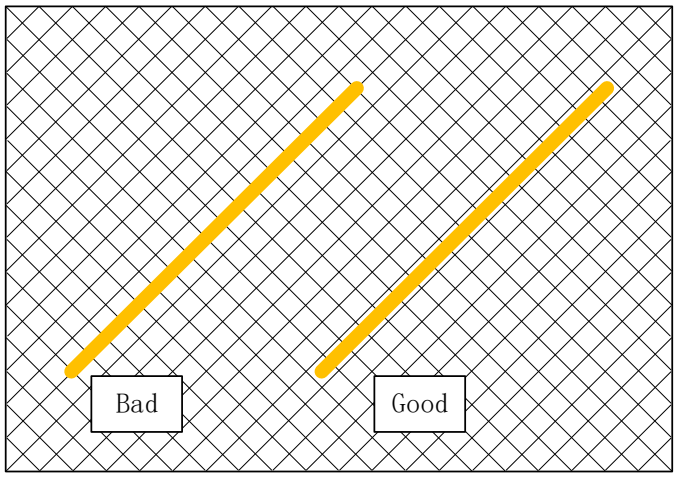

Figure 10-8 Grid detail

10.5.2 Via number and position

In order to reduce the parasitic capacitance and minimize the number of vias, it is recommended that the number of vias should not exceed 3. To shorten the trace, the via can be placed on the edge of the sensor.

10.5.3 Series resistor

All cap-touch channels suggest have a series resistance placed close to the chip to reduce RF interference and provide ESD Protection.
Due to different circuit designs, the resistor value cannot usually be accurately selected and needs to be tested and determined in actual product applications. If the value is too small, it will not play a filtering role, and if the value is too large, it will easily cause a decrease in sensitivity. It is recommended to choose a resistor of 47~560 ohms.

10.6 Sensor Interface

10.6.1 Button

- The Sensor PAD shape is recommended to be round. In some applications, it can be a ring, with a LED in the middle, it is necessary to note that the LED trace is isolated from the TOUCH signal. LED also suggests adding RC filtering to delay the edge of the signal;

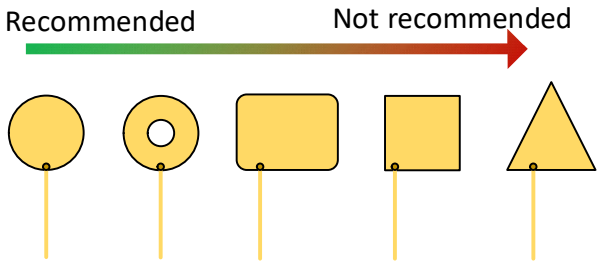

Figure 10-9 Sensor shape

- According to the size of the area touched by the finger, the button size recommends a circular diameter of 10.0mm~18.0mm. The larger PAD can better capture the finger touch signal, in the case of thick cover, the PAD area should be increased properly, and otherwise the sensitivity will be seriously reduced. Similarly, if a spring button is used, increasing the spring diameter can also increase sensitivity;
  - However, the button area should not be too large, because buttons that exceed the finger area do not further enhance sensitivity, but instead lead to increased parasitic capacitance and cost;

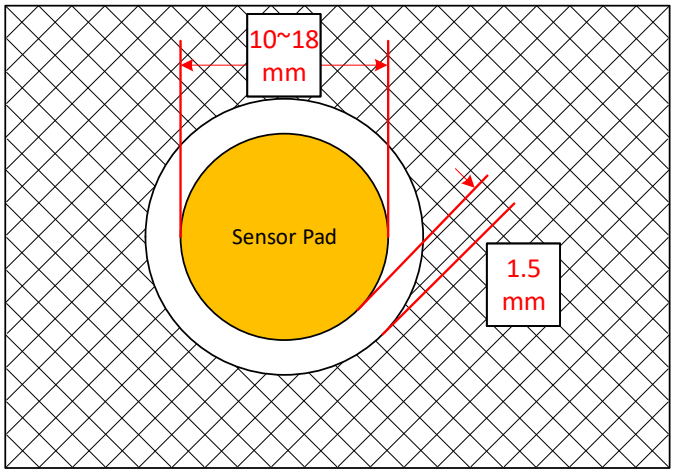

Figure 10-10 Sensor PAD on the PCB

- The gap between the PAD and the surrounding GND is generally 1.5mm~2.5mm. If there is a cover layer (protection overlay), the width of the gap should be increased appropriately increased;
- The spacing between adjacent PADS should be as large as possible to prevent the fingers from pressing multi-PAD. The button is recommended to be separated by more than 8mm;
- On the PCB, do not lay ground wires and signal lines on other layers where button pads overlap. Leave them clear or lay a grid ground.

10.6.2 Spring

In some applications, PCB cannot be directly arranged on the user touch surface, or the shape of the touch surface is irregular. Therefore, it is necessary to use conductors to connect the PCB sensor and the user touch interface. The metal spring is usually used as the elastic connector between the two, and the electric field is coupled to the overlay through the compressed spring.

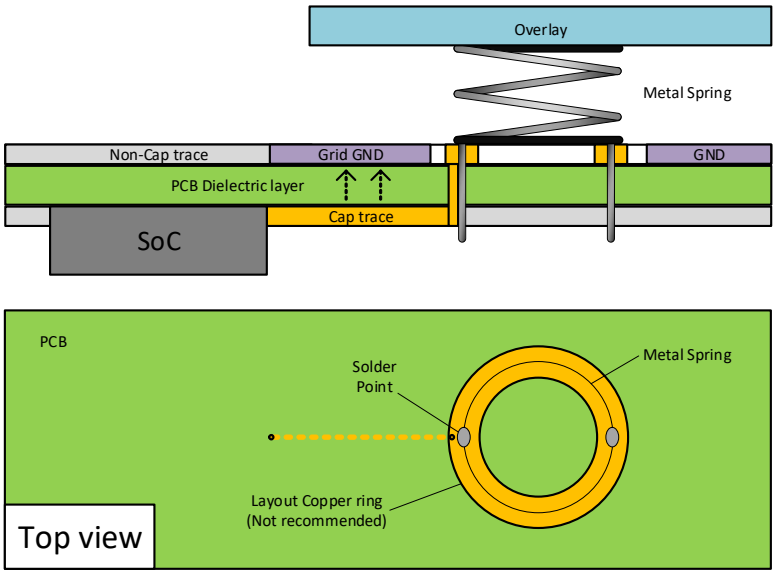

Figure 10-11 Spring diagram

- The spring has high side sensitivity, the adjacent spring needs to be far away from each other to prevent accidental touch;
- When the cover layer is thicker, the spring diameter should also be increased. Using a large diameter spring can improve sensitivity, but it may also affect the mechanical arrangement. Special-shaped springs such as trumpet-shaped and top inner spiral can be used to improve user experience;
  - The area of the top of the spring (the end close to the finger contact), like the PAD button, cannot be less than 10mm;
  - If an oversized spring is unacceptable, a more recommended approach is to use a spring with a tip-specific treatment;
  - The top of the spring can be processed as follows: spiral inward, expand outward, and cover the top with copper.

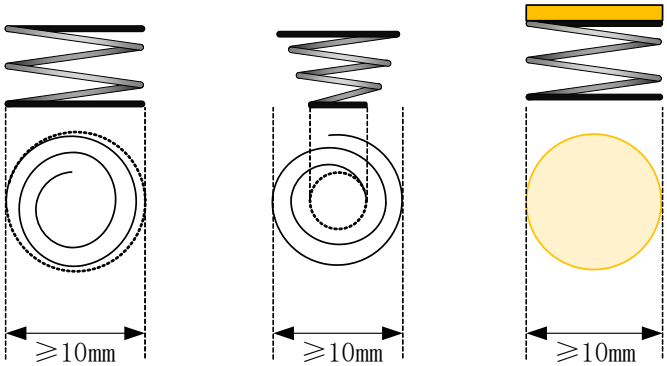

Figure 10-12 Spring processing

- When the spring is used as a sensor, the PAD can be a ring, or only the hole for mounting spring;
- There is at least 1.5 mm gap between the sensor ring and GND;
- The contact part of the spring and the PCB is far away from another signal and the GND;
- LED indicators can also be set in the middle area of the spring, as described in the previous section.

11 General Analog-to-Digital Converter (ADC)

- The routing shall be required to avoid parallel arrangement with high-speed signal traces and high-current power traces. If intersection cannot be avoided, it shall be as vertically as possible; if parallel arrangement, separation GND shall be laid between them.
  - The sources of interference include: SWR power trace and inductor, RF trace, High speed communication interface and so on.
- GND is arranged around the traces as much as possible.
- The traces should be as short as possible.

12 RMII

System designers should follow basic rules in layout and placement， general termination ，filter, plane partitioning, and EMI reduction in order to optimize designs. Following these rules will greatly contribute to a properly functioning hardware system
This guide has the following goals:

- Create a low-noise, power-stable environment
- Reduce the degree of EMI/EMC
- Simplify the task of routing signal traces

12.1 Placement

- The MAC should be placed as close as possible to the PHY. Other placement rules of PHY, RJ45 or magnetics, please refer to the PHY's layout guide
- RTL8721F can provide the 25MHz or 50MHz clock to the PHY, if the PHY need a delicate crystal , the crystal should be placed far away from IO ports， high frequency signals traces (TX, RX, power)
- Decoupling capacitors should be placed as close as possible to the power pins, the distance from the IC power pin to the capacitors is less than 200mils
- Place the RC filter component close to the source of the REFCLK. If the REFCLK direction is MAC to PHY (input to PHY), place filter network close to MAC site. If the REFCLK direction is PHY to MAC (output from PHY), place filter network close to PHY site

12.2 Signal and Trace Routing

- Avoid digital signals (RMII or clock signals) interference with analog signals (RF, RMII PHY TX/RX) and power traces. If it is necessary to cross digital signals with analog/power , the cross should be made at a 90° angles
- Ninety-degree trace turns should be avoided, we recommend that the traces turn at 45° angles. Reducing the trace length will reduce trace inductance during quick energy bursts
- Keep all RMII traces as short as possible, especially the trace of clock(REFCLK, EXT_CLK_OUT if used) and high speed signals (TXD/RXD) should be as short and wide as possible (compared to normal digital traces), it is better to have a ground plane under these traces. If possible, use a GND plane to surround them (Figure 12-1).

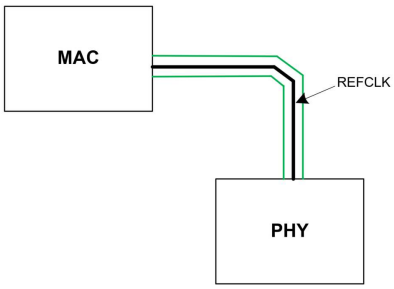

Figure 12-1 RMII REFCLK surrounded by GND

- All RMII traces should be referenced to an unbroken ground or power plane
- REFCLK (50MHz) and EXT_CLK_OUT (25MHz or 50MHz) from RTL8721f are high speed signals, keep a 20mils spacing between clock and data signals
- Match each TX(TXD/TXCTL/REFCLK) group and RX(RXD/RXCTL/REFCLK) group trace length to within 100mils
- Route the RMII traces at 50ohms impedance and use strip line to reduce radiation
- Router the RMII traces away from IO traces to avoid crosstalk (Figure 12-2)
- MDS signals routing rules please refer to the PHY's layout guide

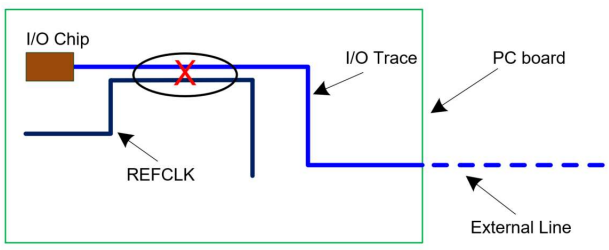

Figure 12-2 clock and IO trace

13 Audio

- The positions of the MIC peripheral devices are placed according to the requirements of the schematic diagram.
- The ESD device must be placed close to the MIC, and the traces drawn from the MIC must first pass through the ESD device before connecting to other devices.

14 Land Pattern and Assembly

- Refer the Package Specification in the datasheet for the detail dimension.
- Recommended to use the normal value in the dimension table.

14.1 Guideline for E-pad land patterns

14.1.1 The E-pad Design

- The center pad size should follow the same E-PAD size of package specifications in the datasheet.

14.1.2 Solder Mask Guidelines for E-pad

- The actual solder mask opening size should adding 2mil at each side to the size of the thermal pad.

14.1.3 Paste Mask Guidelines for E-pad

- Stencil openings should be segmented in exposed regions, solder paste coverage recommend matrix by 3*3 as follows:

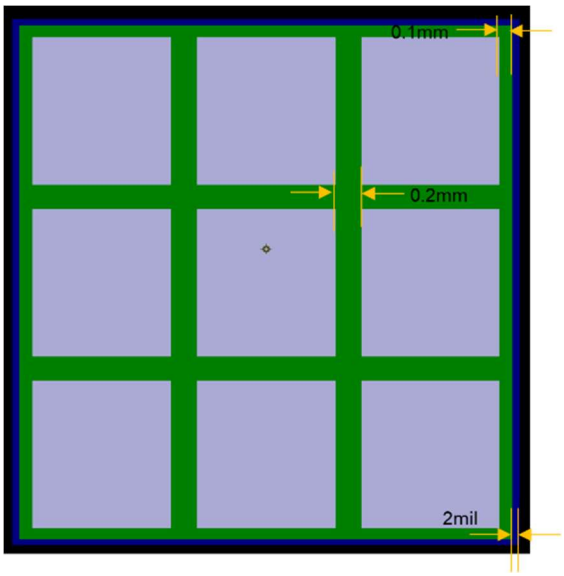

Figure 14-1 Paste Mask of Thermal Pad

- Recommended edge length/width of a matrix land is about 0.1mm.
- Distance between the lands should be about 0.2mm.
- Above two the ratio is 1:2
- Exposed pad design by matrix methods to prevent mass solder let QFN lift, stencil opening should be approximately 60~80% PCB exposed pad size.
- Thermal Pad voiding suggestion <30%

14.1.4 Center pad hole specification

- Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 0.6~1mm grid, as shown in Figure 11-2.
- And the vias under E-pad should be as much as possible for good heat dissipation. Large package like QFN100/QFN144 can use larger size of via and bigger pitch. But for small package size like QFN48/68, it should use smaller size of via and smaller pitch.
- The vias under the E-pad are recommended to be treated with epoxy via plug for low void.

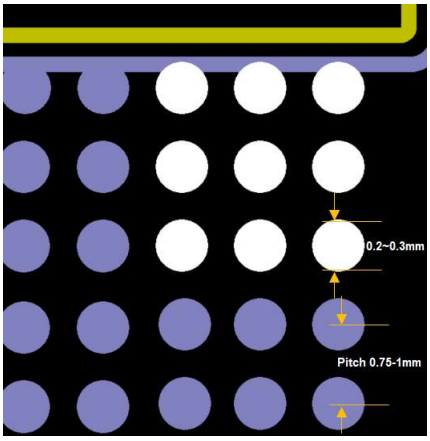

Figure 14-2 PCB Exposed Pad Land Pattern Via Grid

14.2 Signal I/O pad design

14.2.1 Guidelines for perimeter land patterns

- Extend of outer Cu Land towards package center as follows:

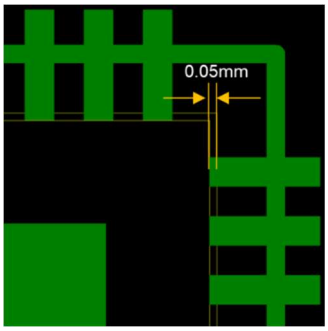

Figure 14-3 Length of outer lead perimeter size towards package center

- Length of Outer Cu land exterior to the package edge ≥ 0.2~0.3 mm

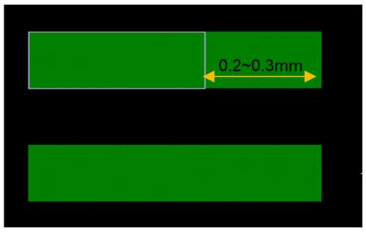

Figure 14-4 Length of outer lead perimeter size to the package edge

14.2.2 Solder Mask guidelines for perimeter lands

- The solder mask can be extend 2mil than the original size of each edge.

- As the follow picture, the orange part is the pin pad. And the red part is the solder mask. The yellow distance is 2mil.

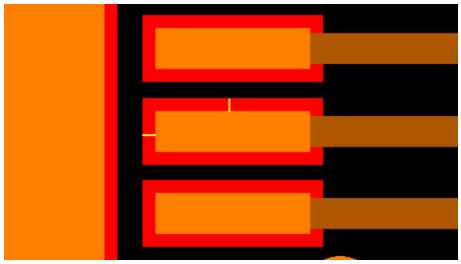

Figure 14-5 The pin pad and the solder mask

- I/O pin lead pitch will be small and small, If PCB fab technology ability is not enough space available for solder mask, we suggestion IC lead pitch low then 0.4mm PCB pad design use “trench” type solder mask opening to design .

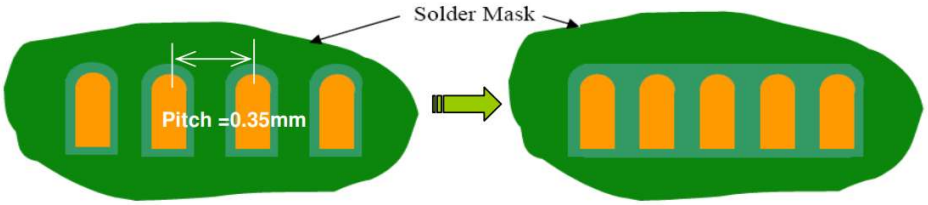

Figure 14-6 between the pads, it’s recommended to use “trench” type solder mask opening to design.

14.3 Stencil Design Guidelines

14.3.1 Stencil Type and Thickness

- Stencil type: Laser-Cut.
- The recommended stencil thickness as follows:

Table 14-1 Stencil Thickness

Terminal Pitch	Recommend Stencil Thickness
≥ 0.65	0.13 ~ 0.15mm
0.4 ~ 0.5	0.1 ~ 1.12mm
< 0.4	0.08 ~ 0.1mm

14.3.2 Solder Paste Type(s)

- The most common solder paste powder sizes for SMT are type 3 (T3), type 4 (T4), and type 5 (T5). The lower the number, the larger the particle size within the solder powder.

14.4 Oven temperature profile

- The reflow condition used in J-STD-020 as following table. All the temperature is measured on the topside of the package.

Table 14-2 Oven Control Data

Stage	Note	Pb-free assembly
Average ramp-up rate	T_L to Tp	3 ℃/ second max.
Preheat	Temperature min (T_{smin})	150℃
	Temperature max (Tsmax)	200℃
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217℃
	Time (t_L)	60 – 150 seconds
Peak package body temperature (Tp)		See following table. Tp must not exceed the specified classification temp in following table.
Time(tp) within 5℃ of the specified classification temperature (Tc)		30 seconds
Ramp-down rate (Tp to T_L)		6 ℃ / seconds max.
Time 25℃ to peak temperature		8 minutes max.

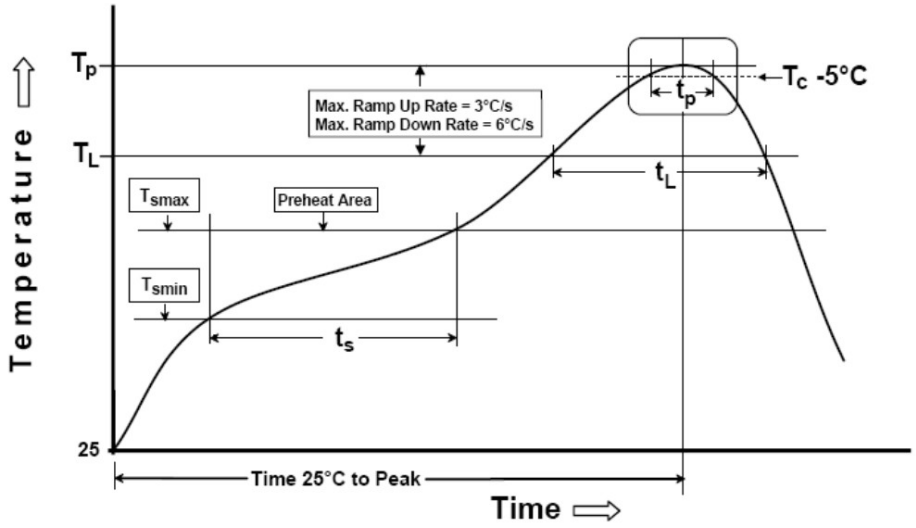

Figure 14-7 Recommended reflow profile

NOTE

The above reflow profile is for MSL classification only, not the recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameter in above table.

- The peak temperature package can sustain depends on its volume and thickness. The reason is that, engineering studies have shown that, thin, small volume SMD packages reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, technical and/or business issues normally require thin, small volume SMD packages to be classified at higher reflow temperatures.
- The different peak temperature for different package volume / thickness is listed as following table:

Table 14-3 Pb-free Process-Package Classification Reflow Temperature

Package Thickness	Volume < 350 mm3	Volume 350 – 2000 mm3	Volume > 2000
＜1.6 mm	260 +0 /-5℃	260 +0/-5 ℃	260 +0 /-5℃
1.6 – 2.5 mm	260 +0 /-5℃	250 +0/-5 ℃	245 +0/-5 ℃
≧ 2.5 mm	250 +0 /-5℃	245 +0/-5 ℃	245 +0/-5 ℃

- Reflow Condition Recommendation For SMT Process
  - In SMT process, the reflow temperature profile for manufacturing should be recommended by solder paste supplier, and the peak temperature should not be higher than the lowest peak temperature used for the MSL classification for the components on board.
  - The reflow temperature profile defined for MSL classification in J-STD-020 is not recommended to be used for real SMT process unless approved by solder paste supplier. Basically, the reflow profile used for MSL

classification is for classification only and regardless of the solder paste itself. Thus the temperature profile is only to “simulate” the reflow process in real case, but not a recommendation for that. The real case still depends on solder paste itself.

- Reflow soldering operations are recommended not to exceed 3 times.

Revision History

Date	Version	Description	Modified by
2025-07-14	R00	Initial release	Ziliang_Yan, Joey_Wang
2025-09-02	R01	Update Cap Touch Controller (CTC)	Xiaohui_Yang