RTL8721Fx Hardware Design Guide

This document provides the Hardware design guide and notes

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document provides the Hardware design guide and notes for the RTL8721Fx.
Please refer to RTL8721FA_RTL8721FC_RTL8721FL_PCB_Layout_and_Assembly_Guide.pdf for layout

2 Power supplement

2.1 Power Structure

Single external power supply is required for the RTL8721Fx. All the other required voltages can be converted and output by two embedded low-dropout regulators (LDO) and one embedded DC-DC switching regulator (DCDC). Embedded LDO and DC-DC have voltage-scaling function, which can effectively reduce power consumption. It is suggested to use embedded LDO and DC-DC powering RTL8721Fx.

Active mode:

- The DCDC outputs typical 1.25V or 1.35V for RF circuits and LDO core (LDOC) input.
- The LDOC outputs typical 0.9V or 1.0V for digital core circuits.0.9V or 1.0V is based on CPU frequency setting.
- The LDO memory (LDOM) outputs typical 1.8V for optional embedded PSRAM based on different part numbers. LDOM_ OUT only has output pin in specific part numbers. When there is a LDOM_OUT output pin, a capacitor of at least 4.7uF is required near the pin for LDO voltage stabilization

Sleep mode:

- The DCDC outputs typical 0.7V or 0.8V for RF circuits and LDO core (LDOC) input.
- The LDOC outputs typical 0.7V or 0.8V for digital core circuits.
- The LDO memory (LDOM) can output typical 1.8V or be shutdown based on configuration for different usage scenarios.

Deep-sleep mode:

- DCDC, LDOC and LDOM are all shut down.

VDH_IO contains up to three separate power pins VDH_IO0, VDH_IO1 and VDH_IO2 for different IOs. Specific power supply relationships can be found in pinmux table. VDH_ IO0 and VDH_ IO1 can independently select the power supply voltage without exceeding the external power supply voltage. Generally, if 1.8V power supply is required, the 1.8V power supply output from LDOM can be selected.

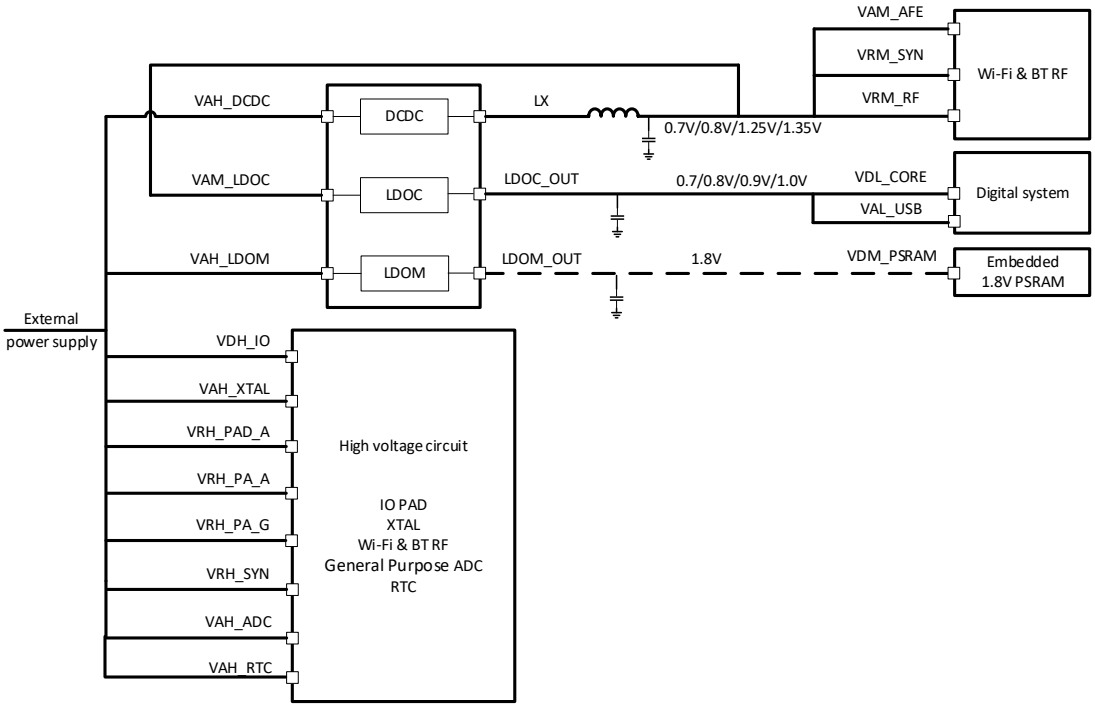

Figure 2-1 Power structure diagram

2.2 Capacitors and Inductance for Power Pins

Generally, for DCDC or LDO regulator's input and output, and RF PA power pins, large capacitor should be placed. For other pins, 0.1uF capacitor is needed.

2.2.1 LDOM

- For package QFN48/QFN68, pin2 has different definition for different IC part number. Please refer to datasheet for more details.
- Taking QFN48 SCH for example, C11/C10 is for LDOM input and output. Capacitor 4.7uF is recommended. If pin2 function is GPIO PA0 for certain part number, C10 can be removed directly.

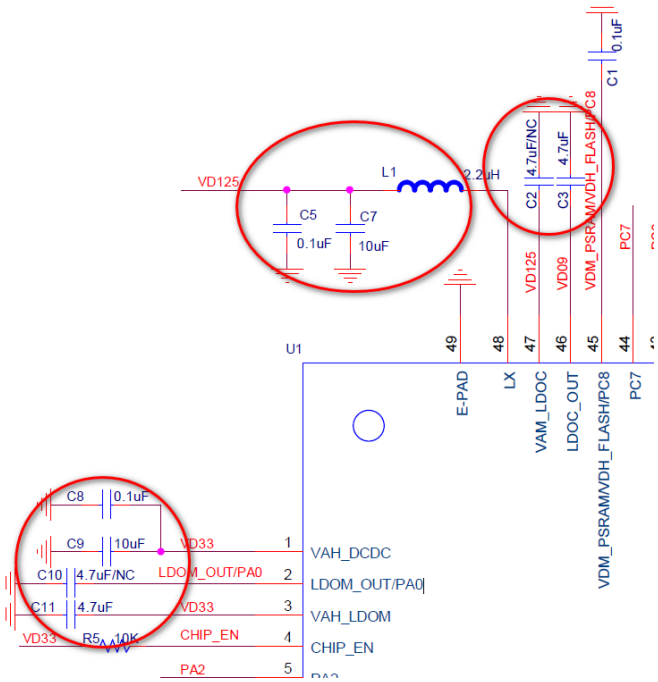

Figure 2-2 LDO and DCDC schematic

2.2.2 LDOC

- C2/C3 is for LDOC input and output, capacitor 4.7uF is recommended.
- Generally, the layout trace length from DCDC output to LDOC input is short enough, which means C5&C7 are close to PIN47, C2 can be un-installed for lower BOM cost. C2 should be reserved in schematic.

2.2.3 DCDC

- C8/C9, C5/C7 are for DCDC input and output, capacitor 0.1uF+10uF is recommended.
- L1 is power inductor for DCDC regulator. The inductor specifications recommended are as follows.

Inductance (uH)	Tol. (%)	Saturation Current, ⊿ L=30%(mA)	Temperature Current, ⊿ T=40℃(mA)	Rdc(Ω) typ.
2.2	20	>= 1100	>= 1100	0.1

2.2.4 RF PA Pins

- C23 is for 5G PA, C21 is for 2.4G PA and C19 is for BT PA. Capacitor 2.2uF or larger is recommended.

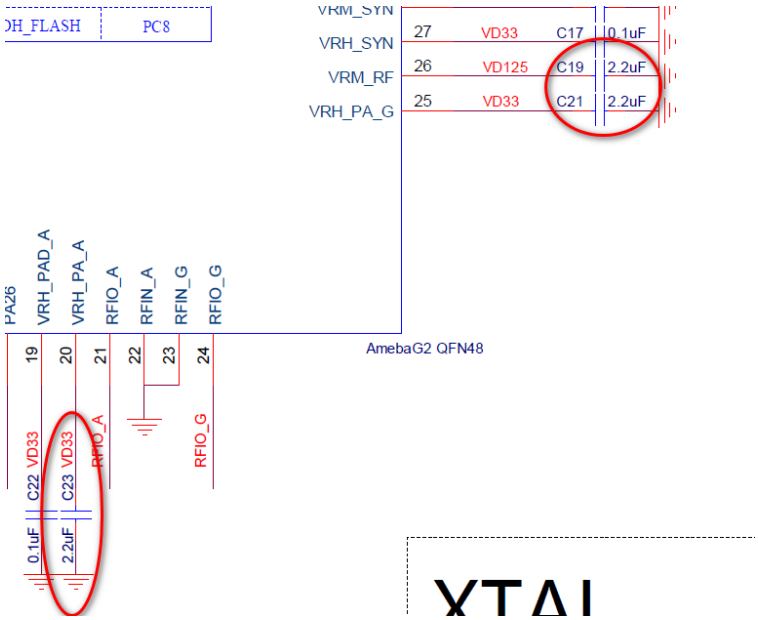

Figure 2-3 RF PIN decap capacitors

2.3 Embedded Regulators Characteristics

The characteristics of embedded regulators including LDOC, DCDC, and LDOM are guaranteed by design.

Table 2-1 Embedded regulators characteristics

Regulators	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LDOC	VIN	Input voltage range	LDO mode	1.20	1.25/1.35	1.45	V
			Bypass mode	0.6	0.7	0.9	
	VOUT	Output voltage range	LDO mode	0.81	0.9/1.0	1.05	V
	$V_{OUT-RIPPLE}$	Output voltage ripple	LDO mode			+/-50	mV
DCDC	VIN	Input voltage range		2.97	3.3	3.63	V
	VOUT	Output voltage range		0.6	1.25/.1.35	1.45	V
	F	Switching frequency	PWM mode	-	2	-	MHz
	$V_{OUT-RIPPLE}$	Output voltage ripple	PWM mode			+/-30	mV
		Output voltage ripple	PFM mode			+/-62.5	mV
LDOM	VIN	Input voltage range		2.97	3.3	3.63	V
	VOUT	Output voltage range		1.7	1.8	1.9	V
	$V_{OUT-RIPPLE}$	Output voltage ripple				+/-50	mV

2.4 External Voltage Regulator Module Recommendation

VXH[1] is the main power supply for Wi-Fi, BT, USB, embedded DC-DC switching regulators, etc. Recommended specification for external VRM is listed in Table 2-2.

- The output voltage of external voltage regulator module can be from 2.97 to 3.63V. Output voltage noise is included in output voltage range.
- The stability of the output power supply is important for RTL8721Fx. Suggested output voltage ripple should be under +/- 100mV. Output voltage ripple should be considered in all possible working states such as WIFI initialization, WIFI TRX, etc. If the VXH is shared with other high power consuming circuits, such as audio amplifiers, IR circuits, etc., output voltage ripple also needs to be under +/- 100mV during the operation of these circuits.
- Continuous output current should be higher than 1 A, which excluding power consumption in circuits other than RTL8721Fx.
- Suggested output voltage rise time is from 0.1 to 3ms, more specific power sequence can be found in datasheet.

Table 2-2 External VRM recommended specification

Symbol	Parameter	Operation conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	Including $V_{OUT-RIPPLE}$	2.97	3.3	3.63	V
$V_{OUT-RIPPLE}$	Output voltage ripple	Including all possible operation conditions[1]			100	mV
I_{OUT}	Continuous output current	Excluding power consumption in circuits other than RTL8721Fx	1			A
T_{RISE}[2]	Output voltage rise time		0.1		3	ms

[1] VXH *refers to power supply including VAH_LDOM, VDH_IO1, VDH_IO2, VDH_IO3, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VAH_ADC, VDH_RTC and VAH_DCDC.*

3 CHIP_EN Pin

CHIP_EN is the enable pin of the whole chip, which can be used to reset the chip. CHIP_EN pin can be pull high with a 10K resistor by default.

If the chip needs to be reset through CHIP_EN pin, it is necessary to ensure that the CHIP_EN is pulled down by at least 0.1ms. For more specific sequences, please refer to the datasheet chapter Power Sequence.

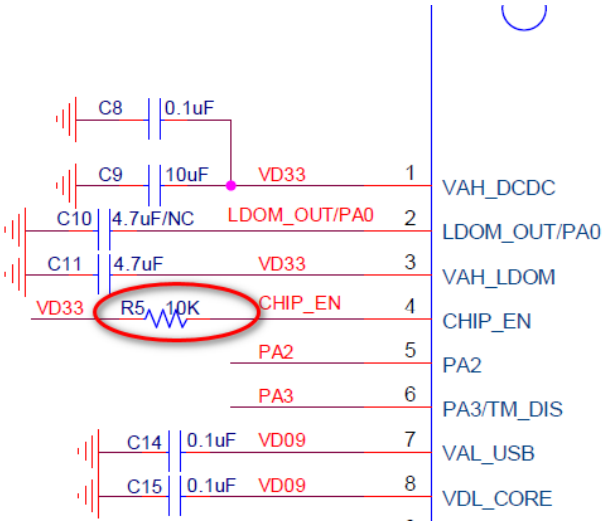

Figure 3-1 CHIP_EN pull-up resistor

4 Crystal Characteristics

The chip has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.

Please connect crystal XI/XO to main IC directly. There is no need to add extra capacitors on net XI/XO.

The characteristic requirements of external crystal are listed in Table 4-1 .

Table 4-1 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

5 RTC Reference Design

The RTC can keep working independently when other power supply pins in the system are powered off, and the VAH_RTC power supply pin is powered by a capacitor for short time (the accuracy of the RTC is not guaranteed in this process). The reference design circuit is as follows:

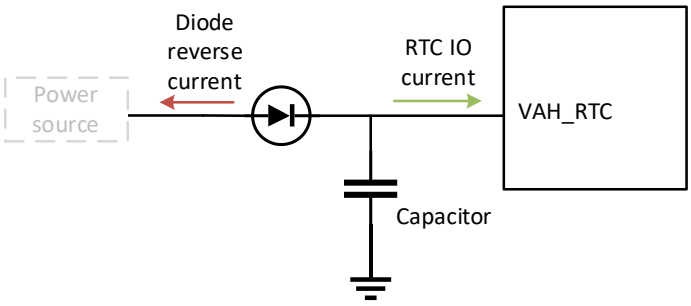

Figure 5-1 RTC reference design for independent work

The above circuit has the following points to note:
1. The minimum voltage on the VAH_RTC pin is not lower than 1.3V.
2. The function of the diode is to prevent the capacitor from being reversely drained by the shutdown power source when the RTC works alone to draw power from the energy storage capacitor.
3. The diode needs to ensure the smallest possible forward voltage drop and the smallest possible reverse leakage current.
4. The capacity of the energy storage capacitor needs to be appropriately selected based on the actual duration that the RTC needs to work alone[1].

NOTE

[1]: The capacitor value needs to be calculated based on the following parameters:
1. The time of the module working alone.
2. The ambient temperature when working alone.
3. The reverse leakage current of the diode at this ambient temperature.
4. Power consumption of the RTC IO at this ambient temperature.

Please refer to the following table for high and low temperature power consumption data when the RTC IO circuit works alone:

Figure 5-2 RTC independent working current consumption

VAH_RTC/V	Typical RTC IO current @ -40 degrees/uA	Typical RTC IO current @ 25 degrees/uA	Typical RTC IO current @ 85 degrees/uA

NOTE

Only some part numbers have VAH_RTC pin, and corresponding RTC can work inpendently.

6 I/O Pins Characteristics

6.1 Features

The following electrical properties are configurable for standard I/O pins:

- Function ID
- Internal Pull-up/Pull-down Resistor
- Driving strength
- Slew rate control
- Schmitt trigger
- Shutdown & RESET
- Open drain mode

6.2 Functional description

The I/O diagram is given in Figure 6-1. There are many kinds of I/Os in RTL8721Fx, different I/Os have different configurations.

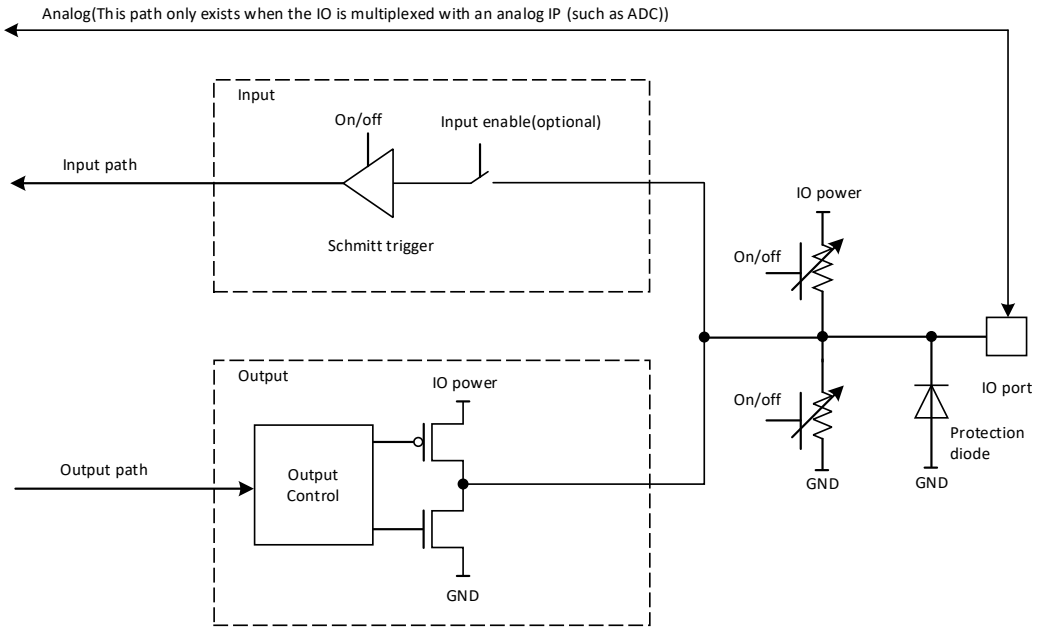

Figure 6-1 I/O diagram

6.2.1 I/O Types

All I/Os are listed in Table 6-1. The Human Body Model (HBM) of all IOs are above 3.5KV.

Table 6-1 I/O Types

Pin name	I/O power pin	Driving Strength(mA)[1]		Internal pull resistor (ohm)[2]		
		I/O power = 1.8V (±10%)	I/O power = 3.3V (±10%)	Min.	Typ.	Max.
PA0-PA1	VAH_LDOM[3]	-	4/8		4.7K/50K[4]	
PA2-PA3	VAH_LDOM	-	8/16		80K	
PA4-PA11	VDH_IO0	1/2/3/4	3/6/9/12		50K	
PA12-PA17	VDH_IO0	2/4	4/8		80K	
PA18-PA21, PA25-PA28	VDH_IO0/VDH_IO1[5]				50K	
PA22-PA24	VDH_IO0/VDH_IO1	2/4	4/8		80K	
PA29-PA31, PB0-PB1	VDH_IO0/VDH_IO1	2/4	4/8		4.7K/50K	
PB2	VDH_IO0/VDH_IO1	4/8	8/16		4.7K/50K	
PB3-PB7	VDH_IO2[3]	-	8/16		4.7K/50K	
PB8-PB31, PC0-PC1	VDH_IO2	-	4/8		4.7K/50K	
PC2-PC7	VDH_IO2	-	3/6/9/12		50K	
PC8	VDH_IO2	-	4/8		50K	

NOTE

1. *The driving capability is related to the I/O power.*
2. *The pull up and pull down values of other IOs in the table are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The variation range at different PVT is ±50% of typical value. Refer to datasheet for detailed values.*
3. *The supply voltage of VAH_LDOM and VDH_IO2 can only be 3.3V.*
4. *These IOs have two types of pull-up and pull-down resistors.*
5. *The IO power pins of these IOs are different for different packages. Please refer to the PINMUX document for details. All groups support both 3.3V and 1.8V I/O power.*

6.2.2 IO CTRL Register

Each I/O pin has one IOCTRL register assigned to control the pin's electrical characteristics.

Table 6-2 IOCTRL register

Bit	Access	Initial value	Symbol	Description
[15]	R/W	0h	gpio@_dis	GPIO shutdown, only when the gpio@_dis signals of this group of GPIOs are all 1, the group of GPIOs will be shutdown. 1. disable 0. enable
[14]	R/W	0h	gpio@_e3[1]	GPIO driving strength control reg2. 0: low 1: high
[13]	R/W	0h	gpio@_sr[2]	GPIO slew rate control. 0: fast slew rate 1: low slew rate
[12]	R/W	1h	gpio@_smt	GPIO Schmitt control
[11]	R/W	1h	gpio@_e2	GPIO driving strength control reg1. 0: low 1: high
[10]	R/W	0h	gpio@_pupdc[3]	Some IO may have two types of PU/PD resistors, this bit can select it. 1: small resistor 0: big resistor
[8]	R/W	1h	gpio@_ie[4]	GPIO input enable control.
[4:0]	R/W/ES	0h	gpio@_sel	GPIO PINMUX function id select

1. *This bit is valid only for PA4-PA11, PA18-PA21 and PC2-PC7.*
2. *This bit is valid except for PA4-PA11, PA18-PA21 and PC2-PC7.*
3. *This bit is valid only for PA0-PA1, PA29-PA31, PB0-PB31, PC0-PC31 and PC8.*
4. *This bit is only valid for PA4-PA5, PA12-PA24.*

Internal pull up and pull down resistors of I/Os are controlled by separate registers. The 32 bits of each register control the status of 32 IOs respectively.

6.2.3 Function ID

Each IO port can be connected to a different function by configuring the function ID, refer to the PINMUX documentation for details.

6.2.4 I/O Pull up/down Resistor Control

Each IO has independent pull-up and pull-down resistors inside, and has the following features:

1. IO can be configured as pull-up, pull-down or no-pull.
2. The pull-up and pull-down resistors of different IOs may be different.
3. Some IOs have multiple pull-up and pull-down resistor levels, users can change it through gpio@_pupdc.
4. The internal pull-up and pull-down resistors will change with the IO power.
5. The pull-up and pull-down states in active and sleep/deep sleep states can be configured through the pinmap document.

Please refer to the datasheet and the pinmap document in Chapter 6.3 for more detailed information.

6.2.4.1 Test methods

Pull-up and Pull-down resistor's value is different between different I/Os. The resistor value is changed by controlling the gpio@_pupdc of register table (Table 6-2). For I/Os with only one resistance value, gpio@_pupdc is not valid.

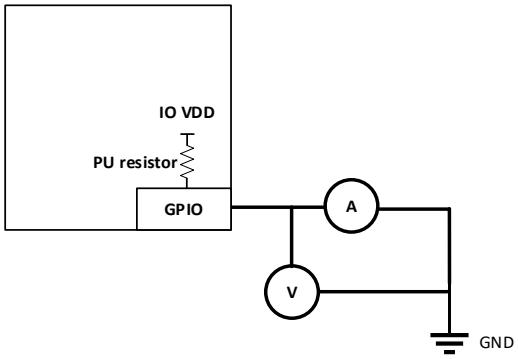

Figure 6-2 I/O Pull up resistor test

I/O pull-up resistor test procedure:

(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 1 for gpio@_pu and 0 for gpio@_pd.
(3) For GPIOs with multiple pull-up resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is V_1.
(5) According to Figure 6-2, only connect the ammeter to test. At this time, the current value is I_1, and the pull-up resistor is $R_{pu}=V_1/I_1$.

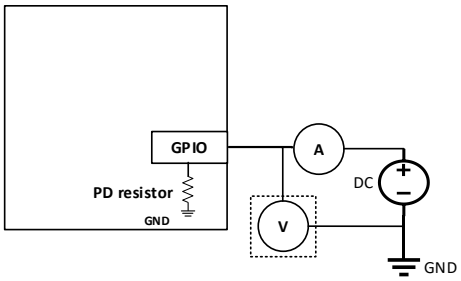

Figure 6-3 I/O Pull down resistor test

I/O pull-down resistor test procedure:

(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 0 for gpio@_pu and 1 for gpio@_pd.
(3) For GPIOs with multiple pull-down resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is 0V.
(5) According to Figure 6-3, use an external power supply to provide the same voltage (V_2) as the GPIO power, and measure the current (I_2) at this time, and the pull-up resistor is $R_{pd}=V_2/I_2$.

6.2.5 I/O Driving Strength

The I/O driving strength can be configured through gpio@_e2 and gpio@_e3 in the IOCTRL register. I/O driving strength is different between different I/O types.

6.2.5.1 Test methods

IO source current test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.85*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2 & gpio@_e3.
(4) I_{SOURCE} is the driving strength of GPIO output high.

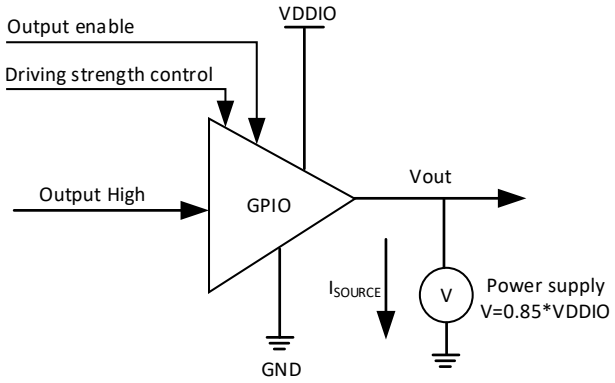

Figure 6-4 Source current test of I/O

IO sink current test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.15*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2.
(4) I_{SINK} is the driving strength of GPIO output Low.

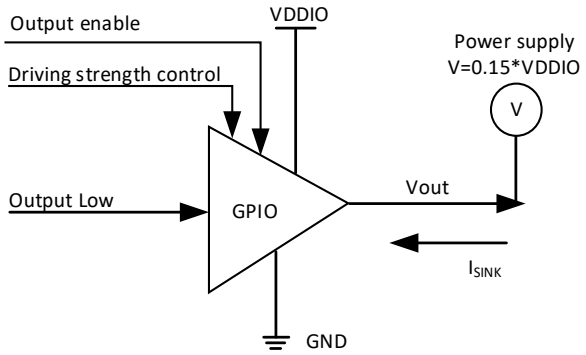

Figure 6-5 Sink current test of I/O

6.2.6 I/O Schmitt Trigger

The I/O pin contains a Schmitt trigger as a digital function, which can be selectively disabled by setting gpio@_smt in the IOCTRL register.

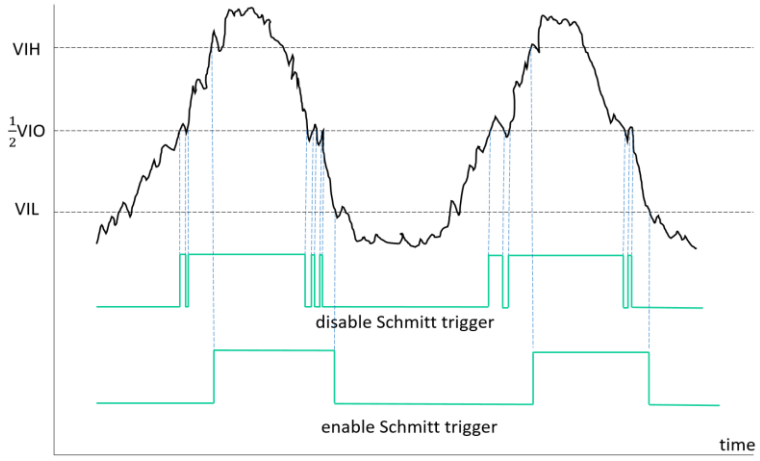

Figure 6-6 The voltage seen by GPIO when Schmitt trigger is enabled or disabled

The specifications of the Schmitt trigger are shown in Table 6-3.

Table 6-3 Digital IO pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIL	IO input low level voltage	V_{IO}=1.8V±10%	-0.3	-	0.35*V_{IO}	V

		V_{IO} =3.3V±10%	-0.3	-	0.8	
VIH	IO input high level voltage	V_{IO}=1.8V±10%	0.65* V_{IO}	-	-	
		V_{IO}=3.3V±10%	2	-	-	

NOTE

- *V_{IO} is the power supply for IO pin.*
- *If the Schmitt trigger is disabled in IOCTRL register, VIH=VIL=0.5*VIO.*

6.2.7 Slew Rate Control

Most IOs have a slew rate control function to adjust the rising or falling slope. For specific IO names and typical rising/falling times at different slew rates, please refer to the datasheet.
Please note that all functions only guarantee the timing performance under the default slew rate setting. If you modify the slew rate setting at will, high-speed functions may not work properly. Please refer to different interface timing data for setting recommendations.

6.2.8 I/O Shutdown & RESET

The power of I/O can be shut down through the GROUP_X_SHDN bit in the PADCTRL register. You can use this function to conserve power.

- When GROUP_X_SHDN is configured, the state of I/O pull resistor will maintain the state before configuration. At this time, the change of the I/O pull-up/pull-down register will not change the state of the I/O pull resistor.
- When GROUP_X_RSTB is set to 0, the state of this group of I/O pull resistors will change to no pull. At this time, the change of the I/O pull-up/pull-down register will not change the state of the I/O pull resistor.

6.2.9 Open Drain Mode

The default output mode of all I/Os is push-pull and can be configured as open-drain only when used as GPIO functions. For more details, please refer to the software APIs.

6.3 I/O Pins Internal Pull Resistor Control Configuration

Each I/O has an Internal Pull-up and Pull-down Resistor. Please refer to section 6.2 for details. This section describes how to configure it.
During the process of boot, sleep and deep-sleep, I/O pull control is needed, and the chip will load the I/O internal pull status of each I/O from the “pinmapcfg.c” file.
The correct configuration of pinmap can achieve low power consumption. Otherwise, the unsuitable configuration may lead to leakage.
Principles for I/O internal control configuration:

1. If the I/O is not used, it is recommended to set it to pull down.
2. If I/O is used as input, it cannot be left floating. Please refer to the following chapters for configuration of different functions.
3. If I/O is used as output, please refer to the following chapters for configuration of different functions.

In the SDK, customers should set the internal pull status of I/O according to the above rules.
In the “pinmapcfg.c” file, PMAP_TypeDef pmap_func[] should be configured. In which,

- Pin Name: indicates the I/O.
- Func PU/PD: is used to configure the I/O internal pull status when the IC is in active mode.
- Slp PU/PD: is used to configure the I/O internal pull status when the IC is in sleep mode.

The following configuration is only applicable to RTK EVB, and customers need to configure it according to the external circuit.

```
const PMAP_TypeDef pmap_func[] = {
//Pin Name          Func PU/PD                  Slp PU/PD
    {_PA_0,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_1,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_2,         GPIO_PuPd_UP,           GPIO_PuPd_UP},          //
    {_PA_3,         GPIO_PuPd_UP,           GPIO_PuPd_UP},          //
    {_PA_4,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_5,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_6,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_7,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_8,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_9,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_10,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_12,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
```

```
{_PA_13,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_14,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_15,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_16,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_17,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_18,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_19,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_20,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_21,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_22,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_23,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_24,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_25,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_26,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_27,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_28,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_29,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_30,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PA_31,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_0,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_1,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_2,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_3,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_4,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_5,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_6,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_7,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_8,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_9,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_10,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_12,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_13,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_14,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_15,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_16,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_17,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_18,        GPIO_PuPd_UP,           GPIO_PuPd_UP},          //
{_PB_19,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
{_PB_20,        GPIO_PuPd_UP,           GPIO_PuPd_UP},          //log_TX sleep need pull up
{_PB_21,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_22,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_23,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_24,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_25,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_26,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_27,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_28,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_29,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_30,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PB_31,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_0,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_1,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_2,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_3,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_4,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_5,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_6,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_7,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_8,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_9,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PC_10,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PC_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
```

```
    {_PC_12,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_13,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_14,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_15,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_16,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_17,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_18,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_19,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_20,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_21,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_22,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_23,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_24,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_25,        GPIO_PuPd_UP,           GPIO_PuPd_UP},
    {_PC_26,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_27,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_28,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PC_29,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
    {_PNC,          GPIO_PuPd_KEEP,         GPIO_PuPd_KEEP},        //table end
};
```

There are four states of the I/O.

- GPIO_PuPd_UP: Indicates that the I/O is through the internal resistor pulled up to VDDIO.
- GPIO_PuPd_DOWN: Indicates that the I/O is through the internal resistor pulled down to GND.
- GPIO_PuPd_NOPULL: Indicates that the I/O is in High-Z.
- GPIO_PuPd_KEEP: Indicates that the I/O will maintain the last status.

The following section illustrates the recommendation of I/O status configurations according to the function of different pins.

6.3.1 Normal GPIO

When a pin is used as a normal GPIO connecting with external circuit, the GPIO PU/PD status depends on the state of the external circuit. If the GPIO is used to driver LED, and pin status is 'External pull up', the GPIO status need to be 'PULL UP' in sleep and DSLP mode. Configure the state of the internal PU/PD according to the GPIO external circuits.

Table 6-4 Normal GPIO status

I/O type	Pin status	Active PU/PD	Sleep PU/PD
Input	External Pull UP	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP / GPIO_PuPd_NOPULL
Input	External Pull Down	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL
Input	Floating	GPIO_PuPd_DOWN	GPIO_PuPd_DOWN
Output	Output High	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP
Output	Output Low	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN

6.3.2 LOGUART

The pins PA2 and PB20 are LOGUART function by default. The I/O status are listed in Table 6-5.

Table 6-5 LOGUART I/O status

Pin function	Pin name	Func PU/PD	Sleep PU/PD
UART_LOG_RXD	PA2	GPIO_PuPd_UP	GPIO_PuPd_KEEP
UART_LOG_TXD	PB20	GPIO_PuPd_UP	GPIO_PuPd_KEEP

6.3.3 ADC & Cap-touch

For PA12~PA24, if customer need to configure it for ADC or cap-touch function, customers need to configure IE to 0 first (please refer to Table 6-2), and pinmapcfg configure to no pull.
If the customer needs to configure other functions, IE needs to be set to 1. For other configurations, please refer to 6.3.1.

6.3.4 SWD

The pins PA30 and PA31 are SWD function by default. The I/O status are listed in Table 6-6.

Table 6-6 SWD I/O status

Pin function	Pin name	Func PU/PD	Sleep PU/PD
SWD_DATA	PA18	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SWD_CLK	PA19	GPIO_PuPd_UP	GPIO_PuPd_KEEP

NOTE

PA18&PA19 is the SWD function by default. If they need to be used as GPIOs or other functions, Please set 0x4080A9F4[0] = 0 first, and then configure these two pins to other function IDs.

6.3.5 Flash Pin

When a pin is configured as SPI_FLASH function, the I/O status is listed in Table 6-7.

Table 6-7 Flash I/O status

Pin function	Func PU/PD	Slp PU/PD
SPI_DATA_X	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CS	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CLK	GPIO_PuPd_DOWN	GPIO_PuPd_KEEP

6.4 I/O Pins Output

6.4.1 IO pin Output Configuration

When setting the IO to output status, you need to perform the configuration according to the following steps:

1. Set IO as GPIO function.
2. Write 1/0 to the output value register of this GPIO.
3. Set the GPIO to output mode.

If the user sets the I/O to output mode without setting the output 1 or 0 first, the I/O will output 0 first, which may cause temporary abnormalities in the application (such as LED lights flashing due to incorrect I/O output status).

6.4.2 IO pin PU&PD during Sleep and Deep-sleep status

Each IO has independent PU and PD configuration registers under sleep and deep-sleep. When the chip enters sleep and deep-sleep states, the corresponding register settings will be automatically loaded. Users can modify the pinmap_configure document in the SDK according to actual application requirements.

6.4.3 IO pin Output during Sleep and Deep-sleep status

After the system enters sleep mode (PG or CG), the status of the I/O output will maintain the status before sleep. For example, before sleep, the I/O is set to output 1. After the system enters PG or CG, this I/O will still remain output 1 unchanged.
However, if the system enters deep sleep, the status of the I/O output set under active will become invalid. For example, if the I/O in active is set to output 1, and the system enters deep sleep, the I/O will not be able to maintain the output 1 state.

7 PINMUX Instructions

7.1 Introduction

RTL8721Fx provides a PINMUX circuit to maximize the user's freedom of use under limited pin-out conditions. Each pin can be connected to different internal IP circuits through configuration. For the specific correspondence between each pin and IP circuit, refer to the provided

PINMUX document.
Before users apply the chip for further development, please read the following precautions about PINMUX to avoid inconvenience due to unexpected behavior.

7.2 Trap Pins

When users power on the chip, the internal circuit will latch several pins conditions to decide whether enter into different mode. The trap pins and their descriptions are as below.

Table 7-1 Trap pin description and precautions

Pin name	Trap pin name	Active level[2]	Descriptions	Note
PA3	TM_DIS[1]	Low	Enter test mode during power on procedure. (Internal use)	1: Normal mode 0: Test mode
PB18	BOOT_NOR[3]	-	Select the flash type used by the chip to store boot files.	0:NAND FLASH 1:NOR FLASH
PB20	UD_DIS	Low	Enter flash download mode during power on procedure.	Download flash content in this mode through LOGUART. 1: Normal mode, 0: UART download mode.

NOTE

The chip will only latch the trap pin value once during the power-on process. After power-on is completed, the trap pin can be used as a normal IO.

CAUTION

1. ***Please make sure that the pin is in the pull-up state during normal use. In addition, if the IO will be connected to other devices during design, please check the power-on timing and the behavior of the docking device to ensure that the IO level remains high during the chip power-on process.***
2. *If there is an external pull-up circuit for the trap pin, make sure the power connected to the pull-up circuit is consistent with the IO power of the trap pin.*
3. *Only valid for RTL8721FxM (embedded PSRAM). All the other part numbers only support NOR flash and always treat flash as NOR flash no matter PB18's state during power on.*

7.3 Wake Pins

PA0, PA1, PA2 and PA3 are directly connected to the wake up circuit which is used to wake up system from deep-sleep state. When users need to use other functions on this pin, please disable the wake up function.

7.4 Function Mux

7.4.1 Function ID 0-16

For functions whose ID number among 0-16, each pin can only be connected to a fixed signal of a certain IP. The functions that can be configured on each pin are very limited, but a dedicated design can maximize the performance of each IP.

NOTE

For example, function id 9 and function id 75-78 are both SPI functions. Since function id 9 is a dedicated pin, the maximum speed of the SPI function reaches 50MHz (Master mode). And the maximum speed of the pins (full-cross pins) corresponding to function id 75-78 is only 25MHz(Master mode).

Take PB31 as an example. If users configure function ID of PB31 to 10, then the pin will be directly connected to the SPI1_MISO signal of the SPI1 IP via PINMUX. Please refer to the PINMUX document for the specific function distribution available on each pin.

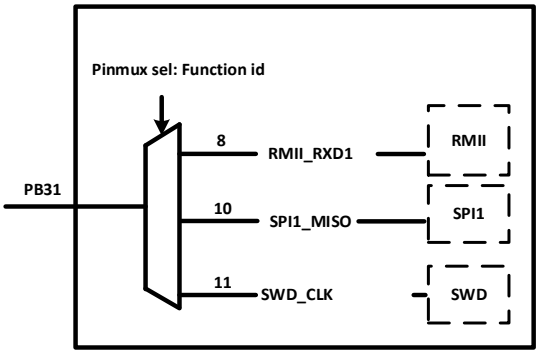

Figure 7-1 Schematic diagram of PINMUX connection of PB31

7.4.2 Function ID 32-155

For functions whose ID number is after 32, each pin can be connected to different signals of a certain IP. This method maximizes the freedom of use, but the scope of use and some IPs' performance (max transfer speed) is limited.

NOTE

These function IDs can be configured in PA0-PA31, PB0-PB31 and PC0-PC8.

Take PA4 as an example. According to the PINMUX document, users can connect PA4 with the I2S0_BCLK signal of I2S0 by configuring the PA4 function ID as 32. Users can also configure the PA4 function ID as 132 and connect PA4 with the IR_TX signal of IR. For details, please refer to the PINMUX documents.

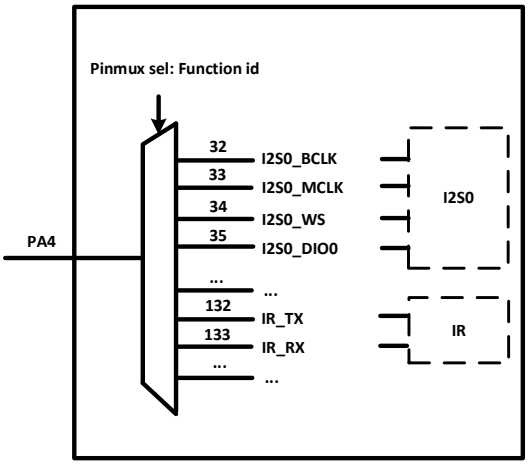

Figure 7-2 Schematic diagram of PINMUX connection of PA4

7.5 PINMUX Signal Descriptions

For all signal descriptions, please refer to PINMUX documents for detailed information.

8 General Purpose ADC

The General purpose ADC (GP-ADC) and Capacitive Touch Sensor multiplexes pin. The signal sampling of Capacitive Touch Sensor itself is also done through GP-ADC, and both of them are sensitive analog signal sensors, so we need to pay special attention to interference.

8.1 Avoidance of interference from adjacent signals

GP-ADC has multiple channels that use a set of fixed pins of IC. Care should be taken to avoid using GPIO in the same group of GP-ADC as high-speed signal ports (I2C, SPI, etc.), as shown in **错误!未找到引用源。**. If unavoidable, it is necessary to set it reasonably on the software to ensure that the high-speed signal has no action while GP-ADC sampling.

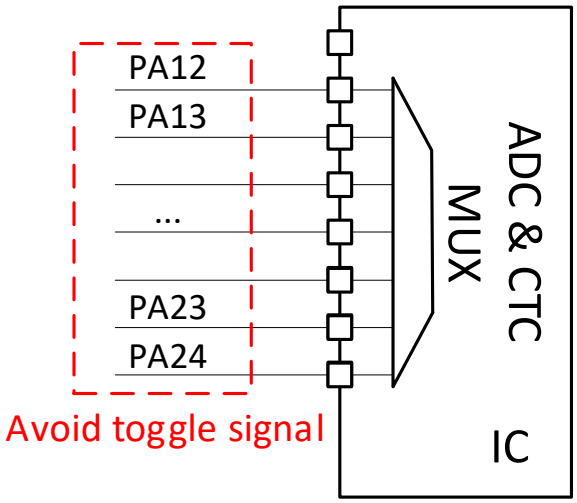

Figure 8-1 GP-ADC net arrangement

In addition, even if the high-speed signal is not arranged in the same set of the GP-ADC GPIO, it should not be arranged adjacent to the pin of the GP-ADC.

8.2 Input impedance

In order to measure the voltage of 0 to 3.3V, a voltage divider is added to the front end of the GP-ADC. The resistance is fixed and cannot be modified, and the accurate resistance value can be obtained by reading the calibration value written in each IC.

Due to the divider resistor, the input resistance of the GP-ADC will be affected by it, and the typical value is 491kohm. It is necessary to pay attention to this situation in application. Take **错误!未找到引用源。** as an example, when the external resistance R2 of GP-ADC is about equal to the internal resistance R, there will be a deviation in the voltage collected by GP-ADC. If R2 is a thermistor, the temperature measurement may be inaccurate.
Therefore, when designing the external circuits, we should consider:
(1) R2 should be sufficiently small (less than 1 / 100 of R) to minimize the impact of internal resistance.
(2) If the requirements (1) cannot be met, the Rin value of the IC can be obtained through the API and incorporated into the circuit design.

Typically GP-ADC normal channel are used to measure the voltage of different sensor, such as NTC thermistor. The simplified block is as follows:

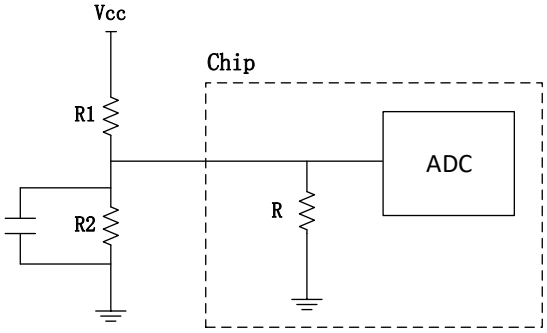

Figure 8-2 simplified application block

There is a 500 kohm resistor to ground inside the chip which will affect the accuracy of GP-ADC with the combination of peripheral circuit. The ideal input voltage to GP-ADC is:

$$V_{\text{ideal}} = V_{\text{cc}} \times R_2 / (R_1 + R_2) = 3.3 \times \frac{R_2}{R_1 + R_2}$$

But the actual input voltage to GP-ADC is:

$$V_{\text{actual}} = V_{\text{cc}} \times \frac{R_2 // R}{R_2 // R + R1} = V_{cc} \times \frac{R_2}{R_2 + R_1 \times R_2 / R + R_1}$$

Compare the two formals, V_{actual} is smaller than V_{ideal} due to the impact of internal R. And the greater the ratio of R1xR2/R is, the greater the error between V_{actual} and V_{ideal} is. What's more, the resistance of internal R vary differently in multi chips which also can impact the accuracy. For better accuracy, internal R should be calculated and its resistance value will be stored in OTP.

After calibration, if R2 is NTC thermistor, the actual resistance of R2 is:

$$R_2 = \frac{R_1 \times V_{\text{adc}}}{V_{cc} - V_{adc} - V_{adc} \times \frac{R_1}{R}}$$

By the way, it's optional for customers to choose another GP-ADC channel to measure the voltage of Vcc, which can reduce the impact that Vcc changes while GP-ADC Vref doesn't change:

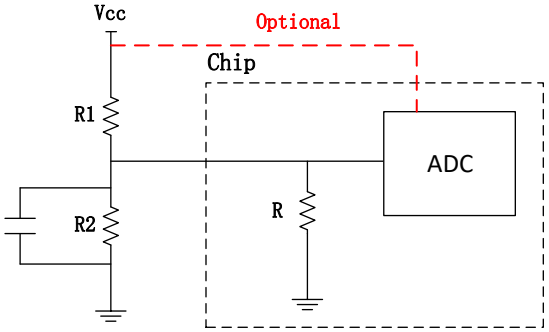

Figure 8-3 Optional application block

(3) R will be connected to the circuit only when the GP-ADC is sampling. Therefore, at the moment when the ADC sampling is turned on, the circuit will be switched, and the parallel C of R2 may slow the transient process of the circuit. There are usually two ways to solve this problem:

a) When the requirement for sampling rate is not high, it can be sampled at intervals, and the interval time needs to exceed the circuit time constant. In this case, the instantaneous value of sampling is the voltage at the beginning of switching, that is, the voltage of the capacitor C. in this case, the circuit design requires that C be greater than 10nF.

b) when the sampling rate is strict and interval sampling is not acceptable, a delay can be added before each sampling of a group of data, which should be greater than 5 times the circuit time constant, and pay attention to clear the conversion result FIFO before reading the data.

9 Capacitive Touch Sensor

9.1 Avoidance of interference from adjacent signals

- It is not recommended to reuse Capacitive Touch Sensor pins with other functions. High-speed signal lines (I2C, SPI, etc.) should not appear in the same group of Capacitive Touch Sensor pins. If unavoidable, it needs to be set reasonably on the software to ensure that Capacitive Touch Sensor works with no high-speed signal action
- It is suggested to keep the Capacitive Touch Sensor away from high speed signal and switching power net
- To prevent crosstalk, if only some Capacitive Touch Sensor channels are used, select channels at intervals and disable unselected channels
- Do not design a pull-up or pull-down voltage on the signal line
- Do not design bypass capacitors on the signal line

NOTE

Capacitive Touch Sensor's layout has a great impact on performance. For specific layout rules, please refer to layout guide.

9.2 Series Resistance

A resistor is connected in series in each Capacitive Touch Sensor channel (placed near the chip). This resistor and the parasitic capacitance on the signal path form a simple RC filter, which can partially filter out the noise interference and improve the ESD resistance. Due to the different circuit design, the resistance usually can not be accurately selected. The filter effect is poor when the resistance is too small, and the sensitivity is reduced because the resistance is too large. It is recommended to choose a resistance of 47-560 ohms.

In addition to using series resistance to improve ESD resistance, the TVS of each sensor channel should be connected in parallel to attenuate the impact of surge current on the sensor, but the junction capacitor of this TVS should not exceed 0.6 pF.

9.3 Button LED Design

When the button is made into a hollowed-out type, a LED can be added in the middle, and the light and darkness of the LED can be used to judge the situation of touching and leaving the finger. It is suggested that the power supply of LED should add RC filter to slow down the change rate of the level edge.

9.4 Max input Voltage

The Capacitive Touch Sensor is an analog circuit, an ADC sample the input net continuously. The max input voltage of the input net is 3.3V. In particular, the use of too large mbias can cause a charging voltage exceeding 3.3V, which may cause damage to the ADC.

10 Flash SPI

10.1 Flash Selection Requirements

- Flash SPI in RTL8721Fx can only operate in typical 3.3V. Users need to select flash with adaptive operating voltage range.
- The compatible flash can be found in Flash AVL. If the expected flash to be used is not in AVL, please contact RTK for more information.

10.2 Schematic Reference Design

- Suggest CS pin reserving a pull up 10K resistor so that the CS pin has a certain high level state to avoid bus floating. If internal pull-up is configured, the external pull-up resistance should be NC
- For dual SPI and standard SPI mode，suggest WS pin and Hold pin reserving an pull up 10K resistor so that the WS pin has a certain high level state to avoid bus floating. If internal pull-up is configured, the external pull-up resistance should be NC
- Vcc requires a filtering capacitor connected to ground, usually one large and one small capacitor connected in parallel, such as 10μF and 0.1μF.

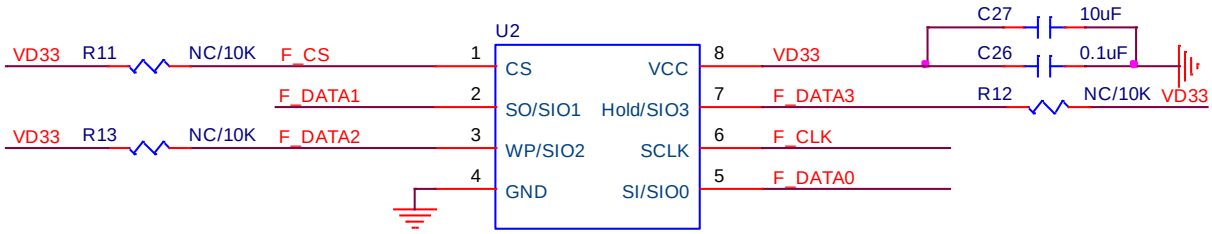

Figure 10-1 SPI flash reference design

11 I2C

11.1 Schematic Reference Design

- Part of the pads used for I2C can switch to 4.7K pull-up resistor internally (PA0, PA1, PA29~PA31, PB0~PB31, PC0, PC1). However, the internal pull-up resistance value of other pads is too large and not suitable for I2C communication. Suggest users to reserve pull-up resistors externally to adjust the resistance value according to their own needs.
- Different speed modes have requirements for the maximum allowable load of the I2C bus. In standard, fast and 1.7M high speed modes, the bus load cannot exceed 400pF, and in 3.4M high speed mode, the bus load cannot exceed 100pF.
- Calculation method for pull-up resistance of I2C bus:
  The voltage value of IO Power determines the minimum value of pull-up resistance. When IO Power is 3.3V, the minimum allowable

value of pull-up resistance is 1K, and when IO power is 1.8V, the minimum allowable value of pull-up resistance is 0.5k. The size of the bus load determines the maximum allowable pull-up resistance, and the calculation formula is as follows:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

In the formula, t_r represents the maximum signal rise time allowed under different speed modes (Standard: 1000ns, Fast: 300ns, High Speed: 40ns), and C_b represents the bus load.

- The I2C protocol also defines resistors Rs connected in series on SDA and SCL lines. The function of this resistor is to effectively suppress interference pulses on the bus from entering the slave device and improve reliability. The selection of this resistor is generally around 100~200Ω. This resistor is not necessary and can be used in harsh noise environments.

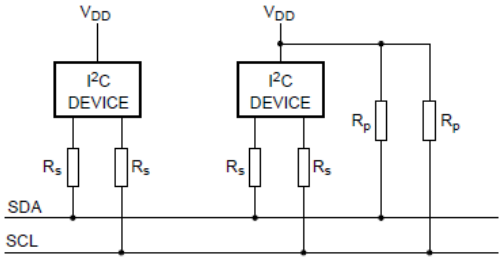

Figure 11-1 I2C schematic reference design

12 SDIO Host

12.1 Schematic reference design

12.1.1 MircoSD

- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be adjusted by users according to their needs, usually between 0~47 Ω. The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value.

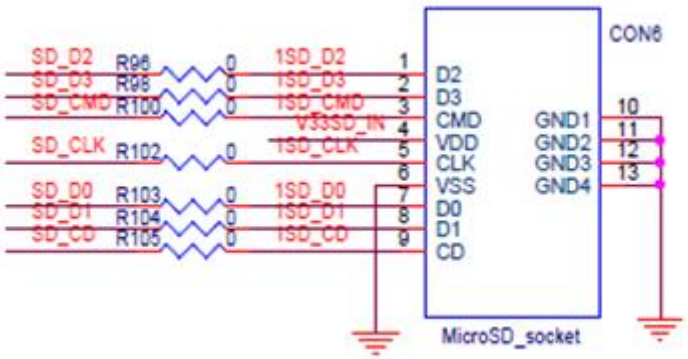

Figure 12-1 MicroSD socket reference design

- Each SD card cable (power and signal lines) needs to be connected to an ESD diode. The selection rules for ESD diodes are as follows:
  - The working voltage V_{RWM} of the ESD diode is greater than the highest operating voltage of the circuit.
  - The parasitic capacitance of the ESD diode is required to be less than 30pF.
  - The breakdown voltage V_{BR} of the ESD diode is greater than the highest operating voltage of the circuit.
  - The clamping voltage Vc should be less than the maximum peak voltage that the protected chip can withstand.

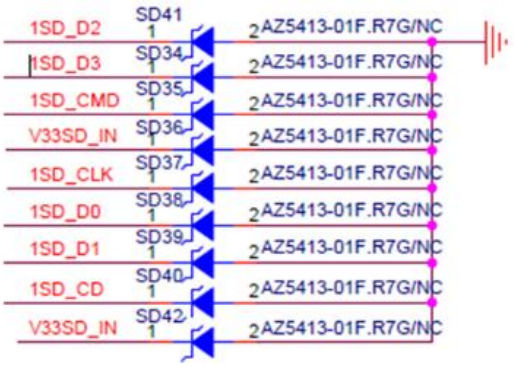

Figure 12-2 ESD diode for SD signals

- The four data cables from D0 to D3, as well as the CMD cable, need to be externally pulled up to IO Power. The pull-up resistance is generally between 10K and 100K.

Figure 12-3 PULL-UP resistors for SD signals

- The VDD of the SD card requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.

12.1.2 EMMC

The schematic design considerations related to external EMMC chips are recommended to refer to the reference design of actual EMMC chips. This section is based on Samsung's EMMC Board Design Guide.

- The VSSQ and VSS pins of the EMMC chip are all grounded, and VCCQ is connected to IO power. VCC is power supply for the internal memory of the EMMC chip.

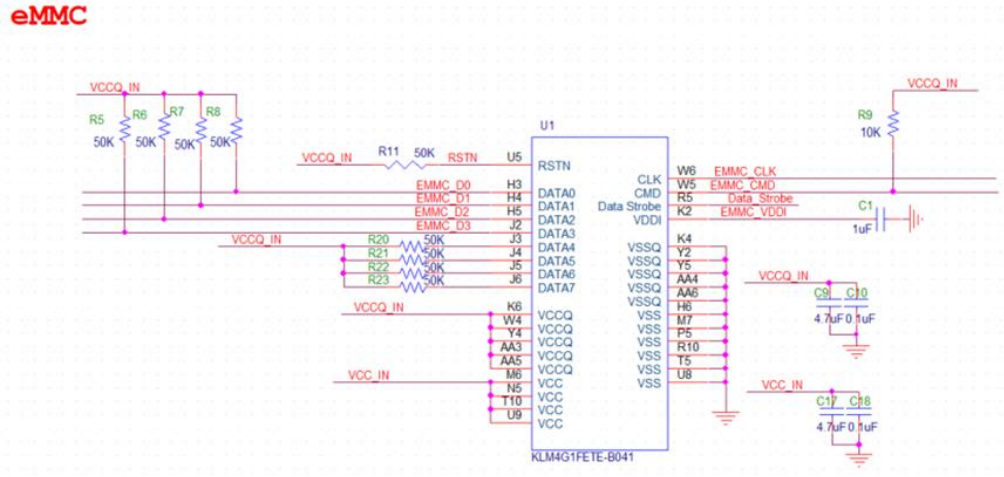

Figure 12-4 EMMC schematic design

- To avoid bus floating, it is recommended to reserve 50K pull-up resistor to VCCQ for the four data pins from Data0 to Data3. Although Data4 to Data7 cannot be used, it is also recommended to reserve 50K pull-up resistor to VCCQ (if the chip end has already done internal pull-up, these pull-up resistors can be removed). CMD pins must be pulled up to VCCQ with 10K resistor.

- For the RSTN pin, since the chip does not use H/W reset, this pin does not need to be connected to the chip side. However, 50KΩ must be pulled up to the RSTN pin, as it must be in a high level state for the EMMC chip to function properly.
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance solder pad at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be selected by customers according to their needs, usually between 0~47 Ω. The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value.
- The VCCQ and VCC of the EMMC chip both need to be connected to the ground with a set of decoupling capacitors, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF. If the VCCQ of EMMC is from the same source as VCC, only one set of decoupling capacitors is needed.
- The VDDI pin needs to be connected to ground with a capacitor to prevent EMI interference and stabilize the output of the internal regulator of the EMMC chip. Suggested capacitance value is 1μF~4.7μF.

If the chip supports DDR400 mode, the data strobe pin requires an external pull-down resistor of 10K~100K. Since our chip does not support DDR400, we cannot use this pin, so we can float it, connect an external pull-up resistor or an external pull-down resistor.

12.1.3 SD NAND

- The four data cables from D0 to D3, as well as the CMD cable, need to be externally pulled up to IO Power. The pull-up resistance is generally between 10K and 100K.
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be adjusted by users according to their needs, usually between 0~47 Ω. The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value.
- The VDD of the SD card requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.

13 SDIO Device

13.1 Schematic Reference Design

- VCC_SDIO requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.
- Suggest users to connect a resistor in series on the clock, cmd, and data lines. The customer can improve signal quality by adjusting the resistance value.

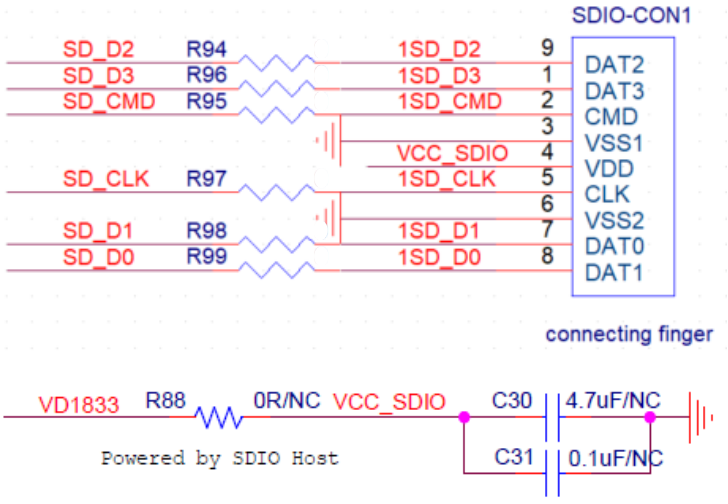

Figure 13-1 SDIO connector schematic design

14 General SPI

14.1 Introduction

- The chip supports Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol.
- Master or slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps

NOTE

1. When the chip is configured as Master, SPI supports transmission with a maximum baud rate of 50Mbps. But when the chip is configured as Slave, whether it can support a maximum baud rate of 50Mbps is controlled by the connected master. Due to the path delay and pad delay of internal signals in the master and slave devices, as well as some delays that may be introduced by pads or PCBs, the connected master needs to support delayed sampling function in order to correctly receive data sent by the slave at 50Mbps baud rate.

2. Dedicated SPI has many groups and does not allow cross group use between signal lines.

14.2 Schematic Reference Design

- Generally, four signal wires (CS, CLK, MISO, and MOSI) can be directly connected to external device.
- Users can pull CS pin up to Vcc by a 10K resistor, so that the CS pin has a certain high level state to avoid bus floating.
- Users also can place resistors connected in series on four signal lines to reduce signal reflection. Users can choose the resistance value based on actual usage scenarios, and it is recommended to use around 27R resistors.

15 SWD

15.1 Schematic Reference Design

- Suggest ground shielding between SWDCLK and SWDIO signal traces to avoid signal crosstalk.
- It is recommended to connect a 22R damping resistor in series at the source of both SWDIO and SWDCLK signals to suppress signal reflection.
- It is recommended to connect one ESD protection device in parallel on each of the SWDIO and SWDCLK signal traces, as manual hot swapping is required during debugging.
- According to the SWD standard, it is recommended to configure the SWD data pad to pull-up state after power on.
- To meet the debugging requirements in engineering development, users need to reserve the signal output points for SWDIO and SWDCLK.

NOTE

1. Port PA18 and port PA19 are default configured as SWD interface but users can configure relevant register to switch these two ports to other functions. If users use PA18 and PA19 for other functions except SWD and connect the two ports to external circuits, users must avoid SWD toggle behavior with a risk of misidentification before switching off the SWD function from the two ports.

16 Universal Serial Bus

USB support high speed, full speed and low speed rates. Both Device mode and host mode are supported. But Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) are not supported. The USB peripheral is compliant with the USB 2.0 specification.

16.1 Pin description

DM and DP are reused with GPIO. When used as USB function, the IO needs to be configured as no pull.
For more information, please refer to Pin Mux table.

16.2 Schematic

1) The TVS device should be put closely with USB socket to avoid chip damage or breakdown caused by ESD (Electro-Static discharge). DP/DM/VBUS requires ESD devices with different specifications.
2) The DP/DM is connected in series with a resistor to prevent D+/D- signal overshoot with VBUS. The resistance is generally 2.5ohm and placed close to the USB interface. If the interface is type A or type C, this resistor can be replaced with 0 ohm. Also, it is recommended to reserve a footprint for a capacitor to ground on each trace.
3) For ESD and EMC performance, it is recommended to keep the chassis ground and digital ground isolated.

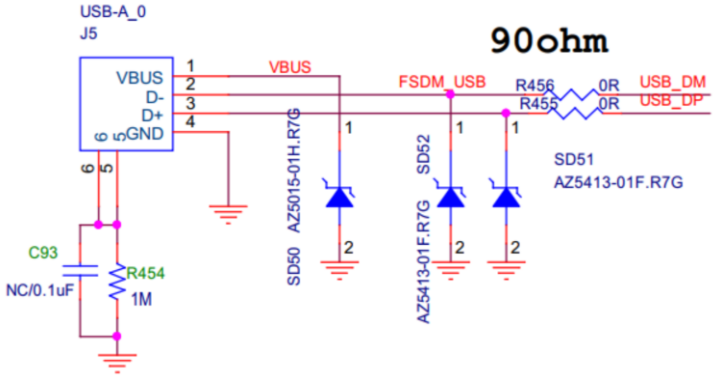

Figure 16-1 Schematic of Type-A USB interface

17 RMII

The interface support RMII mode with external Ethernet PHY rceivers, such as RTL8201F.

- support RMII mode, both 100base-TX, 10base-T
- IEEE 802.3AZ-2010(EEE), need PHY support
- Support 50Mhz clock output to PHY system clock

17.1 Schematic reference design

1) RMII support 50MHz clock output to PHY, users can configure the pin as the EXT_CLK_OUT function through the pin mux table, which outputs a 50MHz clock to the PHY's system clock, if the PHY chip that support external clock input, the PHY's XTAL can be omitted. For more details, please refer to the PHY's datasheet. The schematic reference is shown in the figure below.

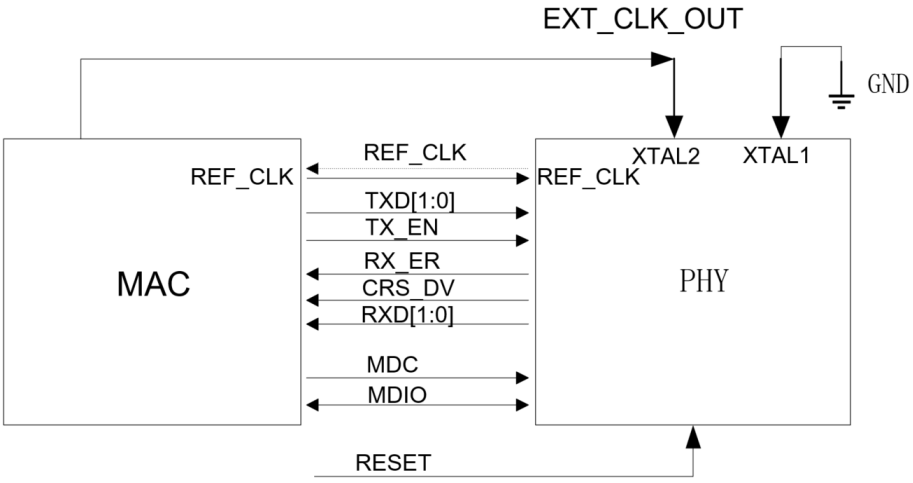

Figure 17-1 Schematic of RMII case1

2) If the PHY's system clock is provided by an additional XTAL, then configuring EXT_CLK_OUT is not necessary. the schematic diagram is shown in the figure as below

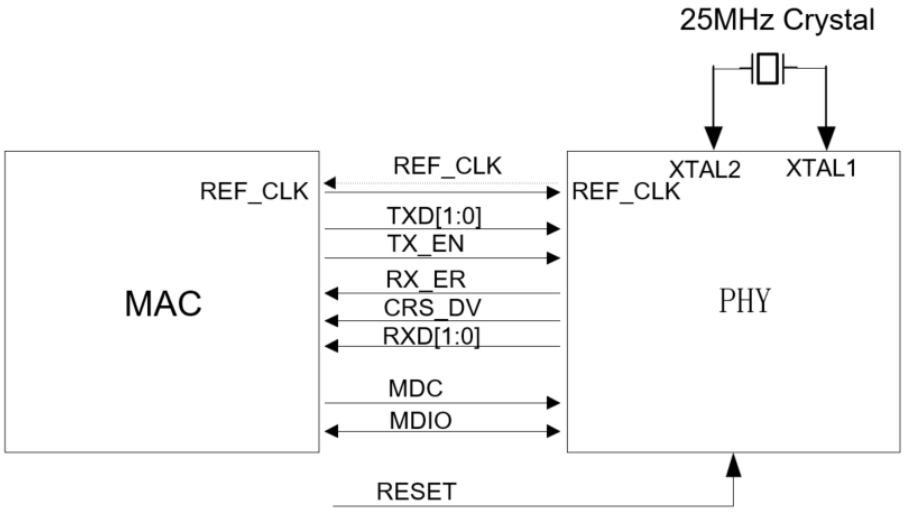

Figure 17-2 Schematic of RMII case2

NOTE: for RMII case1 and case2, the REFCLK can come from either the MAC or the PHY. If REFCLK comes from the PHY, place the filter network close to the MAC side; if it comes from the MAC, place it close to the PHY side, the schematic diagram is shown in the figure below.

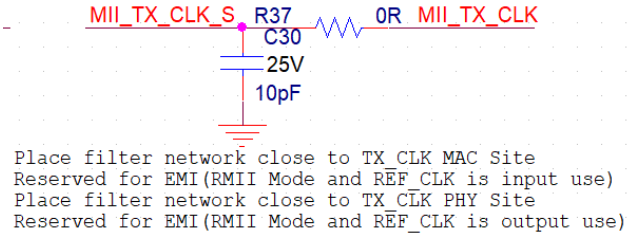

Figure 17-3 Schematic of filter network

3) If the PHY chip use RTL8201F, an extra circuit connection method is supported. The REFCLK can be connected to the PHY's XTAL2, and the PHY's XTAL1 connect to GND to save on the PHY's XTAL, the schematic diagram is shown in the figure as below

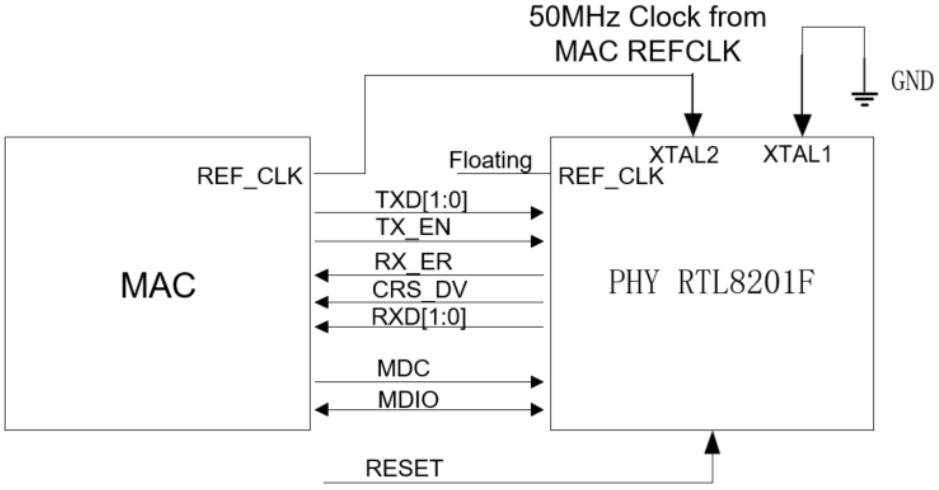

Figure 17-4 Schematic of RMII case3

4) RTL8721Fx RMII also support PHY mode, the REFCLK can come from either the MAC1 or the MAC2. If REFCLK comes from the PHY, place the filter network close to the MAC side; if it comes from the MAC, place it close to the PHY side, the schematic diagram is shown in the figure below.

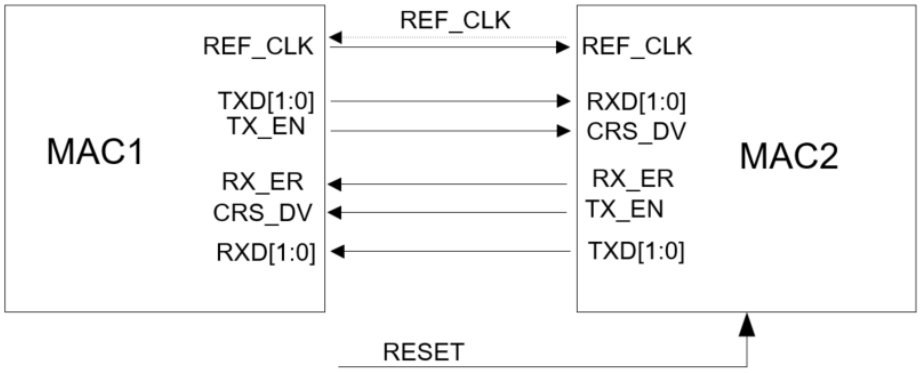

Figure 17-5 Schematic of RMII case4

18 LCDC

The chip support RGB\SRGB\MCU LCD interface, and support the following output format:

- RGB interface: 24bit-RGB888, 16bit-RGB565
- SRGB interface: 8bit-RGB888, 6bit-RGB565
- MCU interface: 24bit-RGB888, 16bit-RGB565, 8bit-RGB888, 8bit-RGB565

I /F Clock:

- RGB/SRGB interface: Maximum 50MHz
- MCU interface: Maximum 25MHz

18.1 Schematic Reference Design

LCDC-related IOs are reused with GPIOs, for detail information, please refer to the PINMUX document.

- Pin assignment should be optimized for smooth PCB routing to ensure better signal integrity. It is recommended to choose IOs far from RFIO as data & clock, and ensure sufficient clearance from RFIO to minimize interference.
- For reset and backlight enable pin, a PD or PU resistor is needed to meet the power on/off sequence of LCD.
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series matched resistor at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be adjusted by users according to their needs.
- The VDD of the LCD requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.
- Taking RGB888 as an example, the schematic reference design illustration is as follows.

NOTE

- *1. The selection of PU or PD resistors must be determined by the target LCD's signal characteristics and sequence requirement.*
  2. Different screens have varying FPC interface definitions and signal names, the following schematic is for illustration only.

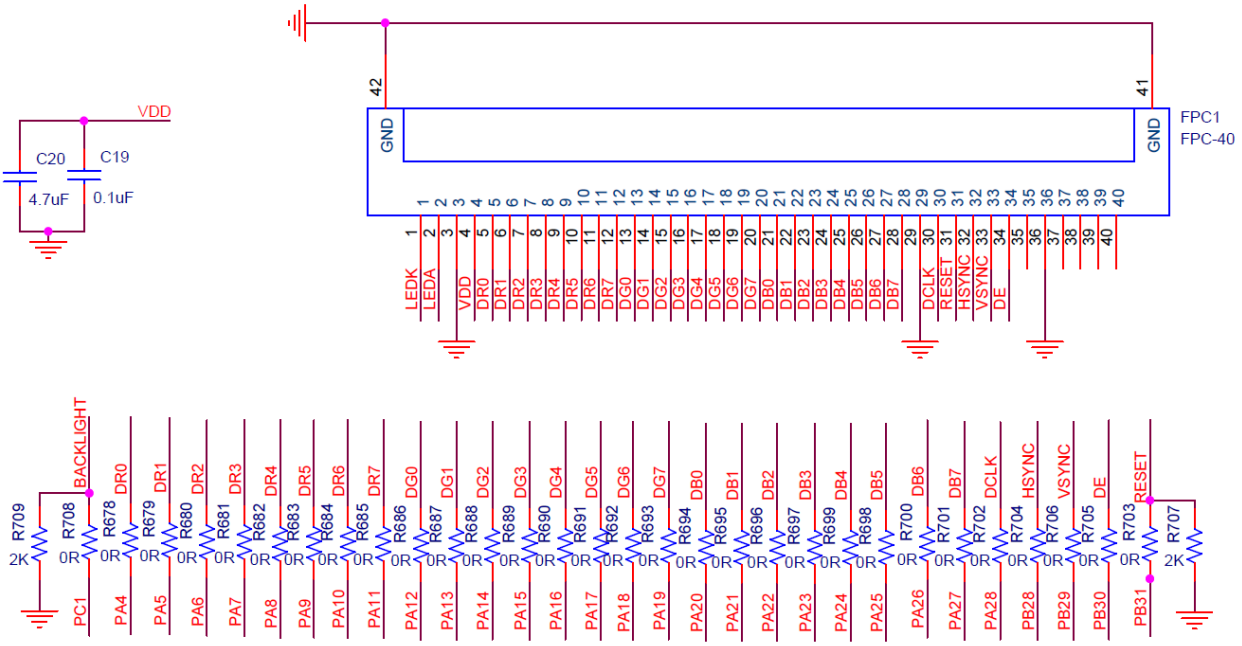

Figure 18-1 LCDC connector schematic

19 RF Circuit

- Diplexer (U7) is needed for combining RFIO_A (5G) and RFIO_G (2.4G).
- L-shape or Pi-shape matching (C26/L2 and C30/L4) should be placed between diplexer and main IC to tune RF impedance and harmonics rejection.
- A TVS (C29) is reserved for ESD protection.
- R12 and R15 is co-lay in our HDK for selecting RFIO path to RF connector (IPEX1) or printed antenna (U6).
- Pi-shape circuit (C27/L3/C28) is reserved for antenna matching.
- You can add a RF test point between R15 and U7 for RF test in mass production.

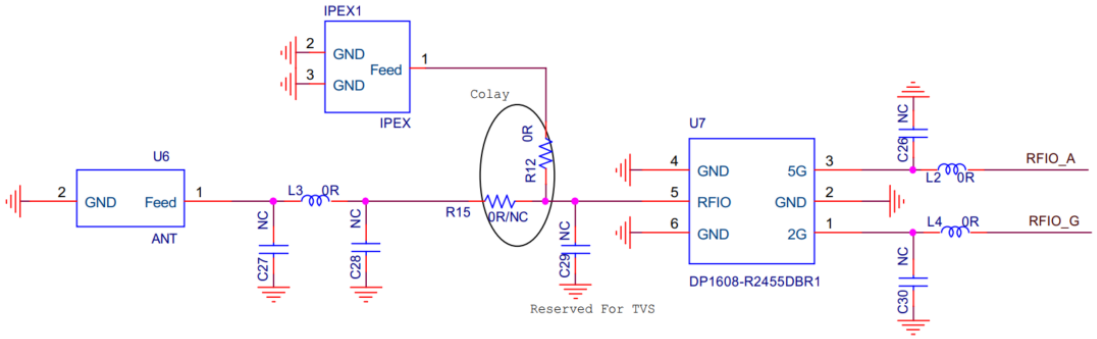

Figure 19-1 RFIO schematic

- If you need only single band of the chip (2.4G only or 5G only), pi-shape low pass filter as follows is recommended to be placed at RFIO pin to suppress Tx harmonics.

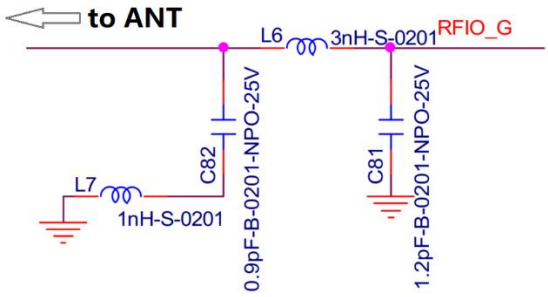

Figure 19-2 Pi-shape low pass filter for single band scenario

Revision History

Date	Version	Description
2025-07-22	R00	Initial release