RTL8721DA/RTL8721DC/RTL8721DG
PCB Layout and Assembly Guide

This document provides the PCB layout and assembly guideline

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document is suitable for RTL8721DA, RTL8721DC, and RTL8721DG.

2 Power

2.1 Switch Regulator Layout

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, LX, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- The input bypass capacitor CIN must be placed as close as possible to the VAH_DCDC pin and avoid vias between CIN and VAH_DCDC pin.
- LX pin is noise node switching with high frequency voltage swing and should be kept at small area. These feedback, analog, digital components and PCB trace keep away from the LX node to prevent stray capacitive noise pickup.
- Make VAH_DCDC, VOUT, and ground bus connections as wide as possible. These power trace length, width, and vias need to depend on recommend operating input and output current. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- For better thermal performance, design a wide and thick plane for E-PAD /GND_DCDC pin or add a lot of vias to connect ground layer plane.

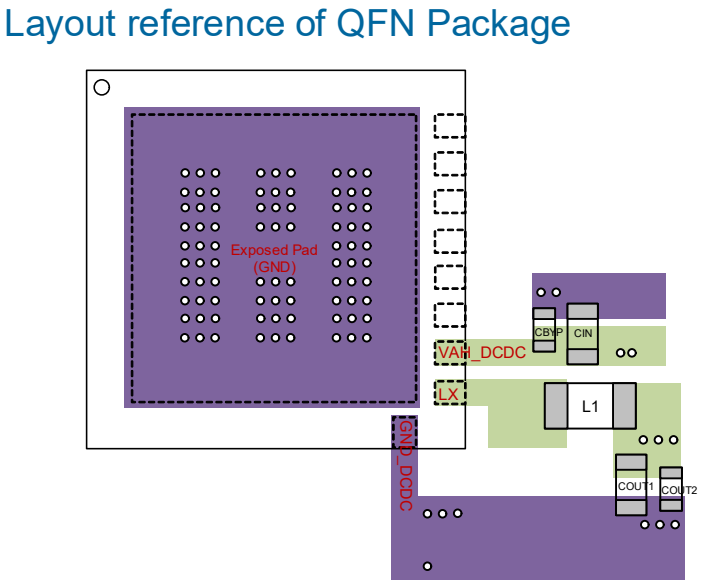

Figure 2-1 Switch Regulator Layout

2.2 Power Trace Routing

- The path of the power trace is recommended using star routing as shown in Figure 2-2 for better noise isolation among circuit blocks. It is strongly recommended that the power trace for PA (VRH_PA_G for 2.4G, VRH_PA_A for 5G) is routed separately. This SoC series support WiFi PA ultra-low power, namely PA can be supplied 1.25V. If you chose this mode in your product design, trace of VRM_RF which supplies DC power for 2.4G PA is also routed separately.

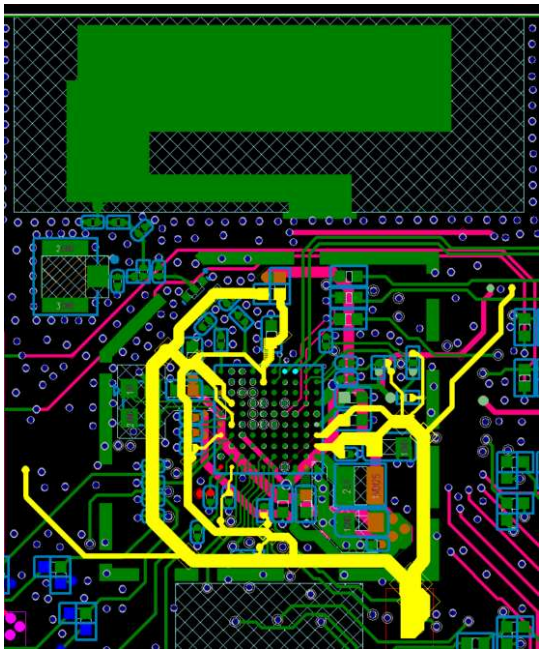

Figure 2-2 Star Routing

- The power trace should be wide enough for lower IR drop.
- Max current for every power pins is shown as follows, as a reference for determining the line width.
- Generally, the width of VRH_PA_G/VRH_PA_A shall be ≧15mil, and the width of VDL_CORE shall be ≧20mil.

Table 2-1 Current of Power pins

Symbol	Type	Pin number			Description	Max current(mA)
		RTL8721DA	RTL8721DC	RTL8721DG		
VAH_LDOM	PI	1	1	D1	3.3V/1.8V input for LDOM	200
LDOM_OUT	PO/I	-	2	E1	1.8V input for PSRAM/flash/IO power	200
VDL_CORE	PI	4	4	G1	0.9V input for digital core	300
VDH_IO1/IO2	PI	11/-	11/17	J1/K2	1.8V/3.3V input for digital I/O power domain	50
VRH_PAD_A	PI	18	28	J6	3.3V/1.8V input for RF circuit	50
VRH_PA_A	PI	19	29	K6	3.3V/1.8V/1.25V input for RF power amplifier circuit	450
VRH_PA_G	PI	24	34	J10	3.3V/1.8V input for RF power amplifier circuit	450
VRM_RF	PI	25	35	H10	1.25V input for RF circuit	50
VRH_SYN	PI	26	36	G9	3.3V/1.8V input for RF circuit	50
VRM_SYN	PI	27	37	F9	1.25V input for RF synthesizer circuit	50
VAH_XTAL	PI	30	40	E9	3.3V/1.8V input for XTAL circuit	20
VAM_AFE	PI	31	41	E10	1.25V input for RF AFE circuit	50
VAH_ADC	PI	32	42	D10	3.3V/1.8V input for ADC circuit	50
VDH_IO3	PI	36	51	A9	1.8V/3.3V input for digital I/O power domain	50
LDOC_OUT	PO	45	65	A3	0.9V output from core LDO and 0.9V input for digital core	500
VAM_LDOC	PI	46	66	A2	1.25V input for LDOC	500
LX	PO	47	67	B1	DCDC regulator output	900
VAH_DCDC	PI	48	68	C1	3.3V/1.8V input for DCDC regulator	400
VDH_RTC	PI	-	-	A10	3.3V/1.8V input for RTC circuit	20
GND_DCDC	PI	-	-	A1	DCDC regulator GND	400
VAL_PLL	PI	-	-	D8	0.9V input for ADC	20

3 Crystal

- The high speed ($\geq 10\text{kHz}$) signal traces shall be keep far away from XI/XO pins and trace.
- Place an intact GND plane with shortest distance connected to the E-PAD under the whole crystal routings. If the GND can't be connected to E-PAD directly, there should be noisy current flowing on this GND plane.
- If the dielectric core of the PCB is too thin(ex: ≦3mil), the high parasitic capacitance on XI/XO routings may dominates the crystal frequency, then the GND under the routes shell be removed, and the high speed signal traces on the lower layers shall be kept far out of the empty (under crystal block) area.
- Signal and power trace near XI/XO should be isolated by ground.
- The crystal should be kept out in top layer.
- Keep whole XI/XO traces in the same layer.

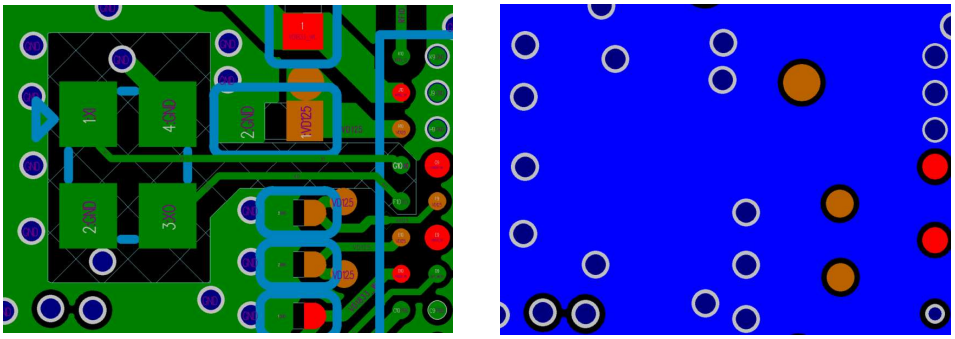

Figure 3-1 Crystal Layout-TOP Layer, GND Layer

4 RF

- The characteristic impedance of RF trace should be 50Ω.
- Placing more GND vias along the RF trace is recommended.

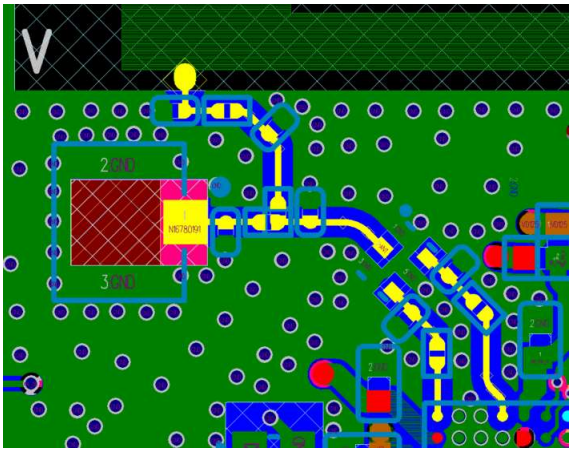

Figure 4-1 RF Trace

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces. The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

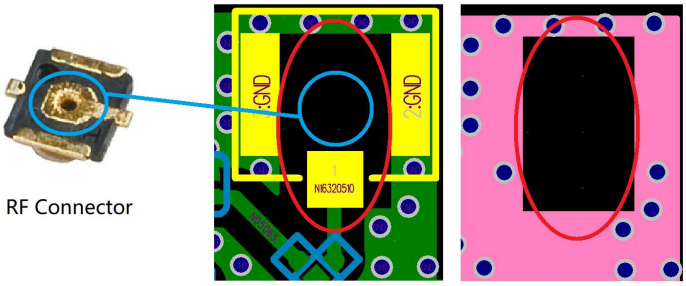

Figure 4-2 Keep-out for RF connector

5 Shielding

- Considering the EMC design, must comply with the following design rules:
  - For good shielding case grounding, there must be GND via placed on/around the soldering pads and the recommended via spacing is a≤1.5mm.
  - The open gap is recommended b≤2mm.
  - Use separated shielding cases if the other circuit blocks need to be shielded as well.
  - The shielding cover soldering on PCB is recommended If do use joint shielding case (frame + cover), make sure that the cover touches the compartment frame firmly.
  - Height: if possible, the minimum (inner) height suggest >1mm.

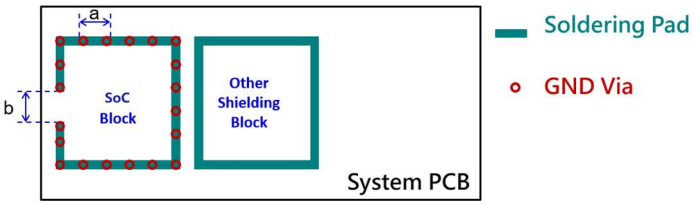

Figure 5-1 Shielding Layout

6 Flash & SDIO

- Place the matched resistance close to the transmitting end.
- The data and clock lines should be length-matched and surrounded by ground lines. Ensure that the spacing between lines is greater than three times the line width and reference plane is intact. Avoid placing signal lines close to high frequency signals.

7 USB

- D+ and D- are wired in a differential manner, and through the continuous reference plane layer to ensure the consistency of impedance, the differential impedance of the signal line is Z=90Ω±15%.
- The USB interface specifies a current of 500mA, but the VBUS trace must be able to withstand a current of 1A to prevent overcurrent events.
- The traces of D+ and D- must be of the same length, and the length error should not exceed 150mil. Instead of right angles, obtuse angles or arc traces are required. The maximum number of vias is 3, please minimize the use of vias to reduce signal reflection and impedance.
- The distance between the USB signal and other CLK or differential signal traces should be >20mil;
- If ESD protection devices and common mode inductors are required, they should be as close to the interface as possible;
- Avoid wiring the USB data signal lines under or near crystal oscillators, crystals, clock signal generators, power inductors, mounting holes, magnetic devices or ICs.

8 Cap Touch Controller (CTC)

In a typical Cap-Touch application, sensors are constructed with traces on a FR4/FR2 or flexible printed circuit (FPC). Cap-Touch layout design is an important step in the design phase, following the PCB layout design guidelines can help your design achieve higher noise immunity, lower parasitic capacitance (CP), and higher signal-to-noise ratio (SNR). The following factors must be considered during layout.

8.1 Board layers

- Sensor pads or sensor interfaces should be on the top (or bottom) side and surrounded by the hatched ground.
- All other components (ICs, VDD and GND traces, other signal traces) should be on the bottom (or top) side, and sensor traces are connected to the sensor pads or sensor interfaces by vias.
- Do not place the trace under the sensor button, and it is recommended not to be placed on the sensor layer for a long distance to prevent mis-touch caused by fingers touching the trace.

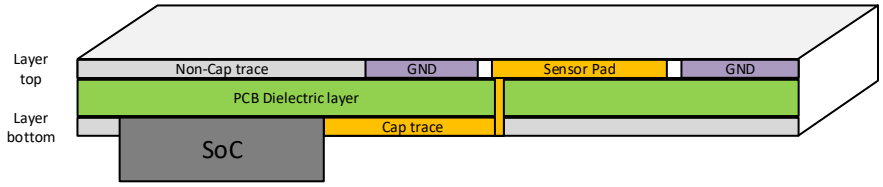

Figure 8-1 two layer PCB

- The copper foil close to the sensor or trace will increase the parasitic capacitance. It is recommended that the opposite layer of the sensor is not filled with copper. If the electromagnetic interference coupling near the sensor cannot be avoided, it is necessary to set up a grid GND near the same layer and opposite layer of the sensor and trace to reduce RF radiation and interference.
- It is not recommended to lay solid copper foil in the opposite layer or near the same layer of the sensor, which will lead to a serious decrease in sensitivity.
- for four-layer or six-layer PCB, if the sensor is located in the first layer, the second layer of the overlapping position cannot have GND copper foil (including grid ground), because in most PCB structures, the distance between the first layer and the second layer is very close, which will produce a large parasitic capacitance for the sensor.
- Thin PCB application: when the thickness of PCB is less than 1.0mm or FPC soft board PCB application, the opposite of sensor should not lay GND to reduce the parasitic capacitance.
- Connector: If the sensor button and the SoC are not on the same PCB layout, the FPC usually needs to connect two PCB. To minimize parasitic capacitance, it is recommended to select a small package pad connector (no copper or grid laying under the connector), and the length of the FPC should be shortened as far as possible.
- Pin reuse: it is not recommended to reuse TOUCH pin with other functions. If necessary, it is recommended to set the jump cap and function selection resistance close to the IC.
- Overlay: covering a layer of nonconductive dielectric overlay outside the sensor copper foil can adapt to more applications, but also can reduce ESD and other hazards. However, the presence of a cover layer reduces the capacitance increased by the finger contact, which significantly reduces the sensitivity. At the same time, because the cover layer is in direct contact with the copper foil, the conductive material cannot be used as a cover layer, which will be connected with the sensor to connect part of the sensor and increase the parasitic capacitor. Generally, the finger capacitance is directly proportional to the dielectric constant of the cover layer and is inversely proportional to the thickness of the cover layer. It is recommended to use materials with a higher dielectric constant, while the thickness of the cover layer should be as small as possible. As the air dielectric constant is very low, it is best to use glue to fix the air gap between the sensor and the cover layer. In practical application, materials with dielectric constant between 2 and 8 are selected as overlay, such as glass, acrylic, plastic and so on.

8.2 GND

- The distance between the sensor button and the floor on the same layer is at least 1.5 mm；

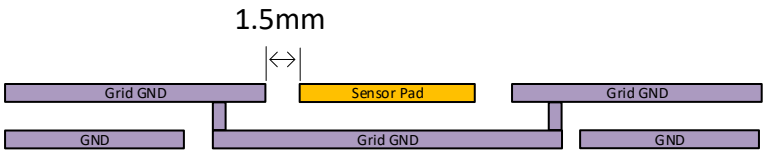

Figure 8-2 Gap between PAD and GND

- Copper is not recommended to lay under the sensor. If copper must be laid, choose grid copper. The grid site specification near the

sensor is:

- Top layer (sensor in the same layer): 25% (7 mil line width, 45 mil spacing), see Figure 8-4;
- Opposite layer: 17% (7 mil line width, 70 mil spacing);

- It is not recommended to have a large area of solid copper foil near the sensor button, which can be made by grid laying copper transition, and the width of the transition zone is at least 2 mm;

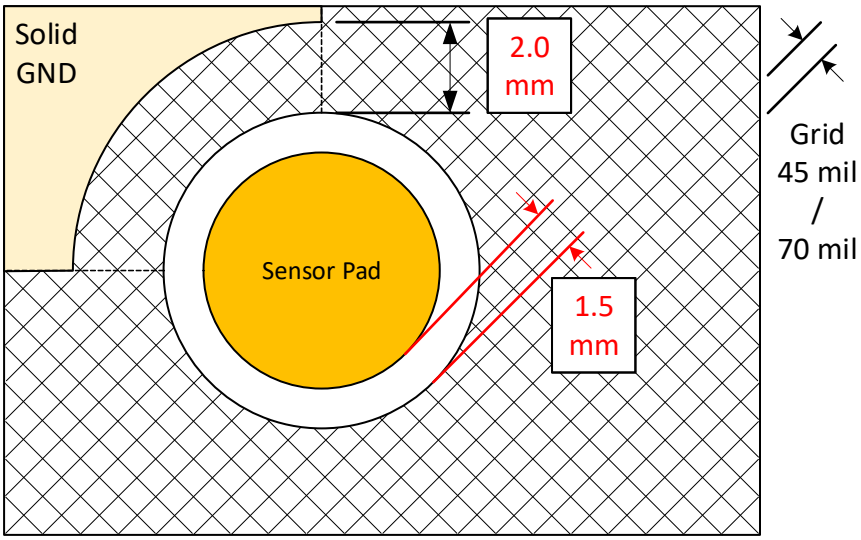

Figure 8-3 GND grid

- The distance between the sensor trace and the grid laying of the same layer is at least 0.5 mm;

8.3 Trace

Sensor trace connects IC and touch PAD, which is also the main way to introduce interference.

- Stay away from high-speed signals (RF, I2C, SPI, etc.) and high-power and high-noise trace (switching power supplies, etc.) as far as possible, and pay special attention to avoid parallel lines with them. If it is unavoidable, it is necessary to ensure that the intersection is at right angles.

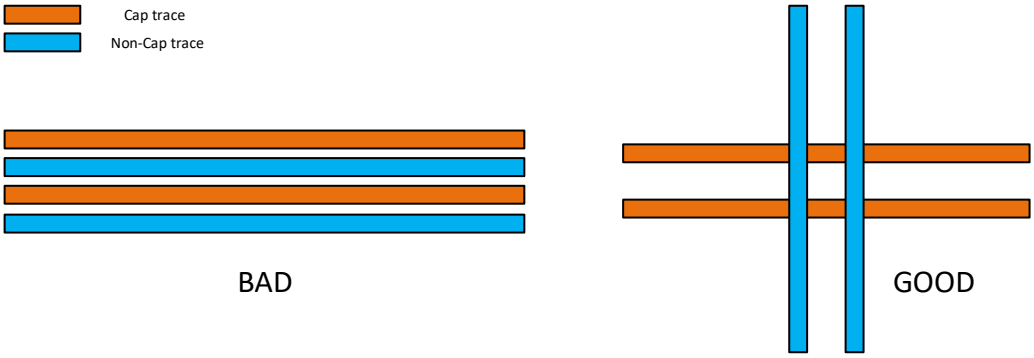

Figure 8-4 trace intersection

- If the sensor trace cannot be avoided parallel to the high-speed signal trace, GND with enough vias needs to be laid between the two to shield.;
- In order to prevent crosstalk, the parallel trace between the two adjacent channels is as far away as possible or lay GND between them. If only some of the all channels are used, the number of channels can be selected at intervals, and the software disables the unselected channels. If it is unavoidable, the distance between adjacent trace should be more than 3 times its trace width.
- The trace should be short and fine as far as possible, usually the maximum length on the PCB is < 30 cm (<= 5 cm on the flexible circuit board), it is recommended that the trace width of 5 ~ 6 mil;
- The gap between the trace and GND is 0.5mm;

8.3.1 Via number and position

In order to reduce the parasitic capacitance and minimize the number of vias, it is recommended that the number of vias should not exceed

3. To shorten the trace, the via can be placed on the edge of the sensor.

8.3.2 Series resistor

All cap-touch channels must have a 560ohm series resistance placed close to the chip (< 1cm) to reduce RF interference and provide ESD Protection.

8.4 Sensor PAD

8.4.1 Button

- The Sensor PAD shape is recommended to be round. In some applications, it can be a ring, with a LED in the middle, it is necessary to note that the LED trace is isolated from the TOUCH signal. LED also suggests adding RC filtering to delay the edge of the signal.;

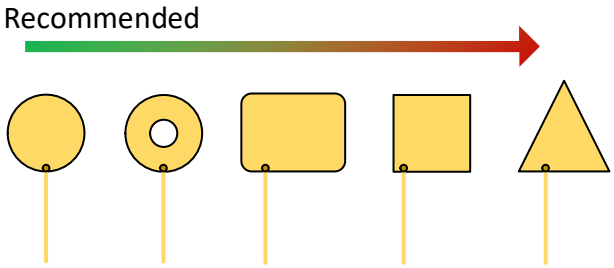

Figure 8-5 Sensor shape

- According to the size of the area touched by the finger, the button size recommends a circular diameter of 10.0mm~15.0mm. The larger PAD can better capture the finger touch signal, in the case of thick cover, the PAD area should be increased properly, and otherwise the sensitivity will be seriously reduced.

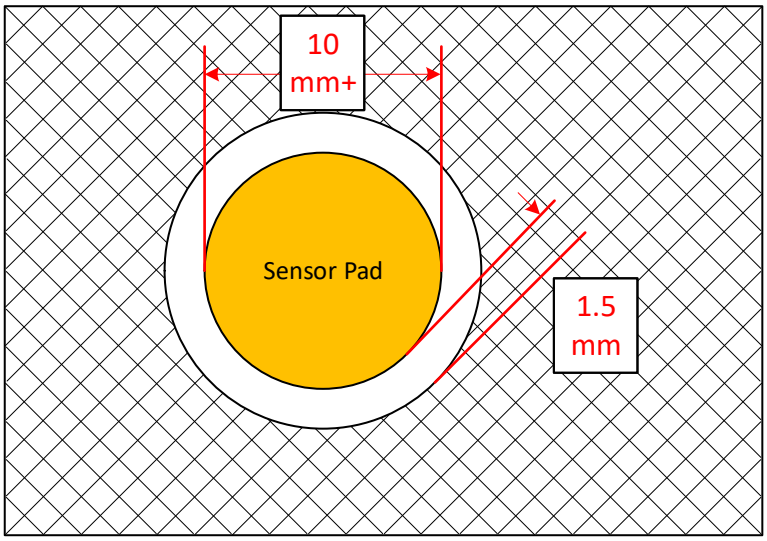

Figure 8-6 Sensor PAD on the PCB

- The gap between the PAD and the surrounding GND is generally 1.5mm~2.5mm. If there is a cover layer (protection overlay), the width of the gap should be increased appropriately increased;
- The thickness of the overlay shall not exceed 4.0mm, and it is recommended to be within 3.0mm. Touch sensitivity may be severely reduced unless a larger diameter sensor PAD is used;
- The spacing between adjacent PADS should be as large as possible to prevent the fingers from pressing multi PAD. The button is recommended to be separated by more than 8mm GND.

8.4.2 Spring

In some applications, PCB cannot be directly arranged on the user touch surface, or the shape of the touch surface is irregular. Therefore, it

is necessary to use conductors to connect the PCB sensor and the user touch interface. The metal spring is usually used as the elastic connector between the two, and the electric field is coupled to the overlay through the compressed spring.

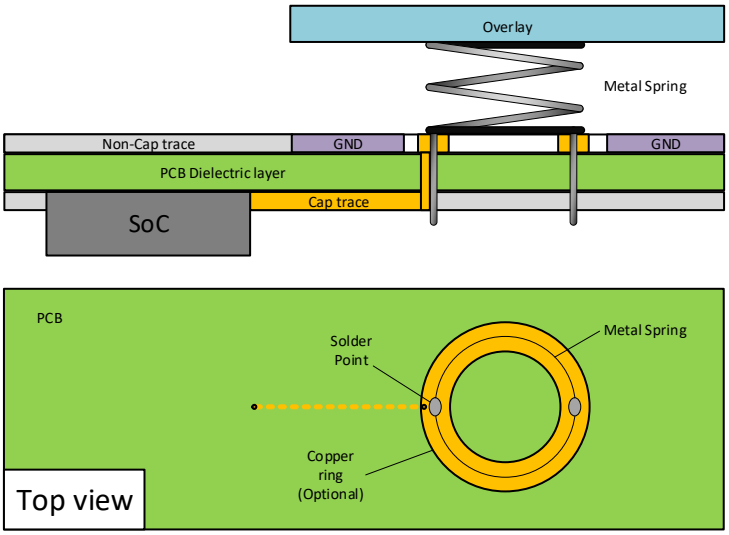

Figure 8-7 Spring diagram

- The spring has high side sensitivity, the adjacent spring needs to be far away from each other to prevent accidental touch;
- When the cover layer is 3-5 mm thick, the spring diameter is 15~30 mm, and the large diameter spring can improve the sensitivity, but at the same time, more noise is introduced;
- When the spring is used as a sensor, the PAD can be a ring, or only the hole for mounting spring;
- There is at least 1.5 mm gap between the sensor ring and GND;
- The contact part of the spring and the PCB is far away from other signal and the GND;
- LED indicators can also be set in the middle area of the spring, as described in the previous section.

9 General Analog-to-Digital Converter (ADC)

- The routing shall be required to avoid parallel arrangement with high-speed signal traces and high-current power traces. If intersection cannot be avoided, it shall be as vertically as possible; if parallel arrangement, separation GND shall be laid between them.
  - The sources of interference include: SWR power trace and inductor, RF trace, High speed communication interface and so on.
- GND is arranged around the traces as much as possible.
- The traces should be as short as possible.
- When using the differential input mode (differential pair: CH 0 & CH 1, CH2 & CH3, CH4 & CH 5), it is necessary to ensure that the differential trace is arranged adjacent, and keep the same length and width as far as possible.

10 Audio

- The positions of the MIC peripheral devices are placed according to the requirements of the schematic diagram.
- The ESD device must be placed close to the MIC, and the traces drawn from the MIC must first pass through the ESD device before connecting to other devices.

11 Land Pattern and Assembly

- Refer the Package Specification in the datasheet for the detail dimension.
- Recommended to use the normal value in the dimension table.

11.1 Guideline for E-pad land patterns

11.1.1 The E-pad Design

- The center pad size should follow the same E-PAD size of package specifications in the datasheet.

11.1.2 Solder Mask Guidelines for E-pad

- The actual solder mask opening size should adding 2mil at each side to the size of the thermal pad.

11.1.3 Paste Mask Guidelines for E-pad

- Stencil openings should be segmented in exposed regions, solder paste coverage recommend matrix by 3*3 as follows:

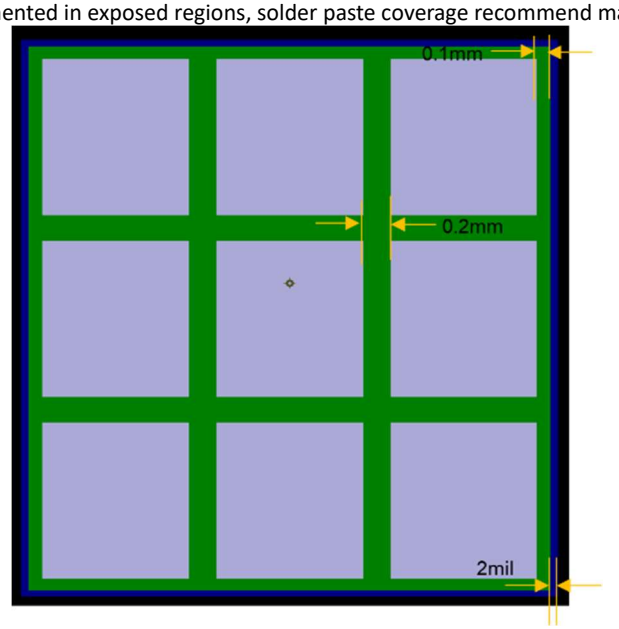

Figure 11-1 Paste Mask of Thermal Pad

- Recommended edge length/width of a matrix land is about 0.1mm.
- Distance between the lands should be about 0.2mm.
- Above two the ratio is 1:2
- Exposed pad design by matrix methods to prevent mass solder let QFN lift, stencil opening should be approximately 60~80% PCB exposed pad size.
- Thermal Pad voiding suggestion <30%

11.1.4 Center pad hole specification

- Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 0.6~1mm grid, as shown in Figure 11-2.
- And the vias under E-pad should be as much as possible for good heat dissipation. Large package like QFN100/QFN144 can use larger size of via and bigger pitch. But for small package size like QFN48/68, it should use smaller size of via and smaller pitch.
- The vias under the E-pad are recommended to be treated with epoxy via plug for low void.

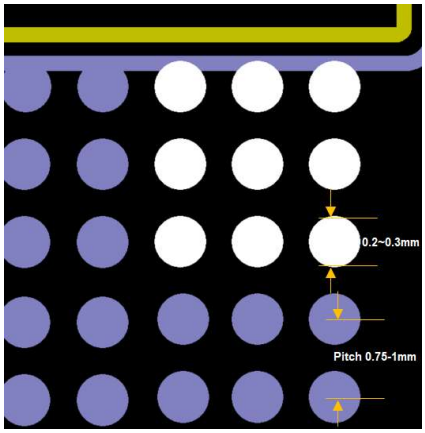

Figure 11-2 PCB Exposed Pad Land Pattern Via Grid

11.2 Signal I/O pad design

11.2.1 Guidelines for perimeter land patterns

- Extend of outer Cu Land towards package center as follows:

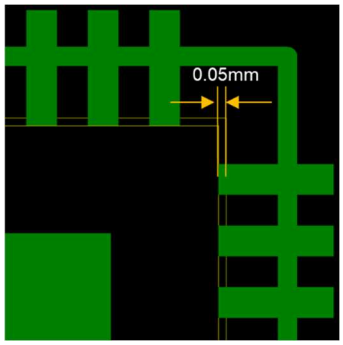

Figure 11-3 Length of outer lead perimeter size towards package center

- Length of Outer Cu land exterior to the package edge ≥ 0.2~0.3 mm

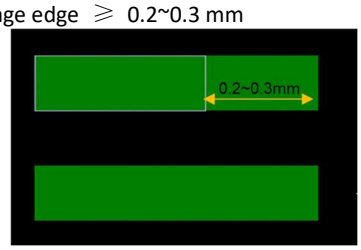

Figure 11-4 Length of outer lead perimeter size to the package edge

- For dual ring QFN, Length of Inner Cu Land L use max parameter.

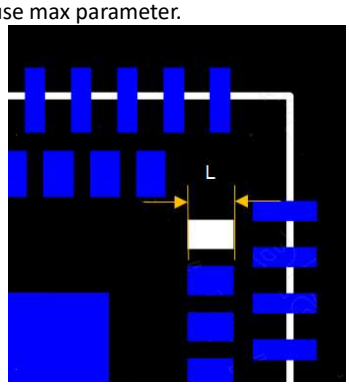

Figure 11-5 Length of Inner lead perimeter size

- Width of Inner Cu Land W should be extend to normal size+0.05mm(for 0.5mm pitch) in order to improve soldering yield. Or you can use the max W parameter in the datasheet.

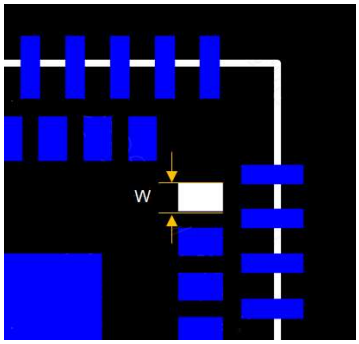

Figure 11-6 Width of Inner lead perimeter size

- For RTL8721DG which is 0.5mm pitch BGA package, the BGA ball land pattern should be circle and the diameter is 0.25mm.

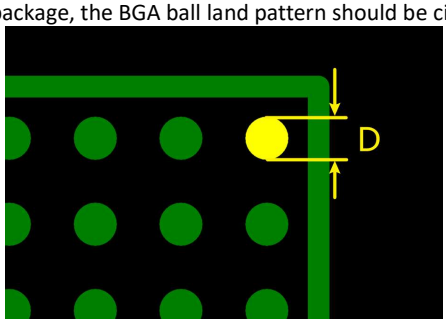

Figure 11-7 Dimension of BGA ball land pattern size

11.2.2 Solder Mask guidelines for perimeter lands

- The solder mask can be extend 2mil than the original size of each edge.
- As the follow picture, the orange part is the pin pad. And the red part is the solder mask. The yellow distance is 2mil.

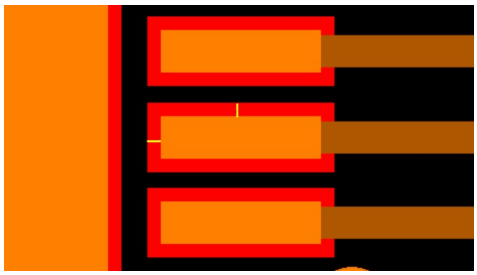

Figure 11-7 The pin pad and the solder mask

- For BGA land pattern， NSMD (Non-Solder Mask Defined) is recommended. And, the solder mask can be extend 1mil than the copper pads.

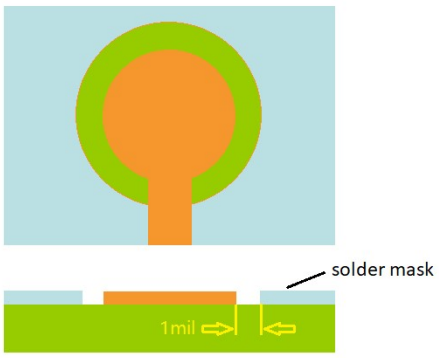

Figure 11-8 The pin pad and the solder mask

- I/O pin lead pitch will be small and small, If PCB fab technology ability is not enough space available for solder mask, we suggestion IC lead pitch low then 0.4mm PCB pad design use “trench” type solder mask opening to design .

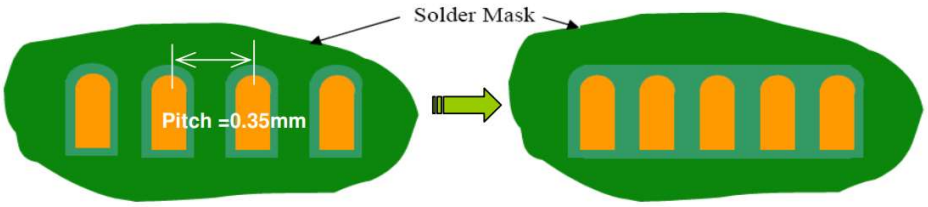

Figure 11-9 between the pads, it’s recommended to use “trench” type solder mask opening to design.

11.3 Stencil Design Guidelines

11.3.1 Stencil Type and Thickness

- Stencil type: Laser-Cut.
- The recommended stencil thickness as follows:

Table 11-1 Stencil Thickness

Terminal Pitch	Recommend Stencil Thickness
≥ 0.65	0.13 ~ 0.15mm
0.4 ~ 0.5	0.1 ~ 1.12mm
< 0.4	0.08 ~ 0.1mm

11.3.2 Solder Paste Type(s)

- The most common solder paste powder sizes for SMT are type 3 (T3), type 4 (T4), and type 5 (T5). The lower the number, the larger the particle size within the solder powder.

11.4 Oven temperature profile

- The reflow condition used in J-STD-020 as following table. All the temperature is measured on the topside of the package.

Table 11-2 Oven Control Data

Stage	Note	Pb-free assembly
Average ramp-up rate	T_L to Tp	3 ℃/ second max.
Preheat	Temperature min (T_{smin})	150℃
	Temperature max (Tsmax)	200℃
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217℃
	Time (t_L)	60 – 150 seconds
Peak package body temperature (Tp)		See following table. Tp must not exceed the specified classification temp in following table.
Time(tp) within 5℃ of the specified classification temperature (Tc)		30 seconds
Ramp-down rate (Tp to T_L)		6 ℃ / seconds max.
Time 25℃ to peak temperature		8 minutes max.

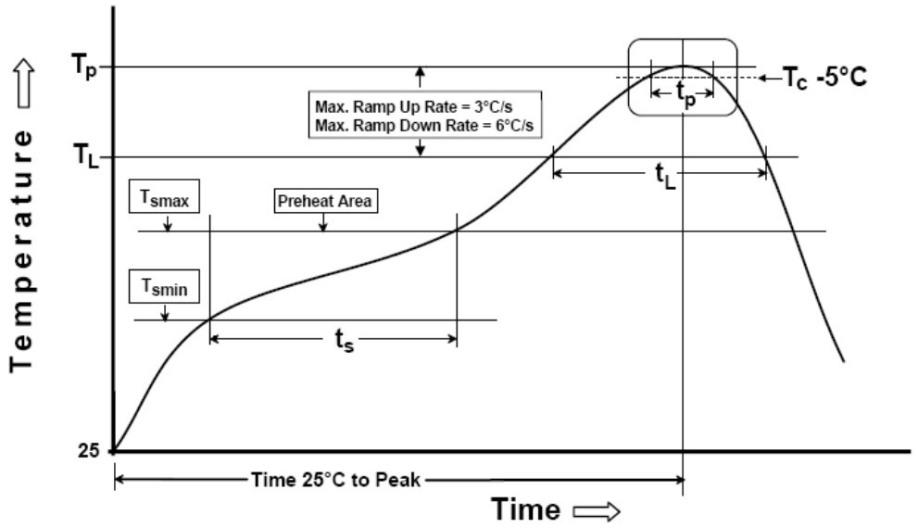

Figure 11-10 Recommended reflow profile

NOTE

The above reflow profile is for MSL classification only, not the recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameter in above table.

- The peak temperature package can sustain depends on its volume and thickness. The reason is that, engineering studies have shown that, thin, small volume SMD packages reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, technical and/or business issues normally require thin, small volume SMD packages to be classified at higher reflow temperatures.
- The different peak temperature for different package volume / thickness is listed as following table:

Table 11-3 Pb-free Process-Package Classification Reflow Temperature

Package Thickness	Volume < 350 mm3	Volume 350 – 2000 mm3	Volume > 2000
＜1.6 mm	260 +0 /-5℃	260 +0/-5 ℃	260 +0 /-5℃
1.6 – 2.5 mm	260 +0 /-5℃	250 +0/-5 ℃	245 +0/-5 ℃
≧ 2.5 mm	250 +0 /-5℃	245 +0/-5 ℃	245 +0/-5 ℃

- Reflow Condition Recommendation For SMT Process
  - In SMT process, the reflow temperature profile for manufacturing should be recommended by solder paste supplier, and the peak temperature should not be higher than the lowest peak temperature used for the MSL classification for the components on board.
  - The reflow temperature profile defined for MSL classification in J-STD-020 is not recommended to be used for real SMT process unless approved by solder paste supplier. Basically, the reflow profile used for MSL classification is for classification only and regardless of the solder paste itself. Thus the temperature profile is only to “simulate” the reflow process in real case, but not a recommendation for that. The real case still depends on solder paste itself.

Revision History

Date	Version	Description	Modified by
2023-07-20	R00	Initial release	Ziliang_yan
2023-12-13	R01	Update file name	Ziliang_yan