RTL8721Dx Hardware Design Guide

This document provides the Hardware design guide and notes

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document provides the Hardware design guide and notes for the RTL8721Dx.
Please refer to RTL8721DA_RTL8721DC_RTL8721DG_PCB_Layout_and_Assembly_Guide.pdf for layout

2 Power supplement

2.1 Power Structure

Only an external power supply is required for the RTL8721Dx. All the other required voltages can be converted and output by two embedded low-dropout regulators (LDO) and one embedded DC-DC switching regulator (DCDC). Embedded LDO and DC-DC have voltage-scaling function, which can effectively reduce power consumption. It is suggested to use embedded LDO and DC-DC powering RTL8721Dx. RTL8721Dx supports wide range input voltage from 1.71 to 3.63V, there is little difference in power structure between different input voltage range. Please refer to the datasheet for the operating voltage range of ICs with different part numbers.

2.1.1 1.95~3.63V Input Range

- The DCDC outputs typical 1.25V or 1.35V for RF circuits and LDO core (LDOC) input.
- The LDOC outputs typical 0.9V or 1.0V for digital core circuits.
- The LDO memory (LDOM) outputs typical 1.8V for optional embedded PSRAM or 1.8V Flash based on different part numbers. The LDOM can also supply power for external 1.8V Flash if needed. LDOM_ OUT only has output pin in specific part numbers. When there is a LDOM_OUT output pin, a capacitor of at least 4.7uF is required near the pin for LDO voltage stabilization
- VDH_IO contains up to three separate power pins VDH_IO1, VDH_IO2 and VDH_IO3 for different IOs. Specific power supply relationships can be found in pinmux table. VDH_ IO1 and VDH_ IO2 can independently select the power supply voltage without exceeding the external power supply voltage. Generally, if 1.8V power supply is required, the 1.8V power supply output from LDOM can be selected.

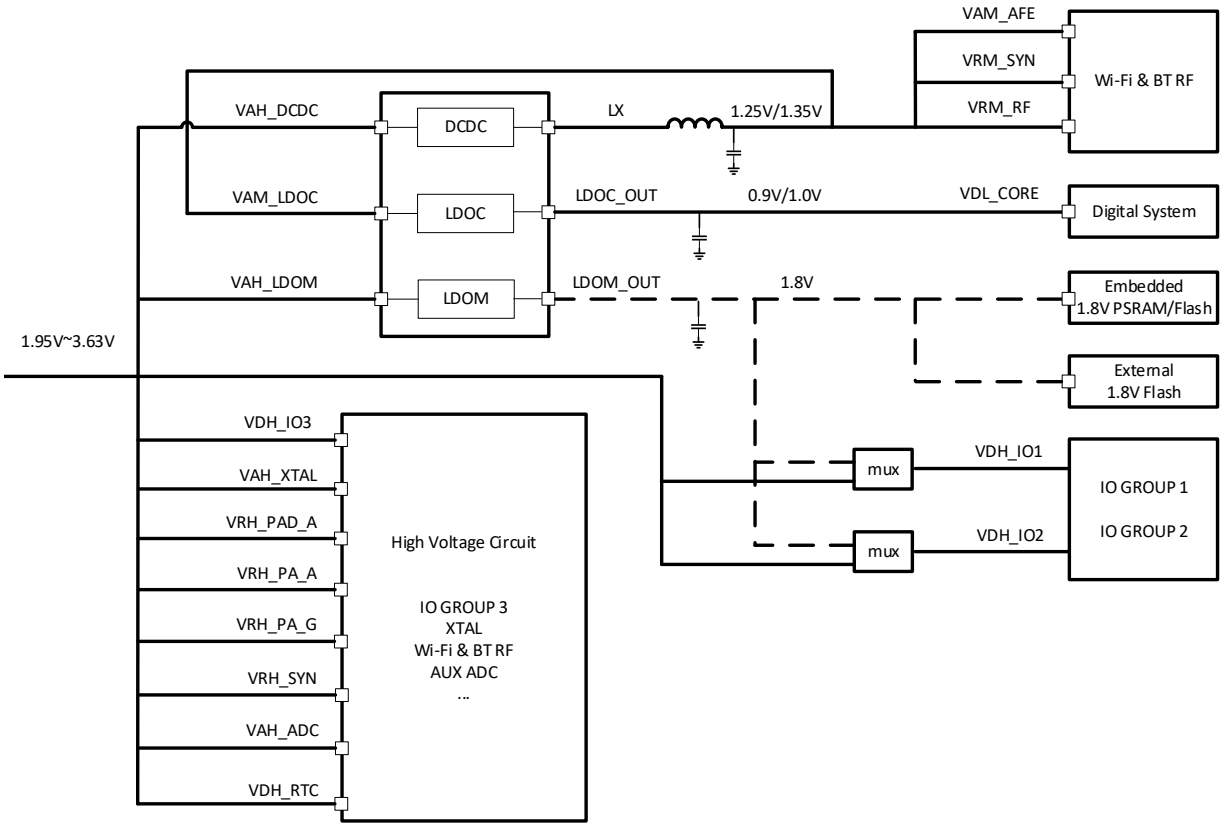
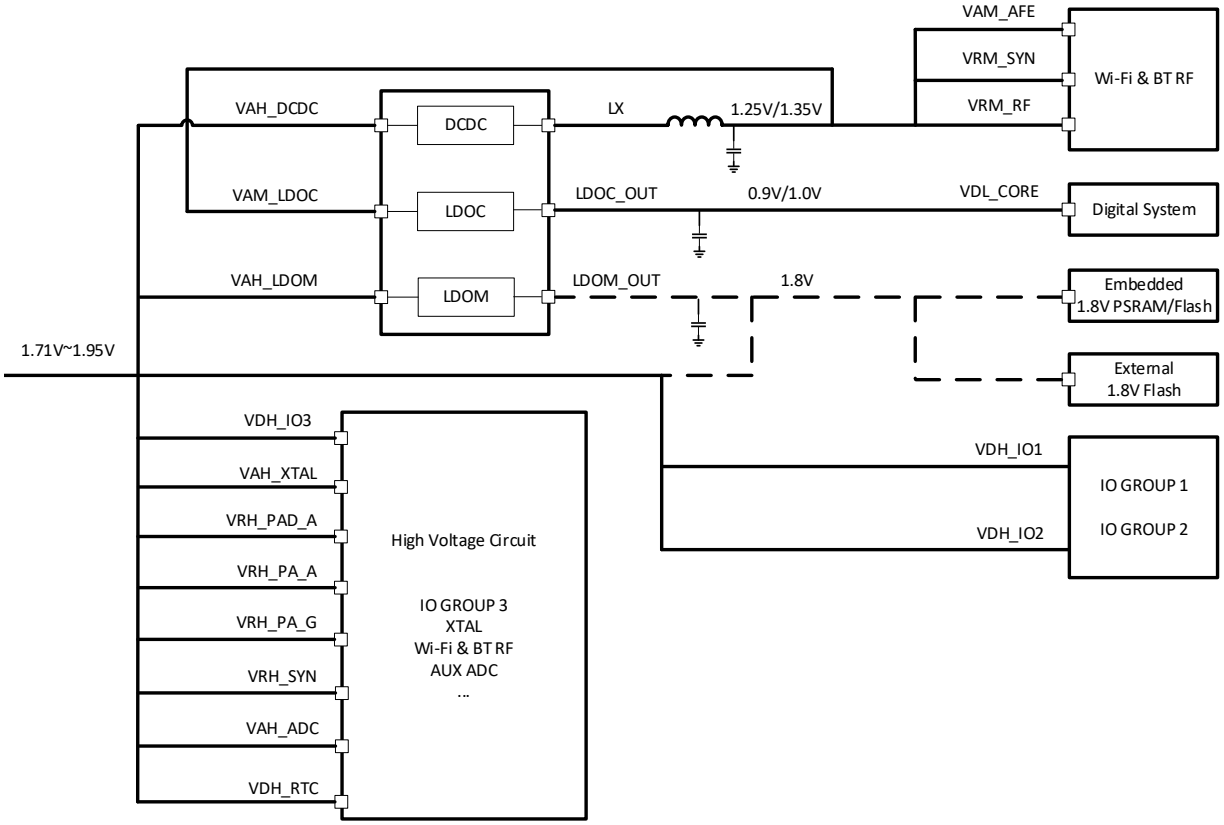


Figure 2-1 Power structure for input from 1.95 to 3.63V

2.1.2 1.71~1.95V Input Range

- The DCDC outputs typical 1.25V or 1.35V for RF circuits and LDO core (LDOC) input.
- The LDOC outputs typical 0.9V or 1.0V for digital core circuits.
- The LDOM cannot work normally under all working conditions when input voltage is under 1.95V because of low dropout voltage. It is suggested to power this pin with external power supply and turn off this LDO by software. Similarly, LDOM_ OUT only has output pin in specific part numbers. When there is a LDOM_OUT output pin, a capacitor of at least 4.7uF is required near the pin for LDO voltage stabilization.
- VDH_IO1 and VDH_IO2 can be only powered by external power supply in this situation.

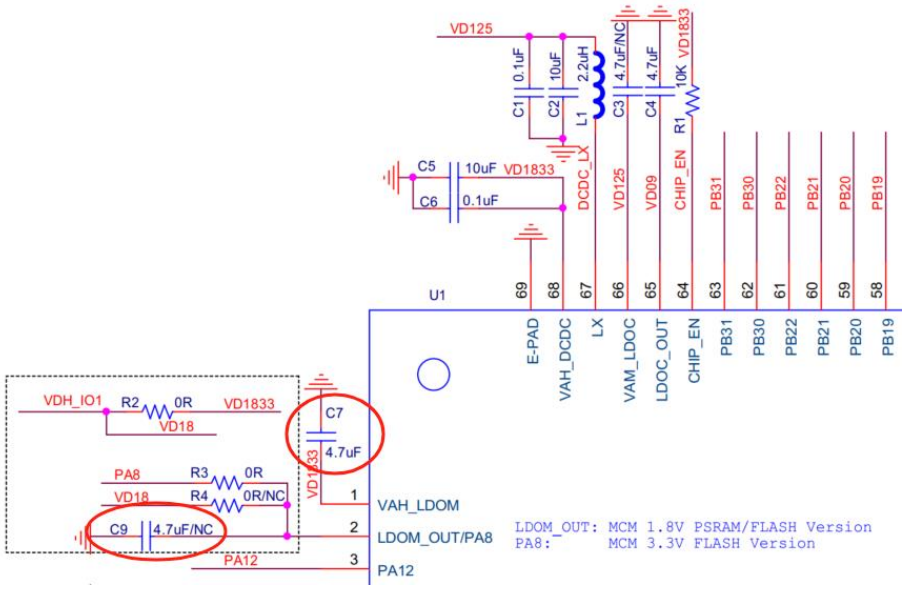


2.2 Capacitors and Inductance for Power Pins

Generally, for DCDC or LDO regulator's input and output, and RF PA power pins, large capacitor should be placed. For other pins, 0.1uF capacitor is needed.

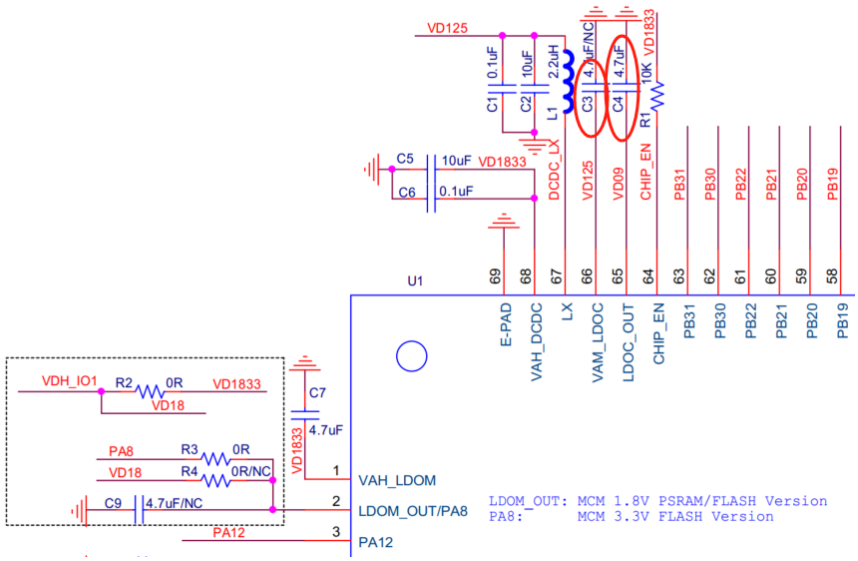
2.2.1 LDOM

- For package QFN48/QFN68, pin2 has different definition for different IC part number. Please refer to datasheet for more details.
- Taking QFN68 SCH for example, C7/C9 is for LDOM input and output. Capacitor 4.7uF is recommended. If pin2 function is GPIO PA8 for certain part number, you can remove C9 directly.



2.2.2 LDOC

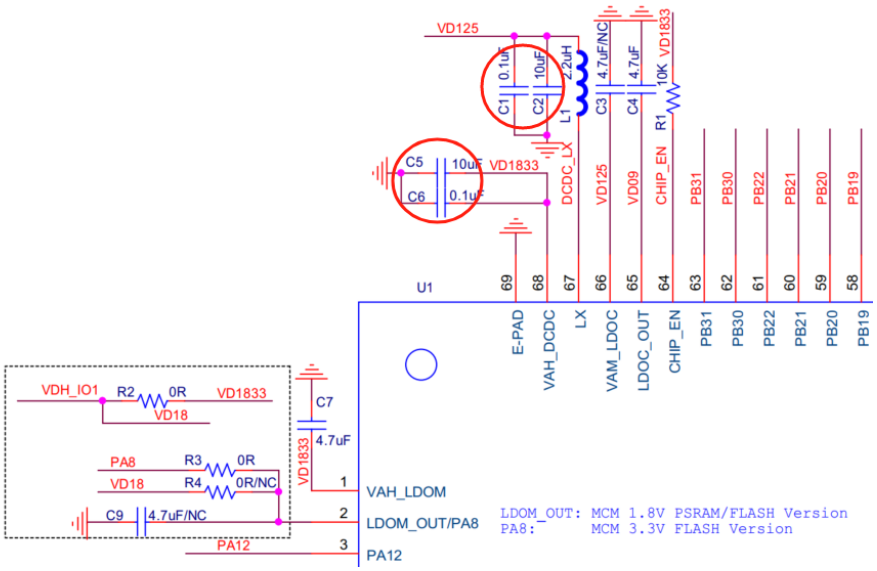
- C3/C4 is for LDOC input and output, capacitor 4.7uF is recommended.
- Generally, the layout trace length from DCDC output to LDOC input is short enough, so you can remove C3 from your BOM list for lower cost. But C3 should be reserved in schematic.



2.2.3 DCDC

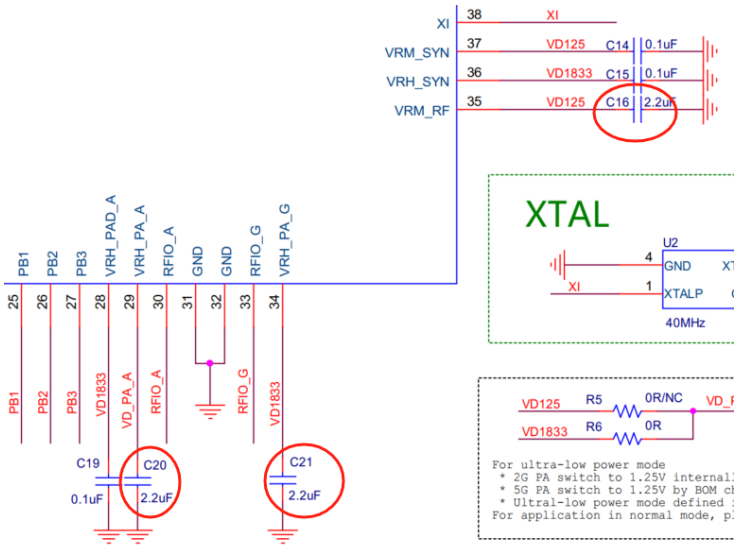
- C5/C6, C1/C2 are for DCDC input and output, capacitor 0.1uF+10uF is recommended.
- L1 is power inductor for DCDC regulator. You should chose the inductor carefully. The inductor specifications recommended are as follows.

Inductance (uH)	Tol. (%)	Saturation Current, ⊿ L=30%(mA)	Temperature Current, ⊿ T=40℃(mA)	Rdc(Ω) typ.
2.2	20	>= 1400	>= 1400	0.1



2.2.4 RF PA Pins

- C20 is for 5G PA, C21 is for 2.4G PA and C16 is for BT PA. Capacitor 2.2uF or larger is recommended.



2.3 Embedded Regulators Characteristics

The characteristics of embedded regulators including LDOC, DCDC, and LDOM are guaranteed by design.

Table 2-1 Embedded regulators characteristics

Regulators	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LDOC	VIN	Input voltage range	LDO mode	1.20	1.25/1.35	1.45	V
			Bypass mode	0.6	0.7	0.9	
	VOUT	Output voltage range	LDO mode	0.81	0.9/1.0	1.05	V
	$V_{OUT-RIPPLE}$	Output voltage ripple	LDO mode			+/-50	mV
DCDC	VIN	Input voltage range		1.71	1.8/3.3	3.63	V
	VOUT	Output voltage range		0.6	1.25/1.35	1.45	V
	F	Switching frequency	PWM mode	-	2	-	MHz
	$V_{OUT-RIPPLE}$	Output voltage ripple	PWM mode			+/-30	mV

		Output voltage ripple	PFM mode			+/-62.5	mV
LDOM	VIN	Input voltage range		1.71	3.3	3.63	V
	VOUT	Output voltage range		1.7	1.8	1.9	V
	$V_{OUT-RIPPLE}$	Output voltage ripple				+/-50	mV

2.4 External Voltage Regulator Module Recommendation

VXH[1] is the main power supply for Wi-Fi, BT, USB, embedded DC-DC switching regulators, etc. Recommended specification for external VRM is listed in Table 2-2.

- The output voltage of external voltage regulator module can be from 1.71 to 3.63V. Output voltage noise is included in output voltage range.
- The stability of the output power supply is important for RTL8721Dx. Suggested output voltage ripple should be under +/-100mV. Output voltage ripple should be considered in all possible working states such as WIFI initialization, WIFI TRX, etc. If the VXH is shared with other high power consuming circuits, such as audio amplifiers, IR circuits, etc., output voltage ripple also needs to be under +/-100mV during the operation of these circuits.
- Continuous output current should be higher than 1A, which excluding power consumption in circuits other than RTL8721Dx.
- Suggested output voltage rise time is from 0.1 to 3ms, more specific power sequence can be found in datasheet.

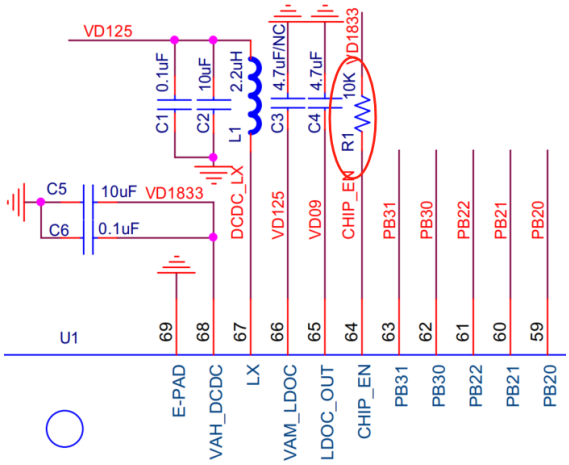
Table 2-2 External VRM recommended specification

Symbol	Parameter	Operation conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	Including $V_{OUT-RIPPLE}$	1.71	3.3	3.63	V
$V_{OUT-RIPPLE}$	Output voltage ripple	Including all possible operation conditions[1]			+/- 100	mV
I_{OUT}	Continuous output current	Excluding power consumption in circuits other than RTL8721Dx	1			A
T_{RISE}[2]	Output voltage rise time		0.1	1	3	ms

[1] VXH *refers to power supply including VAH_LDOM, VDH_IO1, VDH_IO2, VDH_IO3, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VAH_ADC, VDH_RTC and VAH_DCDC.*

3 Chip Enable Pin

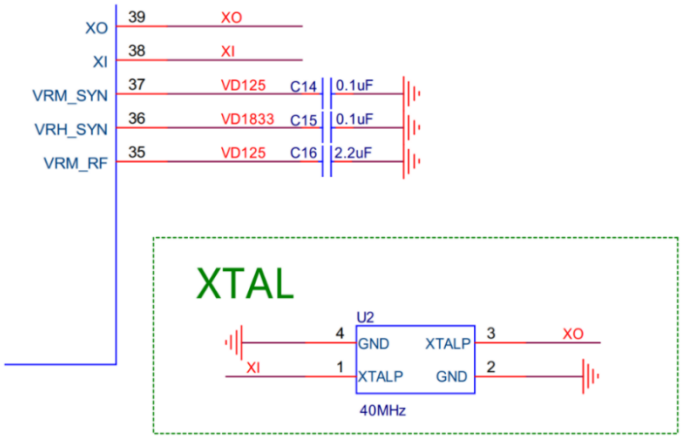
- Chip enable pin should be pull high with a 10K resistor by default.



4 Crystal Characteristics

The chip has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.

Please connect crystal XI/XO to main IC directly. There is no need to add extra capacitors on net XI/XO.



[

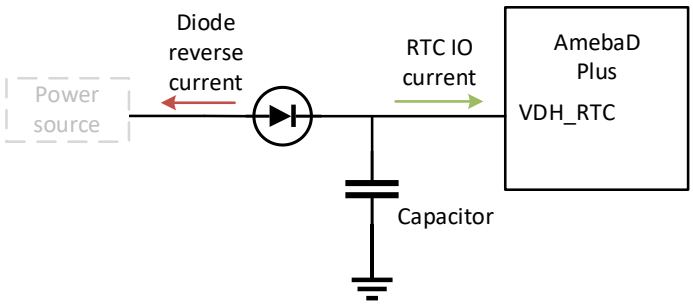
The characteristic requirements of external crystal are listed in Table 4-1 .

Table 4-1 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

5 RTC Reference Design

The RTC can keep working independently when other power supply pins in the system are powered off, and the VDH_RTC power supply pin is powered by a capacitor for short time (the accuracy of the RTC is not guaranteed in this process). The reference design circuit is as follows:



The above circuit has the following points to note:

1. The minimum voltage on the VDH_RTC pin is not lower than 1.62V.
2. The function of the diode is to prevent the capacitor from being reversely drained by the shutdown power source when the RTC works alone to draw power from the energy storage capacitor.
3. The diode needs to ensure the smallest possible forward voltage drop and the smallest possible reverse leakage current.
4. The capacity of the energy storage capacitor needs to be appropriately selected based on the actual duration that the RTC needs to work alone[1].

NOTE

[1]: The capacitor value needs to be calculated based on the following parameters:

1. The time of the module working alone.

2. The ambient temperature when working alone.

3. The reverse leakage current of the diode at this ambient temperature.

4. Power consumption of the RTC IO at this ambient temperature.

Please refer to the following table for high and low temperature power consumption data when the RTC IO circuit works alone:

VDH_RTC/V	Typical RTC IO current @ -40 degrees/uA	Typical RTC IO current @ 25 degrees/uA	Typical RTC IO current @ 85 degrees/uA
1.62	1.34	1.33	1.32
1.8	1.52	1.54	1.52
3.3	2.78	2.82	2.78
3.63	3.11	3.13	3.11

NOTE

Only BGA100 package has VDH_RTC pin, so only on this package can the function of RTC working independently be used.

6 I/O Pins Characteristics

6.1 Features

The following electrical properties are configurable for standard I/O pins:

- Function ID
- Internal Pull-up/Pull-down Resistor
- Driving strength
- Slew rate control
- Schmitt trigger
- Shutdown & RESET
- Open drain mode

6.2 Functional description

The I/O diagram is given in Figure 6-1. There are many kinds of I/Os in RTL8721Dx, different I/Os have different configurations.

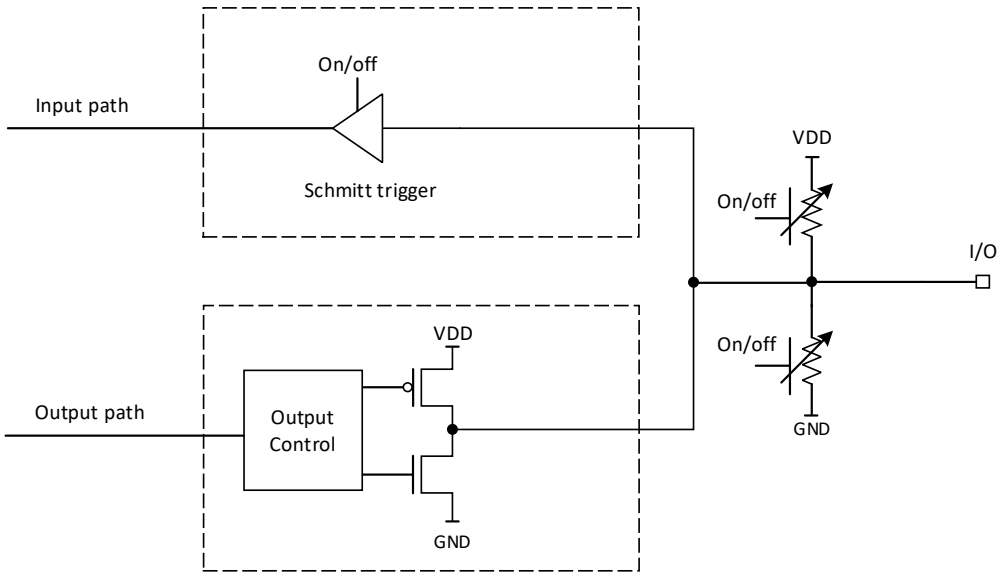


Figure 6-1 I/O diagram

6.2.1 I/O Types

All I/Os are listed in Table 6-1. The Human Body Model (HBM) of all IOs are above 3.5KV.

Table 6-1 I/O Types

Pin name	I/O power pin	Driving (mA)[1]	Internal pull resistor (ohm)[2]	Internal Pull Resistor

		1.8V (±10%)	3.3V (±10%)	Min.	Typ.	Max.	**available in deep sleep mode?**
PA0~PA11	VAH_LDOM	4/8	8/16	40K	80K	120K	Yes
PA12	VAH_LDOM	2/4	4/8	40K	80K	120K	Yes
PA13~PA18	VDH_IO1	4/8	8/16	40K	80K	120K	Yes
PA19~PA25	VDH_IO1	4/8	8/16	2.3K/25K	4.7K/50K	7.1K/75K	Yes
PA26~PA27, PA30~PB3	VDH_IO2	4/8	8/16	2.3K/25K	4.7K/50K	7.1K/75K	Yes
PA28~PA29	VDH_IO2	2/4	4/8	PU:1.1K/25K PD:10.75K	PU:2.2K/50K PD:21.5K	PU:3.3K/75K PD:32.25K	Yes
PB4~PB12	VDH_IO3[3]	4/8	8/16	2.3K/25K	4.7K/50K	7.1K/75K	Yes
PB13~PB19	VDH_IO3	2/4	4/8	40K	80K	120K	Yes
PB20~PB28	VDH_IO3	2/4	4/8	40K	80K	120K	Yes
PB30~PB31	VDH_IO3	4/8	8/16	40K	80K	120K	Yes

NOTE

1. The I/O power supported by different IOs is different, and the driving capability is related to the I/O power.

2. The pull up and pull down values of other IOs in the table are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The range is ±50%.

3. All groups support both 3.3V and 1.8V I/O power.

4. The typical voltage of VDH_IO3 can be 1.8V or 3.3V, and is related to the operating voltage of the chip. It is required to be no lower than the operating voltage of the chip.

For example, if the operating voltage of the chip is required to be 1.8V, the typical voltage of VDH_IO3 can be 1.8V or 3.3V; if the operating voltage of the chip is required to be 3.3V, the typical voltage of VDH_IO3 cannot be 1.8V, but only be 3.3V.

6.2.2 IOCTRL Register

Each I/O pin has one IOCTRL register assigned to control the pin's electrical characteristics. I/O Register base address 0x41008800. For example, the register address of PA0 is 0x41008800, the register address of PA1 is 0x41008804. The bit[4:0] field in the I/O register can be set to GPIO (typically value 00000) or a special function.

- For pins set to GPIO, the GPIO IP registers determine whether the pin is configured as input or output.
- For any special function, the pin direction is controlled automatically depending on the function.
- For specific information about PINMUX function, please refer to the PINMUX documentation.

Table 6-2 IOCTRL register

Offset	**Bit**	**Access**	**INI**	**Symbol**	**Description**
0000h	[15]	R/W	0h	gpio@_dis	IO shutdown Only when the shutdown signals of the entire group of IOs are all 1, will all the IOs of this group be disabled. 1. disable 0. enable
	[13]	R/W	0h	gpio@_sr[1]	GPIO slew rate control. 0: fast slew rate 1: low slew rate
	[12]	R/W	1h	gpio@_smt	GPIO Schmitt control
	[11]	R/W	1h	gpio@_e2	GPIO driving strength control. 0: low 1: high
	[10]	R/W	0h	gpio@_pupdc	Some GPIO may have two types of PU/PD resistors, this bit can select it. 1: small resistor 0: big resistor
	[8]	R/W	1h	gpio@_ie[2]	GPIO input enable control.
	[7:0]	R/W/ES	0h	gpio@_sel	GPIO PINMUX function id select

1. This bit is valid except for PA0-PA14.

2. This bit is only valid for PA12&PB13~PB19.

IO internal pull up and pull down are controlled by separate registers. The 32 bits of each register control the status of 32 IOs respectively. Refer to Table 6-3 for details

Table 6-3 IO pull up & pull down register

Offset	Bit	Access	INI	Symbol	Description
100h	[31:0]	R/W	40022h	PA_PU	PA0~PA31 pull up enable when system is in active.

104h	[31:0]	R/W	C0000020h	PB_PU	PB0~PB31 pull up enable when system is in active.
108h	[31:0]	R/W	0h	PA_PD	PA0~PA31 pull down enable when system is in active.
10Ch	[31:0]	R/W	0h	PB_PD	PB0~PB31 pull down enable when system is in active.
110h	[31:0]	R/W	0h	PA_PU_SLP	PA0~PA31 pull up enable when system is in sleep.
114h	[31:0]	R/W	0h	PB_PU_SLP	PB0~PB31 pull up enable when system is in sleep.
118h	[31:0]	R/W	0h	PA_PD_SLP	PA0~PA31 pull down enable when system is in sleep.
11Ch	[31:0]	R/W	0h	PB_PD_SLP	PB0~PB31 pull down enable when system is in sleep.

6.2.3 Function ID

Change the I/O function ID through gpio@_sel in Table 6-2, refer to the PINMUX documentation for details.

6.2.4 I/O Pull Resistor Control

The PU/PD of the I/O in Active & Sleep mode is controlled by the PU&PD register. Allows selection of on-chip pull-up or pull-down resistors for each pin. For Specific information, please refer to the PU&PD register table.

Pull-up and Pull-down resistor's value is different between different I/Os. The resistor value is changed by controlling the gpio@_pupdc of register table (Table 6-2). For I/Os with only one resistance value, gpio@_pupdc is not valid.

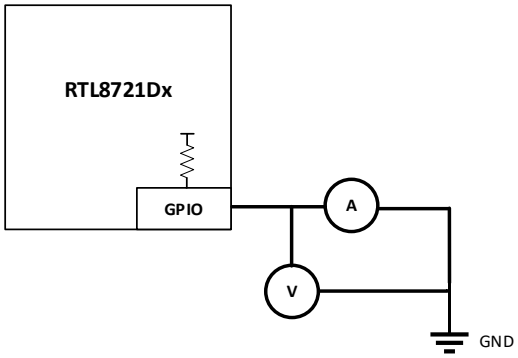


Figure 6-2 I/O Pull up resistor test

I/O pull-up resistor test procedure:
(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 1 for gpio@_pu and 0 for gpio@_pd.
(3) For GPIOs with multiple pull-up resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is V_1.
(5) According to Figure 6-2, only connect the ammeter to test. At this time, the current value is I_1, and the pull-up resistor is $R_{pu}=V_1/I_1$.

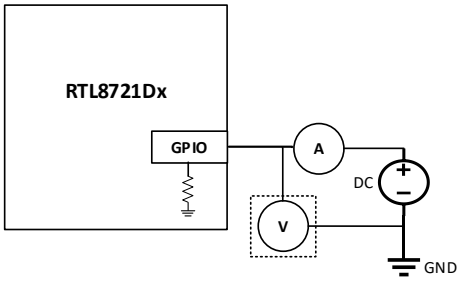


Figure 6-3 I/O Pull down resistor test

I/O pull-down resistor test procedure:
(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 0 for gpio@_pu and 1 for gpio@_pd.
(3) For GPIOs with multiple pull-down resistance values, it is necessary to change the configuration of the register gpio@_pupdc and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is 0V.
(5) According to Figure 6-3, use an external power supply to provide the same voltage (V_2) as the GPIO power, and measure the current

(I_2) at this time, and the pull-up resistor is $R_{pd}=V_2/I_2$.

6.2.5 I/O Driving Strength

The I/O driving strength can be configured through gpio@_e2 in the IOCTRL register. I/O driving strength is different between different I/O types.

GPIO output high driving strength test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.85*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2.
(4) I_{HIGH} is the driving strength of GPIO output high.

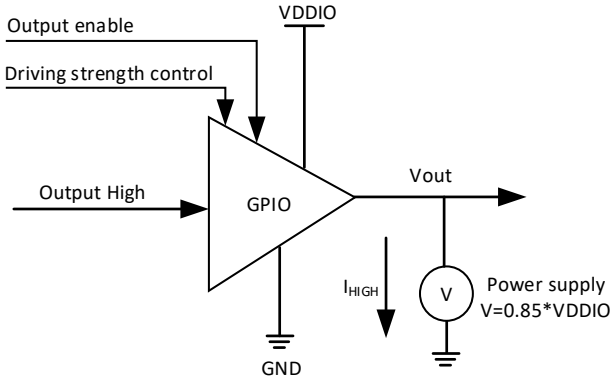


Figure 6-4 GPIO output high driving strength test

GPIO output low driving strength test procedure:

(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.15*VDDIO.
(3) Set the driving Strength to high or low through gpio@_e2.
(4) I_{LOW} is the driving strength of GPIO output Low.

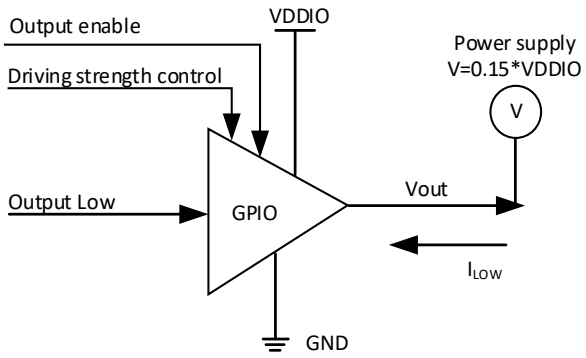


Figure 6-5 GPIO output low driving strength test

6.2.6 I/O Schmitt Trigger

The I/O pin contains a schmitt trigger as a digital function, which can be selectively disabled by setting gpio@_smt in the IOCTRL register. The specifications of the schmitt trigger are shown in Table 6-4.

Table 6-4 Digital IO pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIL	IO input low level voltage	VIO=1.8V±10%	-0.3	-	0.35*VIO	V
		VIO =3.3V±10%	-0.3	-	0.8	
VIH	IO input high level voltage	VIO=1.8V±10%	0.65* VIO	-	-	
		VIO=3.3V±10%	2	-	-	
VOL	IO output Low level voltage	VIO=1.8V±10%,IOL Max	-	-	0.15*VIO	
		VIO=3.3V±10%,IOL Max	-	-	0.15*VIO	

VOH	IO output high level voltage	VIO=1.8V±10%,IOH Max	0.85*VIO	-	-	
		VIO=3.3V±10%,IOH Max	0.85*VIO	-	-	

NOTE

- *VIO is the power supply for IO pin.*
- *If the Schmitt trigger is disabled in IOCTRL register, VIH=VIL=0.5*VIO.*
- *Refer to Table 6-1 for IO driving strength.*

6.2.7 Slew Rate Control

Each IO port of RTL8721Dx has independent slew rate control function except for PA0~PA14. Refer to Table 6-2 for specific control settings. Different slew rate control settings will mainly affect the rise/fall time corresponding to IO port output high/low. When the user's application scenario is sensitive to EMI and there is a problem with the default setting (faster rise/fall time), users can adjust the slew rate corresponding to the IO port to a low gear (slower rise/fall time).
Please refer to for the impact of different slew rate settings on rise/fall time under the same external loading conditions.

Table 6-5 Effect of different slew rate settings on rise/fall time

Pin name	**Conditions**	**Rise/fall time typical value(ns)**			
		SR =0 IO power = 3.3V	SR =0 IO power = 1.8V	SR =1 IO power = 3.3V	SR =1 IO power = 1.8V
PA0~PA11	Loading of IO port = 15pF	0.7/0.7	1.2/1.2	-	-
PA12		1.4/1.4	2.6/2.5	4.1/4.2	8.3/9.0
PA13~PA18		0.7/0.7	1.3/1.3	5.0/4.8	10.9/10.9
PA19~PA25		0.8/0.9	1.5/1.4	4.7/4.8	10.2/10.9
PA26~PA27		0.8/0.9	1.5/1.4	4.7/4.8	10.3/11.0
PA28~PA29		1.2/1.3	2.2/2.3	4.3/4.5	8.8/9.6
PA30~PB3		0.8/0.9	1.5/1.4	4.7/4.8	10.2/10.9
PB4~PB12		0.8/0.9	1.5/1.4	4.7/4.8	10.2/10.9
PB13~PB19		1.4/1.4	2.6/2.5	4.1/4.2	8.3/9.0
PB20~PB28		1.4/1.4	2.6/2.5	4.1/4.2	8.3/8.9
PB30~PB31		0.8/0.9	1.5/1.4	4.7/4.7	10.2/10.8

NOTE

When setting the SR of the IO port to 1 (slower level), the timing of all functions will not be guaranteed.

6.2.8 I/O Shutdown & RESET

The power of I/O can be shut down through the GPIO_BIT_SHUT_DOWN bit in the IOCTRL register. You can use this function to conserve power.
For I/O shutdown, only when the whole group I/O shut down signals are all 1, the I/O SHDN will pull down to shut down the group I/O. Customer can also directly control the Group shutdown register and directly control the I/O shutdown of this group. For Specific information, please refer to the I/O SHDN&RSTB register table.

- When RSTB is set to 0, the I/O is in tri state. At this time, the level of the I/O is determined by the external pull-up and pull-down. If the external pull-down is connected, the I/O level is low. If the external pull-up is connected, the I/O level is high.
- When SHDN=1 and RSTB=1, the PU/PD state of the I/O is determined by register configuration.
- When RSTB=1, SHDN changes from 1 to 0, the state of I/O will latch the current state. At this time, the change of the I/O pull-up/pull-down register will not change the state of the I/O pull resistor.

Table 6-6 I/O Shutdown & RESET register

Address	**Bit**	**Access**	**INI**	**Symbol**	**Description**
0x41008000	[25]	R/W	0	LPGPIO_RSTB	1: Release LP I/O RSTB33 (except Group 5) 0: Global Assert LP I/O RSTB33
	[24]	R/W	0	LPGPIO_SHDN	1: Global Enable LP I/O (except Group 5) 0: Shutdown LP I/O
	[21]	R/W	1	GROUP_5_RSTB	1: Enable group 5 I/O 0: Reset group 5 I/O
	[20]	R/W	1	GROUP_4_RSTB	1: Enable group 4 I/O 0: Reset group 4 I/O
	[19]	R/W	1	GROUP_3_RSTB	1: Enable group 3 I/O 0: Reset group 3 I/O

	[18]	R/W	1	GROUP_2_RSTB	1: Enable group 2 I/O 0: Reset group 2 I/O
	[17]	R/W	1	GROUP_1_RSTB	1: Enable group 1 I/O 0: Reset group 1 I/O
	[16]	R/W	1	GROUP_0_RSTB	1: Enable group 0 I/O 0: Reset group 0 I/O
	[13]	R/W	0	GROUP_5_SHDN	1: Enable group 5 I/O 0: Shutdown I/O Note: AON PMC will auto release this bit in power on init seq.
	[12]	R/W	1	GROUP_4_SHDN	1: Enable group 4 I/O 0: Shutdown I/O
	[11]	R/W	1	GROUP_3_SHDN	1: Enable group 3 I/O 0: Shutdown I/O
	[10]	R/W	0	GROUP_2_SHDN	1: Enable group 2 I/O 0: Shutdown I/O
	[9]	R/W	1	GROUP_1_SHDN	1: Enable group 1 I/O 0: Shutdown I/O
	[8]	R/W	1	GROUP_0_SHDN	1: Enable group 0 I/O 0: Shutdown I/O

NOTE

- *GROUP_0: PA0~PA12*
- *GROUP_1: PA13~PA25*
- *GROUP_2: PA26~PA31 & PB0~PB3*
- *GROUP_3: PB4~PB12*
- *GROUP_4: PB13~PB28*
- *GROUP_5: PB30~PB31*

6.2.9 Open Drain Mode

The I/O is default to push pull mode, and can be configured to implement open drain mode. For more details, refer to the software APIs.

6.3 I/O Pins Internal Pull Resistor Control Configuration

Each I/O has an Internal Pull-up and Pull-down Resistor. Please refer to section 6.2 for details. This section describes how to configure it. During the process of boot, sleep and deep-sleep, I/O pull control is needed, and the chip will load the I/O internal pull status of each I/O from the “pinmapcfg.c” file.

The correct configuration of pinmap can achieve low power consumption. Otherwise, the unsuitable configuration may lead to leakage.

Principles for I/O internal control configuration:

1. If the I/O is not used, it is recommended to set it to pull down.
2. If I/O is used as input, it cannot be left floating. please refer to the following chapters for configuration of different functions.
3. If I/O is used as output, please refer to the following chapters for configuration of different functions.

In the SDK, customers should set the internal pull status of I/O according to the above rules.

In the “pinmapcfg.c” file, PMAP_TypeDef pmap_func[] should be configured. In which,

- Pin Name: indicates the I/O.
- Func PU/PD: is used to configure the I/O internal pull status when the IC is in active mode.
- Slp PU/PD: is used to configure the I/O internal pull status when the IC is in sleep mode.

The following configuration is only applicable to RTK EVB, and customers need to configure it according to the external circuit.

```
const PMAP_TypeDef pmap_func[] = {
//Pin Name          Func PU/PD                Slp PU/PD
    {_PA_0,         GPIO_PuPd_UP,             GPIO_PuPd_UP},          //
    {_PA_1,         GPIO_PuPd_UP,             GPIO_PuPd_UP},          // flash cs pin
    {_PA_2,         GPIO_PuPd_KEEP,           GPIO_PuPd_UP},          //
    {_PA_3,         GPIO_PuPd_KEEP,           GPIO_PuPd_UP},          //
    {_PA_4,         GPIO_PuPd_KEEP,           GPIO_PuPd_UP},          //
    {_PA_5,         GPIO_PuPd_KEEP,           GPIO_PuPd_KEEP},        //
    {_PA_6,         GPIO_PuPd_DOWN,           GPIO_PuPd_DOWN},        //
    {_PA_7,         GPIO_PuPd_DOWN,           GPIO_PuPd_DOWN},        //
    {_PA_8,         GPIO_PuPd_KEEP,           GPIO_PuPd_DOWN},        //
    {_PA_9,         GPIO_PuPd_DOWN,           GPIO_PuPd_DOWN},        //
    {_PA_10,        GPIO_PuPd_DOWN,           GPIO_PuPd_DOWN},        //
```

```
    {_PA_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_12,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_13,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_14,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_15,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_16,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_17,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_18,        GPIO_PuPd_UP,           GPIO_PuPd_UP},          // flash cs pin
    {_PA_19,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_20,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_21,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_22,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_23,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_24,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_25,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_26,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_27,        GPIO_PuPd_KEEP,         GPIO_PuPd_DOWN},        //
    {_PA_28,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_29,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_30,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PA_31,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_0,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_1,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_2,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_3,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_4,         GPIO_PuPd_UP,           GPIO_PuPd_UP},          // log_RX sleep need pull up
    {_PB_5,         GPIO_PuPd_UP,           GPIO_PuPd_UP},          // log_TX sleep need pull up
    {_PB_6,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_7,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_8,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_9,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_10,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_12,        GPIO_PuPd_NOPULL,       GPIO_PuPd_NOPULL},      //
    {_PB_13,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_14,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_15,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_16,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_17,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_18,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_19,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_20,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_21,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_22,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_23,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_24,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_25,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_26,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_27,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_28,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_29,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},        //
    {_PB_30,        GPIO_PuPd_UP,           GPIO_PuPd_UP},          //
    {_PB_31,        GPIO_PuPd_UP,           GPIO_PuPd_UP},          //
    {_PNC,          GPIO_PuPd_KEEP,         GPIO_PuPd_KEEP},        //table end
};
```

There are four states of the I/O.

- GPIO_PuPd_UP: Indicates that the I/O is through the internal resistor pulled up to VDDIO.
- GPIO_PuPd_DOWN: Indicates that the I/O is through the internal resistor pulled down to GND.
- GPIO_PuPd_NOPULL: Indicates that the I/O does not have an internal pull-up or pull-down configured.
- GPIO_PuPd_KEEP: Indicates that the I/O will maintain the last status.

The following section illustrates the recommendation of I/O status configurations according to the function of different pins.

6.3.1 Normal GPIO

When a pin is used as a normal GPIO connecting with external circuit, the GPIO PU/PD status depends on the state of the external circuit. If the GPIO is used to driver LED, and pin status is 'External pull up', the GPIO status need to be 'PULL UP' in sleep and DSLP mode. Configure the state of the internal PU/PD according to the GPIO external circuits.

Table 6-7 Normal GPIO status

I/O type	Pin status	Active PU/PD	Sleep PU/PD
Input	External Pull UP	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP / GPIO_PuPd_NOPULL
Input	External Pull Down	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL
Input	Floating	GPIO_PuPd_DOWN	GPIO_PuPd_DOWN
Output	Output High	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP
Output	Output Low	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN

6.3.2 LOGUART Pin

The pins PB4 and PB5 are LOGUART function by default. The I/O status are listed in Table 6-8.

Table 6-8 LOGUART I/O status

Pin function	Pin name	Func PU/PD	Sleep PU/PD
UART_LOG_RXD	PB4	GPIO_PuPd_UP	GPIO_PuPd_KEEP
UART_LOG_TXD	PB5	GPIO_PuPd_UP	GPIO_PuPd_KEEP

6.3.3 ADC & Cap-touch Pin

For PB13~PB19, if customer need to configure it for ADC or cap-touch function, customers need to configure IE to 0 first (please refer to Table 6-2), and configured as internal no pull.
If the customer needs to configure other functions, IE needs to be set to 1. For other configurations, please refer to 6.3.1.

6.3.4 SWD Pin

The pins PA30 and PA31 are SWD function by default. The I/O status are listed in Table 6-9.

Table 6-9 SWD I/O status

Pin function	Pin name	Func PU/PD	Sleep PU/PD
SWD_DATA	PA31	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SWD_CLK	PA30	GPIO_PuPd_UP	GPIO_PuPd_KEEP

NOTE

PA30&PA31 is the SWD function by default. If they need to be used as GPIOs or other functions, besides switching the PINMUX function ID, users also need to set 0x410089F4[0] = 0.

6.3.5 Flash Pin

When a pin is configured as SPI_FLASH function, the I/O status is listed in Table 6-10.

Table 6-10 Flash I/O status

Pin function	Func PU/PD	Slp PU/PD
SPI_DATA_X	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CS	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CLK	GPIO_PuPd_DOWN	GPIO_PuPd_KEEP

6.4 I/O Pins Output Description

If customers need to use I/O to drive other devices, such as LEDs, they should first set the I/O to output 1 or 0, and then set the I/O to output mode. Because if you set the I/O to output mode without first setting output 1 or 0, the I/O will output 0 first, which may cause the LED light

to flash due to the incorrect status of the I/O output.
After the system enters sleep mode (PG or CG), the status of the I/O output will maintain the status before sleep. For example, before sleep, the I/O is set to output 1. After the system enters PG or CG, this I/O will still remain output 1 unchanged.
However, if the system enters deep sleep, the status of the I/O output set under active will become invalid. For example, if the I/O in active is set to output 1, and the system enters deep sleep, the I/O will not be able to maintain the output 1 state.

7 PINMUX Instructions

7.1 Introduction

RTL8721DX provides a PINMUX circuit to maximize the user's freedom of use under limited pin-out conditions. Each pin can be connected to different internal IP circuits through configuration. For the specific correspondence between each pin and IP circuit, refer to the provided PINMUX document.
Before users apply the chip for further development, please read the following precautions about PINMUX to avoid inconvenience due to unexpected behavior.

7.2 Trap Pins

When users power on the chip, the internal circuit will latch several pins conditions to decide whether enter into different mode. The trap pins and their descriptions are as below.

Table 7-1 Trap pin description and precautions

Pin name	Trap pin name	Active level	Descriptions	Note
PB31	TM_DIS	Low	Enter test mode (Internal use).	Please make sure that the pin is in the pull-up state during normal use.
PB5	UD_DIS	Low	Enter flash download mode	Download flash content in this mode through LOGUART.
PB30	OTP_DIS	Low	Load OTP settings	Please make sure that the pin is in the pull-up state during normal use.

NOTE

The Trap pin needs to select the external pull-up and pull-down voltages according to the IO power supply.

7.3 Wake Pins

PB30 and PB31 are directly connected to the wake up circuit which is used to wake up system from deep-sleep state. When users need to use other functions on this pin, please disable the wake up function.

7.4 Special pin

PA12 is a special pin in process of use. If the chip embedded a 1.8V flash or psram, then PA12 can only work at 1.8V, and all functions that use PA12 can only work at 1.8V. If the chip embedded a 3.3V flash, then PA12 can only work at 3.3V, and all functions that use PA12 can only work at 3.3V.

7.5 Function Mux

7.5.1 Function ID 0-18

For functions whose ID number among 0-18, each pin can only be connected to a fixed signal of a certain IP. The functions that can be configured on each pin are very limited, but a dedicated design can maximize the performance of each IP.

NOTE

For example, function id 8 and function id 29-32 are both SPI functions. Since function id 8 is a dedicated pin, the maximum speed of the SPI function reaches 50MHz (Master mode). And the maximum speed of the pins (full-cross pins) corresponding to function id 29-32 is only 25MHz(Master mode).

Take PB31 as an example. If users configure function ID of PB31 to 1, then the pin will be directly connected to the UART1_TXD signal of the

UART1 IP via PINMUX. Please refer to the PINMUX document for the specific function distribution available on each pin.

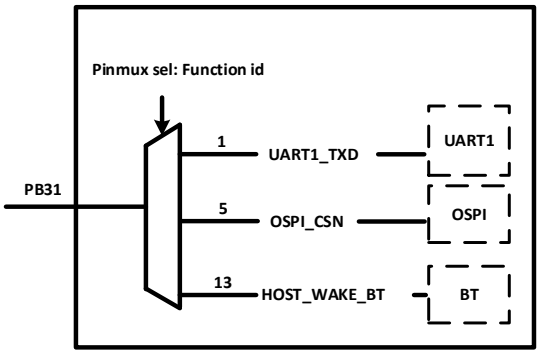


Figure 7-1 Schematic diagram of PINMUX connection of PB31

7.5.2 Function ID 19-81

For functions whose ID number is after 19, each pin can be connected to different signals of a certain IP. This method maximizes the freedom of use, but the scope of use and some IPs' performance (max transfer speed) is limited.

NOTE

These function IDs can only be configured in PA6-PA31, PB0-PB11 and PB13-PB31.

Take PA6 as an example. According to the PINMUX document, users can connect PA6 with the UART0_TXD signal of UART0 by configuring the PA6 function ID as 19. Users can also configure the PA6 function ID as 20, and connect PA6 with the UART0_RXD signal of UART0. For details, please refer to the PINMUX documents.

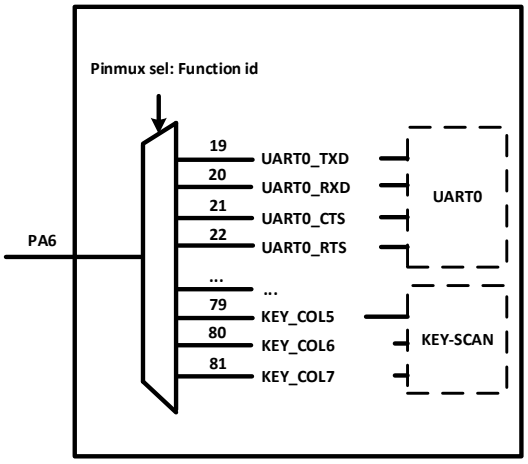


Figure 7-2 Schematic diagram of PINMUX connection of PA6

7.6 PINMUX Signal Descriptions

For all signal descriptions, please refer to PINMUX-SPEC for detailed information.

8 Audio

8.1 DMIC-in

Digital microphone (DMIC) records audio data. It is integrated with ADC internal, and can directly output digital signal. DMIC-in supports mono mode and stereo mode.

8.1.1 DMIC-in Mono Mode

Tie the L/R of a digital microphone to ground or VDD if only one digital microphone is placed.

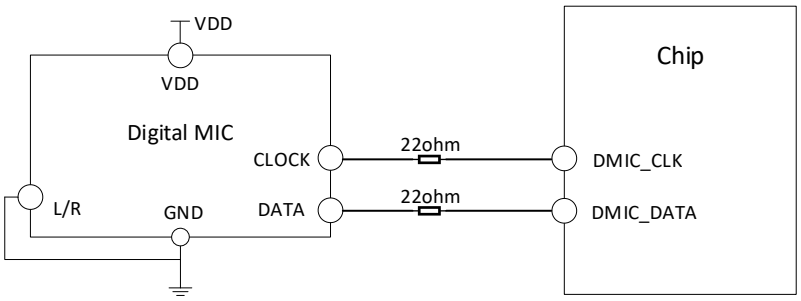


Figure 8-1 DMIC-in mono mode connection

For layout design, DMIC_CLK and DMIC_DATA should add ground isolation on both sides of the routing.

Figure 8-2 DMIC-in layout

8.1.2 DMIC-in Stereo Mode

Tie the L/R of two digital microphones to ground and VDD respectively if a stereo microphone is needed. The two microphones share the DMIC_DATA according to the rising/falling edge. DMIC_CLK and DMIC_DATA layout design refer to Figure 8-2.

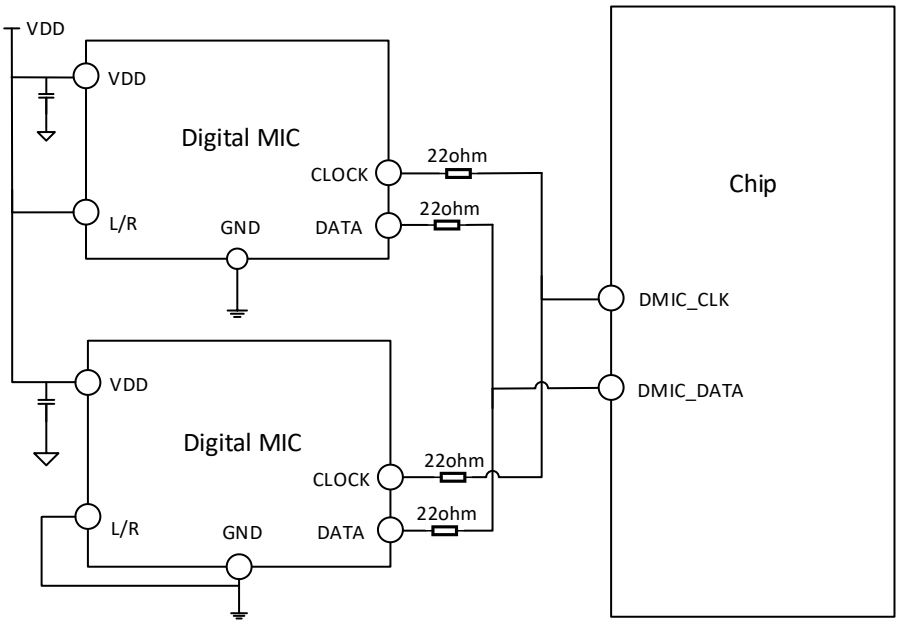


Figure 8-3 DMIC-in stereo mode connection

8.2 I2S

Reserve 0R resistors on the clock and data paths of I2S. If layout space allows, increase ground isolation for clock and data as much as possible.

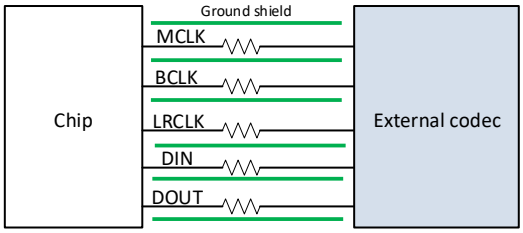


Figure 8-4 I2S layout

9 General Purpose ADC

The General purpose ADC (GP-ADC) and Capacitive Touch Sensor multiplexes pin. The signal sampling of Capacitive Touch Sensor itself is also done through GP-ADC, and both of them are sensitive analog signal sensors, so we need to pay special attention to interference.

9.1 Net Arrangement

GP-ADC has multiple channels that use a set of fixed pins of IC. Care should be taken to avoid using GPIO in the same group of GP-ADC as high-speed signal ports (I2C, SPI, etc.), as shown in Figure 9-1. If unavoidable, it is necessary to set it reasonably on the software to ensure that the high-speed signal has no action while GP-ADC sampling.

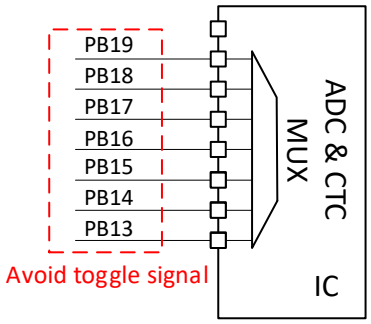


Figure 9-1 GP-ADC net arrangement

In addition, even if the high-speed signal is not arranged in the same set of the GP-ADC GPIO, it should not be arranged adjacent to the pin of the GP-ADC.

9.2 Input impedance

In order to measure the voltage of 0 to 3.3V, a voltage divider is added to the front end of the GP-ADC. The resistance is fixed and cannot be modified, and the accurate resistance value can be obtained by reading the calibration value written in each IC.

Due to the divider resistor, the input resistance of the GP-ADC will be affected by it, and the typical value is 491kohm. It is necessary to pay attention to this situation in application. Take Figure 9-2 as an example, when the external resistance R2 of GP-ADC is about equal to the internal resistance R, there will be a deviation in the voltage collected by GP-ADC. If R2 is a thermistor, the temperature measurement may be inaccurate.

NOTE

Some products GP-ADC contain a battery dedicated channel for battery voltage detection, which receives 5V input voltage, the internal input resistance is about 150 kohm, and it is not calibrated. In application, it is noted that the source resistance should be much less than 150 kohm.

Therefore, when designing the external circuits, we should consider:

(1) R2 should be sufficiently small (less than 1 / 100 of R) to minimize the impact of internal resistance.

(2) If the requirements (1) cannot be met, the Rin value of the IC can be obtained through the API and incorporated into the circuit design.

Typically GP-ADC normal channel are used to measure the voltage of different sensor, such as NTC thermistor. The simplified block is as follows:

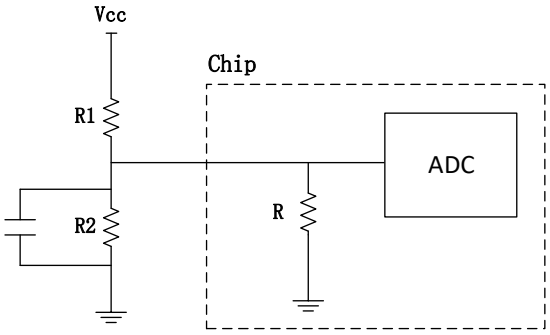


Figure 9-2 simplified application block

There is a 500 kohm resistor to ground inside the chip which will affect the accuracy of GP-ADC with the combination of peripheral circuit. The ideal input voltage to GP-ADC is:

$$V_{\text{ideal}} = V_{\text{cc}} \times R_2 / (R_1 + R_2) = 3.3 \times \frac{R_2}{R_1 + R_2}$$

But the actual input voltage to GP-ADC is:

$$V_{\text{actual}} = V_{\text{cc}} \times \frac{R_2 // R}{R_2 // R + R1} = V_{cc} \times \frac{R_2}{R_2 + R_1 \times R_2 / R + R_1}$$

Compare the two formals, Vactual is smaller than Videal due to the impact of internal R. And the greater the ratio of R1xR2/R is, the greater the error between Vactual and Videal is. What's more, the resistance of internal R vary differently in multi chips which also can impact the accuracy.
For better accuracy, internal R should be calculated and its resistance value will be stored in OTP.

After calibration, if R2 is NTC thermistor, the actual resistance of R2 is:

$$R_2 = \frac{R_1 \times V_{\text{adc}}}{V_{cc} - V_{adc} - V_{adc} \times \frac{R_1}{R}}$$

By the way, it's optional for customers to choose another GP-ADC channel to measure the voltage of Vcc, which can reduce the impact that Vcc changes while GP-ADC Vref doesn't change:

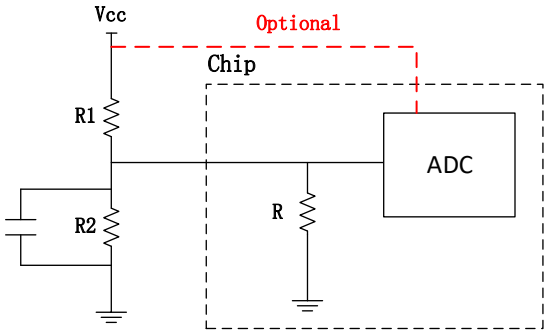


Figure 9-3 Optional application block

(3) R will be connected to the circuit only when the GP-ADC is sampling. Therefore, at the moment when the ADC sampling is turned on, the circuit will be switched, and the parallel C of R2 may slow the transient process of the circuit. There are usually two ways to solve this problem:
   a) When the requirement for sampling rate is not high, it can be sampled at intervals, and the interval time needs to exceed the circuit time constant. In this case, the instantaneous value of sampling is the voltage at the beginning of switching, that is, the voltage of the capacitor C. in this case, the circuit design requires that C be greater than 10nF.
   b) when the sampling rate is strict and interval sampling is not acceptable, a delay can be added before each sampling of a group of

data, which should be greater than 5 times the circuit time constant, and pay attention to clear the conversion result FIFO before reading the data.

9.3 ADC Calibration Principle

To improve the linearity of the input / output characteristics of the ADC, each IC will implement a nonlinear calibration of the ADC in the factory. With the nonlinear calibration, the gain and offset error of the ADC can also be reduced.The user can use the API to directly obtain the exact voltage conversion results that have been calibrated.

After calibration, each IC can find its own value of A, B and C and store them in one time program (OTP). The A and C are stored in the form of binary complement, while B is stored as an unsigned integer. When acquiring ADC code, use the following formula to get the current voltage with unit as mV, here parameter x is ADC code:

$$y = ax^2 + bx + c = \left(\frac{A}{2^{26}}\right)x^2 + \left(\frac{B}{2^{15}}\right)x + \left(\frac{C}{2^{6}}\right)$$

For example, if A, B, and C read from OTP are 0xff66, 0x6f91, and 0x53f, and ADC code is 1800. The original A is 0x809a, parameter a = -(0x9A)/2^26, parameter b = (0x6f91)/2^15, and parameter c = (0x53f)/2^6. So, the current voltage y = 1582mV.

Users can obtain the calibrated results directly through API: ADC_GetVoltage or ADC_GetVBATVoltage.

10 Capacitive Touch Sensor

10.1 Net Arrangement

- It is not recommended to reuse Capacitive Touch Sensor pins with other functions. High-speed signal lines (I2C, SPI, etc.) should not appear in the same group of Capacitive Touch Sensor pins. If unavoidable, it needs to be set reasonably on the software to ensure that Capacitive Touch Sensor works with no high-speed signal action
- It is suggested to keep the Capacitive Touch Sensor away from high speed signal and switching power net
- To prevent crosstalk, if only some Capacitive Touch Sensor channels are used, select channels at intervals and disable unselected channels
- Do not design a pull-up or pull-down voltage on the signal line
- Do not design bypass capacitors on the signal line

NOTE

Capacitive Touch Sensor's layout has a great impact on performance. For specific layout rules, please refer to layout guide.

10.2 Series Resistance

A resistor is connected in series in each Capacitive Touch Sensor channel (placed near the chip). This resistor and the parasitic capacitance on the signal path form a simple RC filter, which can partially filter out the noise interference and improve the ESD resistance. Due to the different circuit design, the resistance usually can not be accurately selected. The filter effect is poor when the resistance is too small, and the sensitivity is reduced because the resistance is too large. It is recommended to choose a resistance of 47-560 ohms.

In addition to using series resistance to improve ESD resistance, the TVS of each sensor channel should be connected in parallel to attenuate the impact of surge current on the sensor, but the junction capacitor of this TVS should not exceed 0.6 pF.

10.3 Button LED Design

When the button is made into a hollowed-out type, a LED can be added in the middle, and the light and darkness of the LED can be used to judge the situation of touching and leaving the finger. It is suggested that the power supply of LED should add RC filter to slow down the change rate of the level edge.

10.4 Max input Voltage

The Capacitive Touch Sensor is an analog circuit, an ADC sample the input net continuously. The max input voltage of the input net is 0.85V. In particular, the use of too large Mbias can cause a charging voltage exceeding 0.85V, which may cause damage to the ADC.

11 Flash SPI

11.1 Introduction

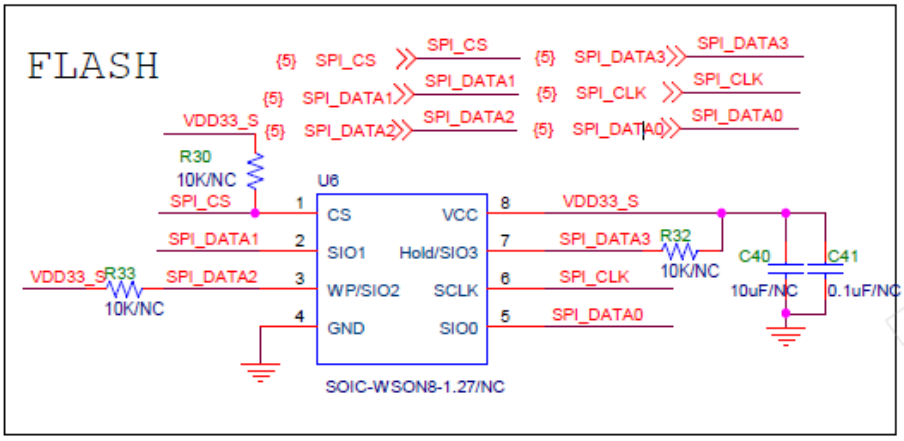
The SPIC is used to communicate with SPI Flash Devices (Flash). Flash SPI can only be configured as master with Max. Baud rate: 100MHz.

11.2 Flash Selection Requirements

- Some chips with MCM PSRAM package require external flash to function properly. For chips with MCM flash package, if users have a requirement for dual flash usage, external flash should also be connected.
- The applicable flash is divided into two operating gears: 3.3V and 1.8V. The operating voltage range that 3.3V flash must cover is 2.97V~3.63V, and the working voltage range that 1.8V flash must cover is 1.71V~1.89V.
- Users must pay attention to the t_{VSCL} symbol of the flash power-on timing, and the time from the power on of the flash to the start of operation cannot be longer than the time from the power on of the IC to booting of IC.

11.3 Schematic Reference Design

- Suggest CS pin reserving a 10K pull-up resistor so that the CS pin has a certain high level state to avoid bus floating.
- For dual SPI and standard SPI mode，suggest WS pin reserving an pull up 10K resistor so that the WS pin has a certain high level state to avoid bus floating.
- For dual SPI and standard SPI mode，suggest Hold pin reserving an pull up 10K resistor so that the Hold pin has a certain high level state to avoid bus floating.
- Vcc requires a filtering capacitor connected to ground, usually one large and one small capacitor connected in parallel, such as 10μF and 0.1μF.



12 I2C

12.1 Introduction

The I2C has the following features:

- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three speed modes:
  - Standard Speed (SS), up to 100Kbps
  - Fast Speed (FS), up to 400Kbps
  - High Speed (HS), up to 3.4Mbps and up to 1.7Mbps
- Master or Slave I2C operation

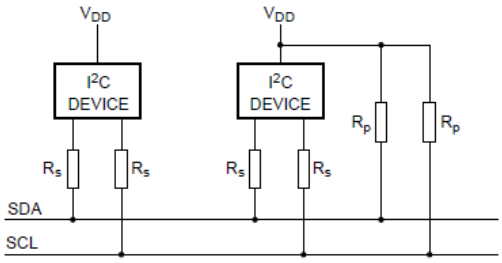
12.2 Schematic Reference Design

- Part of the pads used for I2C can switch to 4.7K pull-up resistor internally (PA19~PA27, PA30, PA31, PB0~PB12). However, the internal pull-up resistance value of other pads is too large and not suitable for I2C communication. Suggest users to reserve pull-up resistors externally to adjust the resistance value according to their own needs.
- Different speed modes have requirements for the maximum allowable load of the I2C bus. In standard , fast and 1.7M high speed modes, the bus load cannot exceed 400pF, and in 3.4M high speed mode, the bus load cannot exceed 100pF.
- Calculation method for pull-up resistance of I2C bus:

  The voltage value of IO Power determines the minimum value of pull-up resistance. When IO Power is 3.3V, the minimum allowable value of pull-up resistance is 1K, and when IO power is 1.8V, the minimum allowable value of pull-up resistance is 0.5k. The size of the bus load determines the maximum allowable pull-up resistance, and the calculation formula is as follows:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

  In the formula, t_r represents the maximum signal rise time allowed under different speed modes (Standard: 1000ns, Fast: 300ns, High Speed: 80ns), and C_b represents the bus load.
- The I2C protocol also defines resistors Rs connected in series on SDA and SCL lines. The function of this resistor is to effectively suppress interference pulses on the bus from entering the slave device and improve reliability. The selection of this resistor is generally around 100~200 Ω. This resistor is not necessary and can be used in harsh noise environments.



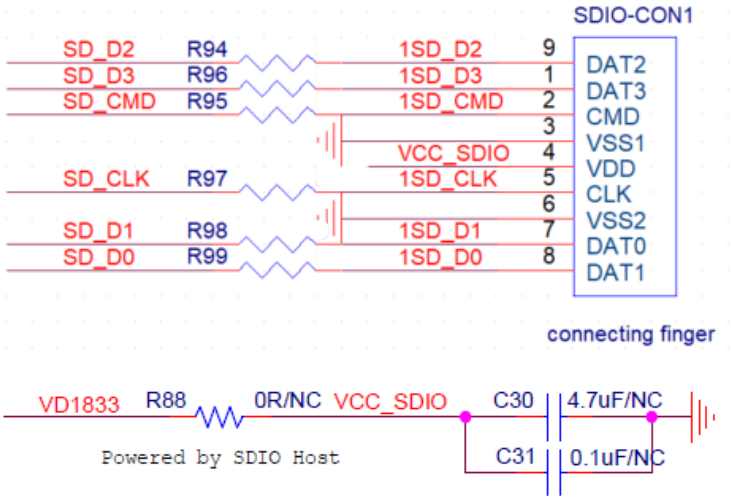
13 SDIO Device

13.1 Features

- Full compliance with SDIO card specification version 2.0.
- Support SDIO clock up to 25/50MHz
- Support 4 bits I/O mode.
- Dedicated DMA engine for data transfer to reduce CPU loading.

13.2 Schematic Reference Design

- VCC_SDIO requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7μF and 0.1μF.
- Suggest users to connect a resistor in series on the clock, cmd, and data lines. The customer can improve signal quality by adjusting the resistance value.



14 General SPI

14.1 Introduction

- The chip supports Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol.
- Master or slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps

NOTE

1. When the chip is configured as Master, SPI supports transmission with a maximum baud rate of 50Mbps. But when the chip is configured as Slave, whether it can support a maximum baud rate of 50Mbps is controlled by the connected master. Due to the path delay and pad delay of internal signals in the master and slave devices, as well as some delays that may be introduced by pads or PCBs, the connected master needs to support delayed sampling function in order to correctly receive data sent by the slave at 50Mbps baud rate.

2. Dedicated SPI has many groups and does not allow cross group use between signal lines.

14.2 Schematic Reference Design

Generally, four signal wires(CS, CLK, MISO, and MOSI) can be directly connected to external device. You can pull CS pin up to Vcc by a 10K resistor, so that the CS pin has a certain high level state to avoid bus floating.

15 SWD

15.1 Introduction

Debug Interface supports Arm® standard bi-directional Serial Wire Debug (SWD) to pass data to and from the debugger and the target system in a highly efficient and standard way. It provides a probe interface consisting of two signals—TCK and TMS. The TMS signal is bidirectional and carries control information to the adapter and data in both directions. The TCK signal(max baud rate: 20MHz) is sourced from the probe.

15.2 Schematic Reference Design

- Suggest ground shielding between SWDCLK and SWDIO signal traces to avoid signal crosstalk.
- It is recommended to connect a 22R damping resistor in series at the source of both SWDIO and SWDCLK signals to suppress signal reflection.
- It is recommended to connect one ESD protection device in parallel on each of the SWDIO and SWDCLK signal traces, as manual hot swapping is required during debugging.
- According to the SWD standard, it is recommended to configure the SWD data pad to pull-up state after power on.

NOTE

Port PA30 and port PA31 are default configured as SWD interface but users can configure relevant register to switch these two ports to other functions. If users use PA30 and PA31 for other functions except SWD and connect the two ports to external circuits, users must avoid SWD toggle behavior with a risk of misidentification before switching off the SWD function from the two ports.

16 USB

16.1 Pad Configuration

1. Pin mux to USB function
2. Pad is configured as no pull mode

16.2 Feature

- Full speed only
- Device mode only

16.3 The Type of Interface

16.3.1 Type A

The DP/DM can be directly connected

Figure 16-1 USB type A interface

16.3.2 Type-C

- DP1/DP2 short, DN1/DN2 short;
- CC1/CC2 pulls down the resistor by 5.1kohm respectively

NOTE

See figure 14-3 for the schematic design requirement.

16.3.3 Micro USB

The DP/DM can be directly connected

Figure 16-2 USB micro interface

16.4 Schematic Design Requirements

1. Add 10uF power filter capacitor to VBUS to prevent the instantaneous voltage of VBUS from being too large due to plugging and unplugging, and place it close to the USB interface;
2. Electrostatic protection: In order to prevent static electricity from damaging the connector signal, hang ESD devices on DP/DM/VBUS/ID, pay attention to device selection, and place them close to the USB interface;
3. The resistor of the data line is connected in series to prevent the internal resistance damage caused by the micro interface D+/D- mistake and VBUS short, the resistance value is generally 2.5ohm, placed close to the USB controller, if the interface is type A or C, this resistor can be replaced with 0 ohm without placement;
4. The SHIELD is grounded by a resistor-capacitor network. This helps isolate the signal and reduces EMI and RFI emissions. Try to place the resistor close to the USB connector.

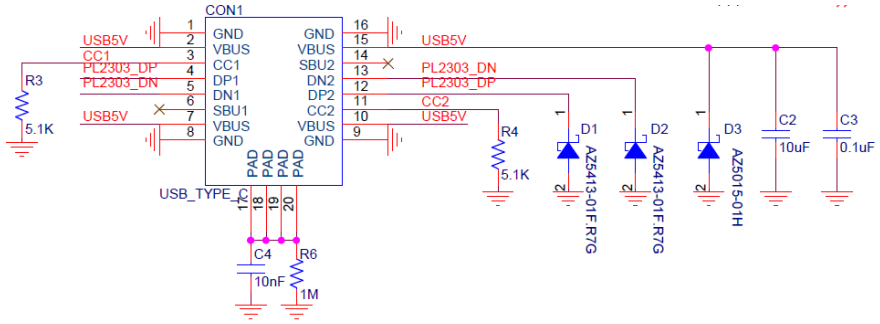
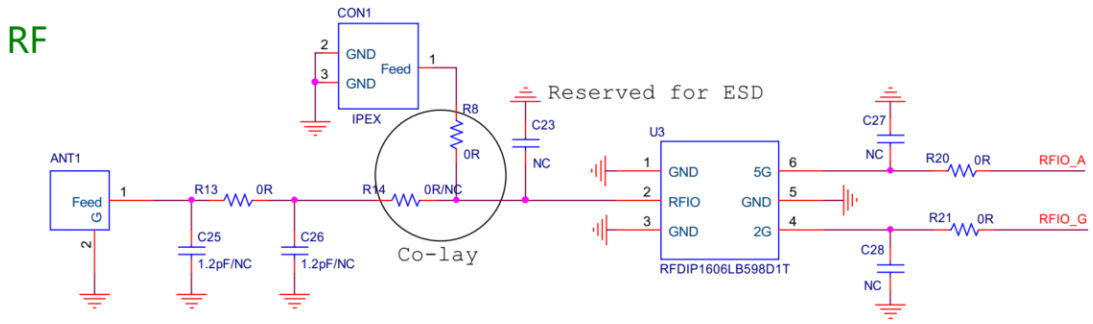


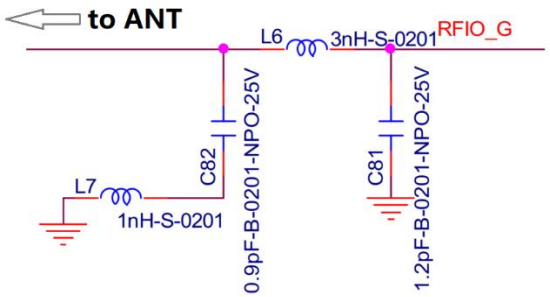
Figure 16-3 USB type-C interface

17 RF Circuit

- Diplexer (U3) is needed for combining RFIO_A (5G) and RFIO_G (2.4G).
- L-shape or Pi-shape matching (C27/R20 and C28/R21) should be placed between diplexer and main IC to tune RF impedance and harmonics rejection.
- A TVS (C23) is reserved for ESD protection.
- R8 and R14 is co-lay in our HDK for selecting RFIO path to RF connector (CON1) or printed antenna (ANT1).
- Pi-shape circuit (C26/R13/C25) is reserved for antenna matching.
- You can add a RF test point between R14 and U3 for RF test in mass production.



- If you need only single band of the chip (2.4G only or 5G only), pi-shape low pass filter as follows is recommended to be placed at RFIO pin to suppress Tx harmonics.

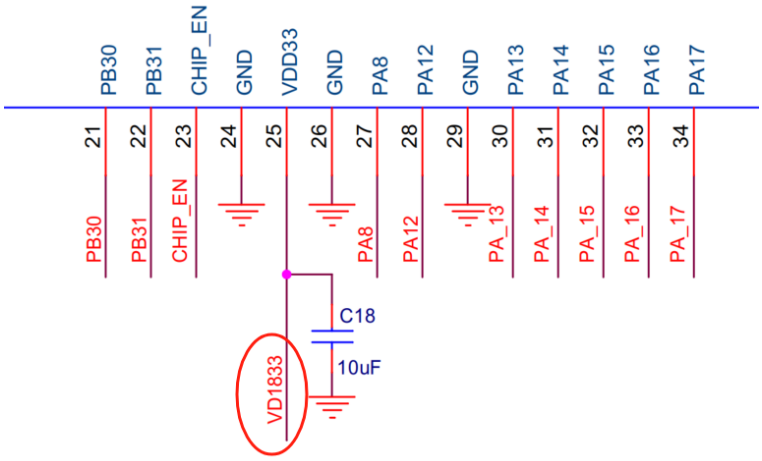


18 Options in HDK

The HDK provided will cover different part numbers and different scenarios. So, there are same reserved components which may be superfluous to your design. You can delete them to simply your schematic.

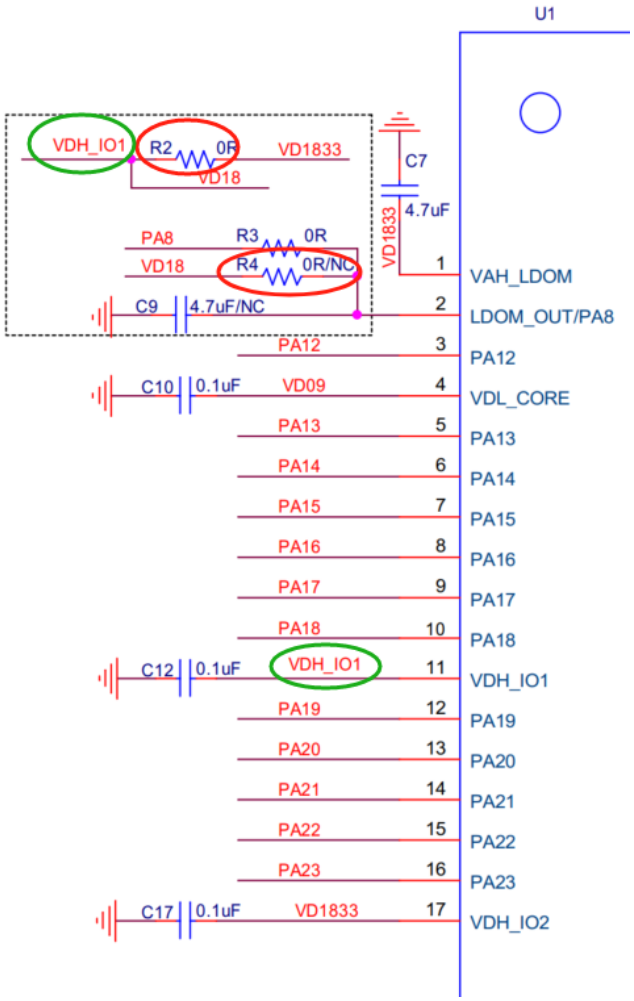
18.1 Wide-Range Voltage Supply

- We have IC part number supporting wide-range voltage supply. You can check the datasheet for more details. So, we named the total input net VD1833, which means the input DC voltage can be 1.8V or 3.3V.
- If you use regular voltage IC (3.3V) in your design, you can name the total power supply net VD33 to avoid confusion.



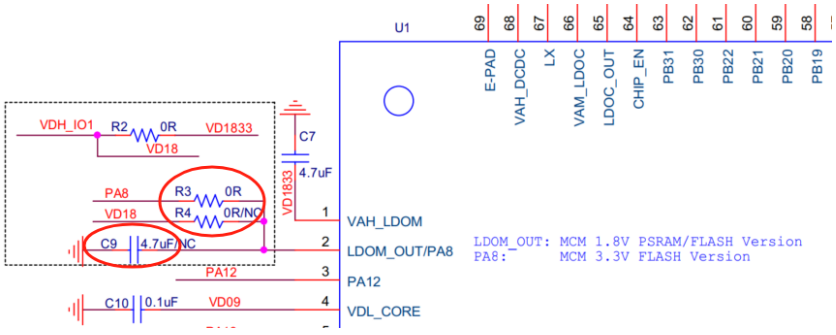
18.2 GPIO Power Option

- VDH_IO1 is from VD1833 or from VD18 by placing R2 or R4 on. VD18 is from LDOM output if the IC you chose pin2 is supported.
- So, if there is no need to reserve different voltage for VHD_IO1 in your design, you can remove the 0R resistors (R2/R4) from your schematic directly.



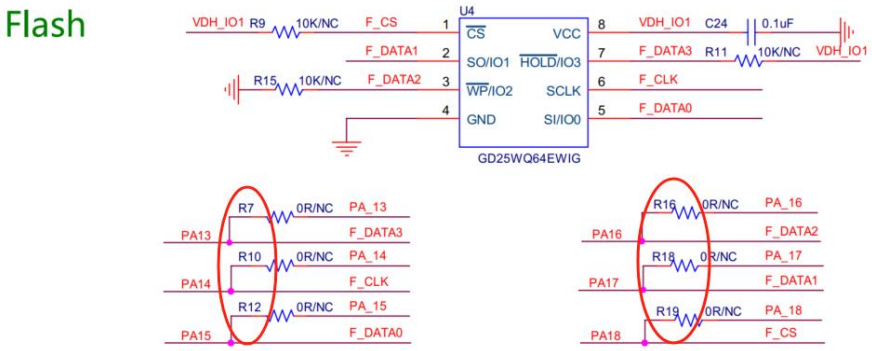
18.3 Pin2 Function Option

- As mentioned above, pin2 has different definition for different IC part number. Please refer to datasheet for more details.
- If the IC part number you used is definite, namely, pin2 function is definite, there is no need to keep the option 0R resistors (R3/R4) in your schematic.
- If the IC you used pin2 function is PA8, there is no need to place C9 in your schematic.
- If the IC you used pin2 function is LDOM_OUT, you should place C9 in your schematic and BOM list.
- If you use the wide-range voltage IC and supply the module total voltage with 1.8V and pin2 function is LDOM_OUT, you should supply pin2 with 1.8V.



18.4 Flash Option

- In our HDK, we keep the option that the flash GPIOs can be connected to module pins for certain IC MCM flash which there is no need to use an external flash.
- If the IC part number you used is definite, there is no need to keep the option 0R resistors (R7/R10/R12/R16/R18/R19) in your schematic.



18.5 PA DC Power Option

- This SoC series have the option to switch WiFi PA working at 1.25V to saving current consumption. Meanwhile, the WiFi Tx power will be limited. For more details, please refer to 'RTL8721DA_RTL8721DC_RTL8721DG_RF DC Power Supply Modes Application Guide_R00.pdf''.
- For 2.4G PA switched to 1.25V, there is no need extra circuit change. It will be switched internally by parameter configuration.
- For 5G PA switched to 1.25V, you should put R5 on and R6 off.
- If your requirement is definite, there is no need to keep the option 0R resistors (R5/R6) in your schematic. You can supply the 5G PA pin (VRH_PA_A) directly.

Revision History

Date	Version	Description
2024-03-14	R00	Initial release
2024-06-17	R01	Supplement the content of Chapters 6~9.
2024-06-20	R02	Modify the contents of Chapter 2 and Chapter 6. Added audio content in Chapter 8.
2025-08-05	R03	Modify some descriptions.