RTL8720E/RTL8726E PCB Layout and Assembly Guide

This document provides the PCB layout and assembly guideline for RTL8720E and RTL8726E

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document is suitable for RTL8720E and RTL8726E.

2 Power

2.1 Switch Regulator Layout

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, LX, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- The input bypass capacitor CIN must be placed as close as possible to the VAH_DCDC pin and avoid vias between CIN and VAH_DCDC pin.
- LX pin is noise node switching with high frequency voltage swing and should be kept at small area. These feedback, analog, digital components and PCB trace keep away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors and minimize trace length to the FB pin net. Place the feedback components as close as possible to the FB pin net. The feedback path cannot connect bead. Pin45 of RTL8720E, and pin65 of RTL8726E are the feedback pins for DCDC regulator.
- Make VAH_DCDC, VOUT, and ground bus connections as wide as possible. These power trace length, width, and vias need to depend on recommend operating input and output current. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- For better thermal performance, design a wide and thick plane for E-PAD /GND_DCDC pin or add a lot of vias to connect ground layer plane.

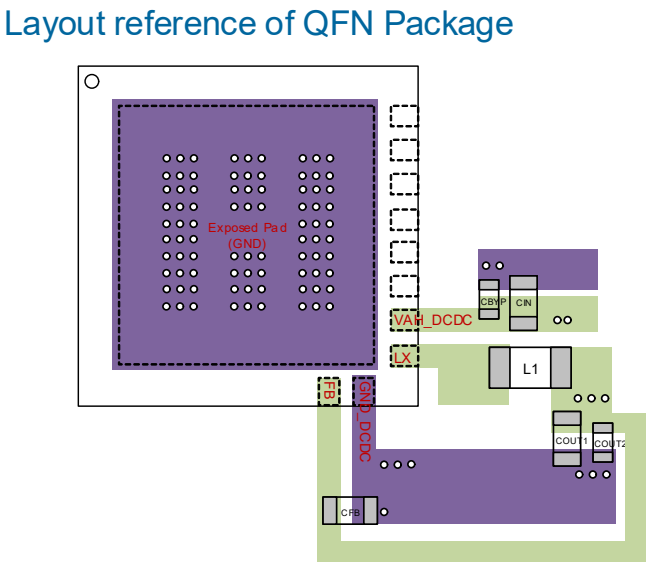

Figure 2-1 Switch Regulator Layout

2.2 Power Trace Routing

- The path of the power trace is recommended using star routing as shown in Figure 1-2 for better noise isolation among circuit blocks. It is strongly recommended that the power trace for PA (VRH_PA) is routed separately.

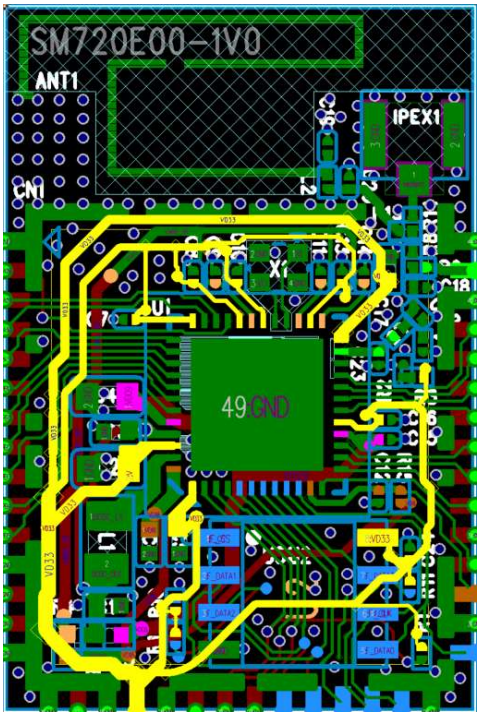

Figure 2-2 Star Routing

- The power trace should be wide enough for lower IR drop.
- Max current for every power pins is shown as follows, as a reference for determining the line width.
- Generally, the width of VRH_PA shall be ≧15mil, and the width of VDL_CORE shall be ≧20mil.

Table 2-1 Current of Power pins

Symbol	Type	Pin number		Description	Max current(mA)
		RTL8720E	RTL8726E		
VAH_LODM	PI	1	1	3.3V input for LDOM	250
VDM_PSRAM	PI	11 (for RTL8720ExM only)	13	1.8V input for PSRAM	100
VAM_AUD	PI	-	14	1.8V input for audio	30
VDL_CORE	PI	16	24	0.9V input for digital core	250
VDH_IO2	PI	17	27	3.3V input for digital I/O power domain	30
VRH_PA	PI	24	34	3.3V input for RF power amplifier circuit	350
VRM_RF	PI	25	35	1.25V or 1.8V input for RF circuit	50
VRH_RF	PI	26	36	3.3V input for RF circuit	50
VRM_SYN	PI	27	37	1.25V or 1.8V input for RF synthesizer circuit	50
VAH_XTAL	PI	30	40	3.3V input for XTAL circuit	20
VAM_AFE	PI	31	41	1.25V or 1.8V input for RF AFE circuit	50
VAH_AUX	PI	32	42	3.3 for AUX ADC	20
VDH_IO1	PI	36	51	1.8V or 3.3V input for digital I/O power domain	30
LDOC_OUT	PO/I	44	64	0.9V output from core LDO and 0.9V input for digital core	500
VAM_LDOC	PI	45	65	1.25V input for LDOC	500
VAH_DCDC	PI	46	66	3.3V input for DCDC regulator	400
LX	PO	47	67	DCDC regulator output	700
LDOM_OUT	PO	48	68	1.8V output for LDOM	200

3 Flash & SD card & EMMC

- Place the matched resistance close to the transmitting end.
- The data and clock lines should be length-matched and surrounded by ground lines. Ensure that the spacing between lines is greater than three times the line width and reference plane is intact. Avoid placing signal lines close to high frequency signals.

4 Cap-Touch

In a typical Cap-Touch application, sensors are constructed with traces on a FR4/FR2 or flexible printed circuit (FPC). Cap-Touch layout design is an important step in the design phase, following the PCB layout design guidelines can help your design achieve higher noise immunity, lower parasitic capacitance (CP), and higher signal-to-noise ratio (SNR). The following factors must be considered during layout.

4.1 Board layers

4.1.1 Two layers

- Sensor pads or sensor interfaces should be on the bottom side and surrounded by the hatched ground.
- All other components (ICs, VDD and GND traces, other signal traces) should be on the top side, and sensor traces are connected to the sensor pads or sensor interfaces by vias.
- Ground surrounding the sensor interfaces and sensor traces close to the chip should be in a hatch pattern.
  - For top side, a hatched ground with 7 mil line and 70 mil spacing is better.
  - For bottom side, it is recommended to use the hatched ground with 7 mil line and 45 mil spacing.

4.1.2 Four layers

- Top layer: Place all other components (ICs, VDD and GND traces, sensor traces and other signal traces).
- The second layer: Place the hatched ground with 7 mil line and 70 mil spacing under the sensor traces area.
- The third layer: Place sensor traces and VDD player
- Bottom layer: Place sensor pads or sensor interfaces, where sensor pads or sensor interfaces should be surrounded by the hatched ground with 7 mil line and 45 mil spacing.

NOTE

No matter two or four layers, if limited by other conditions, you can use the full clearance between the top and bottom layers to replace the grid ground.
For the other parts not related to the cap-touch function, solid ground should be placed as much as possible.

4.2 Trace

4.2.1 Trace length and width

- To reduce parasitic capacitance, the trace between sensors and IC pins should be as short and thin as possible.
- Generally, the max trace length should be less than 30cm on standard PCB and less than 5cm on flexible PCB (FPC).
- The trace width should be between 6mil and 9mil (7mil recommended).
- The spacing between sensor trace and ground should be between 10mil and 20mil.
- Since the longer trace will introduce larger parasitic capacitance, higher consumption (large parasitic capacitance needs more current to maintain good performance) and lower sensitivity, it's better to minimize the trace length in applications.

4.2.2 Trace routing

- When a finger touch sensor pad used, it can only interact with the effective cap-touch channel, which means do not route the sensor traces directly under any sensor pads, except the sensor traces connected to it.
- When routing, try to keep away from high-speed signals (RF antenna, SPI, I2C, XTAL, etc) and avoid parallel with them. Otherwise it will introduce crosstalk.
- If any non-sensor trace crosses the sensor trace, ensure that the intersection is orthogonal.
- If it's unavoidable that sensor traces are parallel to the high-speed signal, a ground wire with 7 mil width should be placed between them, and the spacing between sensor trace and ground wire should be at least 10mil.

4.2.3 Via number and position

- Via number: To reduce parasitic capacitance on sensor traces, it's better to use less vias. The number of vias should not be more than 3.

- Via position: To shorten the trace length, vias should be places on the edge of the sensor pads, and the aperture range is from 12mil/6mil to 24mil/12mil. 16mil/10mil is the recommended size.

4.2.4 Series resistor

All cap-touch channels must have a 560ohm series resistance placed close to the chip (< 1cm) to reduce RF interference and provide ESD protection.

4.3 Check list

Category	Item	Min.	Max.	Description
Placement	2-layer PCB	N/A	N/A	● Top: Sensors, devices, and components; VDD and GND traces, other signal traces ● Bottom: Sensor traces, devices and components; VDD and GND traces, other signal traces **Note**: ● Avoid VDD traces, clock traces, and driven traces over sensor traces. ● Avoid sensor trace run parallel to a clock signal or driven signal.
	4-layer PCB	N/A	N/A	● Top: Sensors, devices, and components ● Second layer: Hatched ground ● Third layer: Sensor traces, VDD layer ● Bottom: Devices, and components **Note**: Avoid VDD traces, clock traces, and driven traces run parallel under or over sensor traces.
Routing	Sensor trace length			Not more than 30cm in standard PCB and 5cm in FPC, and make sure the trace capacitance and sensor capacitance is less than 50pF.
	Sensor trace width	6mil	9mil	The recommended value is 7mil (FR4/FR2/FPC).
	Sensor trace routing	N/A	N/A	The best choice for sensor is routed on the non-sensor side. Otherwise, make sure the sensor trace area is a touch forbidden area. **Note**: Avoid sensor trace run parallel to a clock signal or driven signal. If any non-sensor trace crosses the sensor trace, ensure that the intersection is orthogonal.
	Via position	N/A	N/A	Via should be placed near the edge.
	Via number	0	3	1 via is needed, more via results other parasitic capacitance.
	Via hole size	12mil/6mil	24mil/12mil	The recommended via hole size is 16mil/10mil.
	Trace series resistor	47	560	Series resistors close to the chip for better suppression and ESD.
	Trace-GND layer distance	10mil	20mil	20mil
GND	GND-Top layer			Hatched pattern 7mil trace and 35~45 mil grid
	GND-Bottom layer			Hatched pattern 7mil trace and 65~75 mil grid or no ground
Overlay	Overlay thickness	N/A	3mm	Depends on your product, 3mm for glass or plastic; higher thickness may decrease the sensitivity.
	Overlay material	N/A	N/A	Non-conductive material

5 Audio

- The positions of the MIC peripheral devices are placed according to the requirements of the schematic diagram.
- MICx_P/MICx_N, quasi-differential traces, through holes are punched in the ground, and the integrity of the ground is guaranteed when passing through the layers.
- MIC traces and placement are far away from (>=200mil) RF, PA, switching power supplies.
- The ESD device must be placed close to the MIC, and the traces drawn from the MIC must first pass through the ESD device before connecting to other devices.
- AEC circuits are neatly arranged in the order of the schematic diagram.
- The LINEOUTP/N signal is grounded, the line width is 5 mil, and the traces and vias are far away from high-speed signals and clock

signals.

- The reference design of the grounding of the signal line is as follows:

Figure 5-1 Audio Trace

6 Crystal

- The high speed ($\geq 10\text{kHz}$) signal traces shall be keep far away from XI/XO pins and trace.
- Place an intact GND plane with shortest distance connected to the E-PAD under the whole crystal routings. If the GND can't be connected to E-PAD directly, there should be noisy current flowing on this GND plane.
- If the dielectric core of the PCB is too thin(ex: ≦3mil), the high parasitic capacitance on XI/XO routings may dominates the crystal frequency, then the GND under the routes shell be removed, and the high speed signal traces on the lower layers shall be kept far out of the empty (under crystal block) area.
- Signal and power trace near XI/XO should be isolated by ground.
- The Xtal should be kept out in top layer.
- Keep whole XI/XO traces in the same layer.

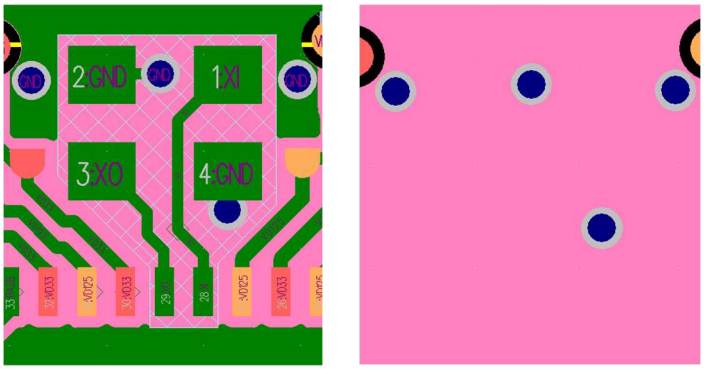

Figure 6-1 Xtal Layout-TOP Layer, GND Layer

7 RF

- The characteristic impedance of RF trace should be 50Ω.
- For a 2-layer PCB design, we recommend having good ground shielding on both sides of the RF traces near the IC pins and connecting them to the EPAD to enhance isolation between the RF and the crystal oscillator.
- Placing more GND vias along the RF trace is recommended.

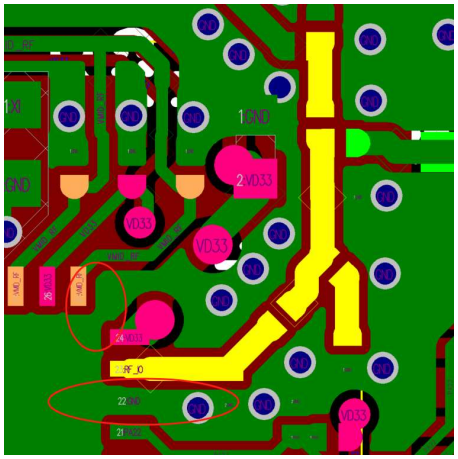

Figure 7-1 RF Trace

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

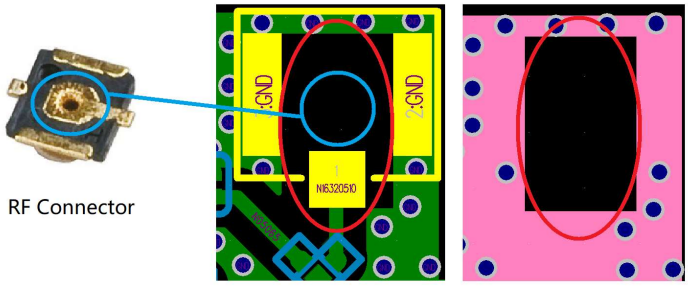

Figure 7-2 Keep-out for RF connector

8 Shielding

- Considering the EMC design, must comply with the following design rules:
  - For good shielding case grounding, there must be GND via placed on/around the soldering pads and the recommended via spacing is a≤1.5mm.
  - The open gap is recommended b≤2mm.
  - Use separated shielding cases if the other circuit blocks need to be shielded as well.
  - The shielding cover soldering on PCB is recommended If do use joint shielding case (frame + cover), make sure that the cover touches the compartment frame firmly.
  - Height: if possible, the minimum (inner) height suggest >1mm.

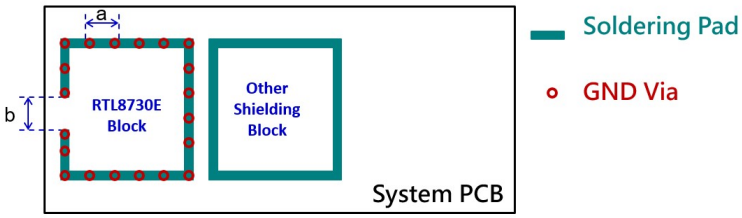

Figure 8-1 Shielding Layout

9 Land Pattern and Assembly

- Refer the Package Specification in the datasheet for the detail dimension.
- Recommended to use the normal value in the dimension table.

9.1 Guideline for E-pad land patterns

9.1.1 The E-pad Design

- The center pad size should follow the same E-PAD size of package specifications in the datasheet.

9.1.2 Solder Mask Guidelines for E-pad

- The actual solder mask opening size should adding 2mil at each side to the size of the thermal pad.

9.1.3 Paste Mask Guidelines for E-pad

- Stencil openings should be segmented in exposed regions, solder paste coverage recommend matrix by 3*3 as follows:

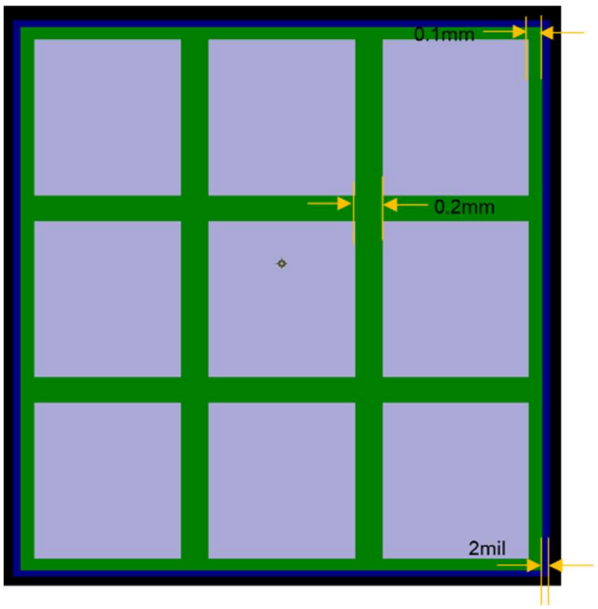

Figure 9-1 Paste Mask of Thermal Pad

  - Recommended edge length/width of a matrix land is about 0.1mm.
  - Distance between the lands should be about 0.2mm.
  - Above two the ratio is 1:2
  - Exposed pad design by matrix methods to prevent mass solder let QFN lift, stencil opening should be approximately 60~80% PCB exposed pad size.
  - Thermal Pad voiding suggestion <30%

9.1.4 Center pad hole specification(s)

- Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 0.6~1mm grid, as shown in Figure 9-2.
- And the vias under E-pad should be as much as possible for good heat dissipation. Large package like QFN100/QFN144 can use larger size of via and bigger pitch. But for small package size like QFN48/68, it should use smaller size of via and smaller pitch.

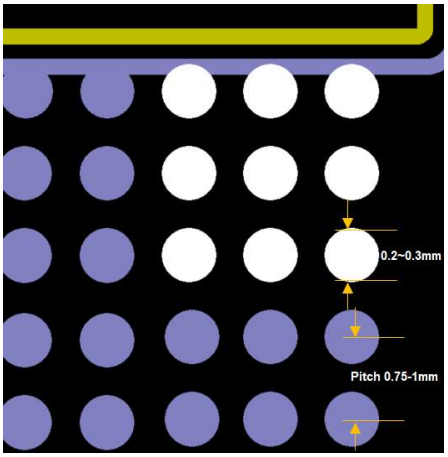

Figure 9-2 PCB Exposed Pad Land Pattern Via Grid

9.2 Signal I/O pad design

9.2.1 Guidelines for perimeter land patterns

- Extend of outer Cu Land towards package center as follows:

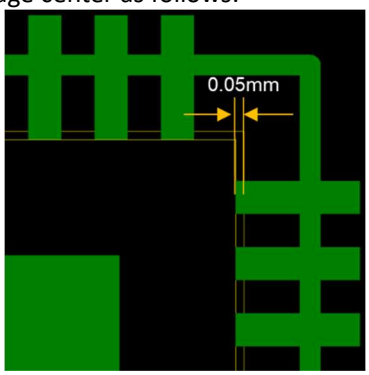

Figure 9-3 Length of outer lead perimeter size towards package center

- Length of Outer Cu land exterior to the package edge ⩾ 0.2~0.3 mm

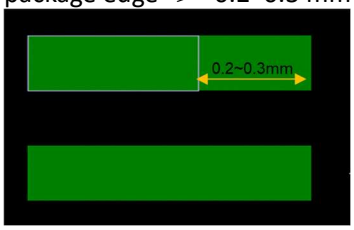

Figure 9-4 Length of outer lead perimeter size to the package edge

- For dual ring QFN, Length of Inner Cu Land L use max parameter.

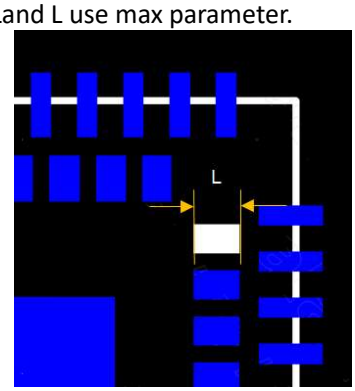

Figure 9-5 Length of Inner lead perimeter size

- Width of Inner Cu Land W should be extend to normal size+0.1mm(for 0.5mm pitch) in order to improve soldering yield.

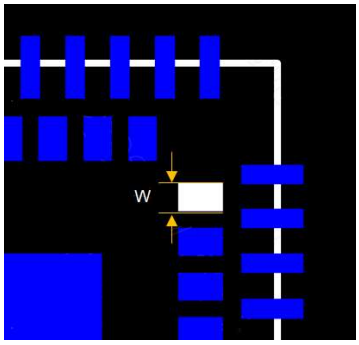

Figure 9-6 Width of Inner lead perimeter size

9.2.2 Solder Mask guidelines for perimeter lands

- The solder mask can be extend 2mil than the original size of each edge.
- As the follow picture, the orange part is the pin pad. And the red part is the solder mask. The yellow distance is 2mil.

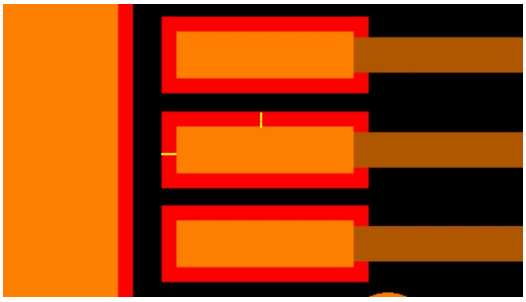

Figure 9-7 The pin pad and the solder mask

- I/O pin lead pitch will be small and small, If PCB fab technology ability is not enough space available for solder mask, we suggestion IC lead pitch low then 0.4mm PCB pad design use “trench” type solder mask opening to design .

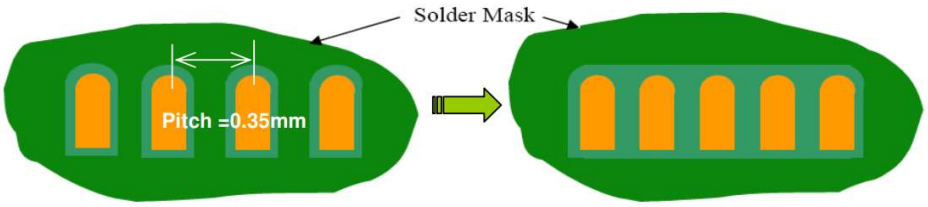

Figure 9-8 Between the pads, it’s recommended to use “trench” type solder mask opening to design.

9.3 Stencil Design Guidelines

9.3.1 Stencil Type and Thickness

- Stencil type: Laser-Cut.
- The recommended stencil thickness as follows:

Table 9-1 Stencil Thickness

Terminal Pitch	Recommend Stencil Thickness
≥ 0.65	0.13 ~ 0.15mm
0.4 ~ 0.5	0.1 ~ 1.12mm
< 0.4	0.08 ~ 0.1mm

9.3.2 Solder Paste Type(s)

- The most common solder paste powder sizes for SMT are type 3 (T3), type 4 (T4), and type 5 (T5). The lower the number, the larger the particle size within the solder powder.

9.4 Oven temperature profile

- The reflow condition used in J-STD-020 as following table. All the temperature is measured on the topside of the package.

Table 9-2 Oven Control Data

Stage	Note	Pb-free assembly
Average ramp-up rate	T_L to Tp	3 ℃/ second max.
Preheat	Temperature min (T_{smin})	150℃
	Temperature max (Tsmax)	200℃
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217℃
	Time (t_L)	60 – 150 seconds
Peak package body temperature (Tp)		See following table. Tp must not exceed the specified classification temp in following table.
Time(tp) within 5℃ of the specified classification temperature (Tc)		30 seconds
Ramp-down rate (Tp to T_L)		6 ℃ / seconds max.
Time 25℃ to peak temperature		8 minutes max.

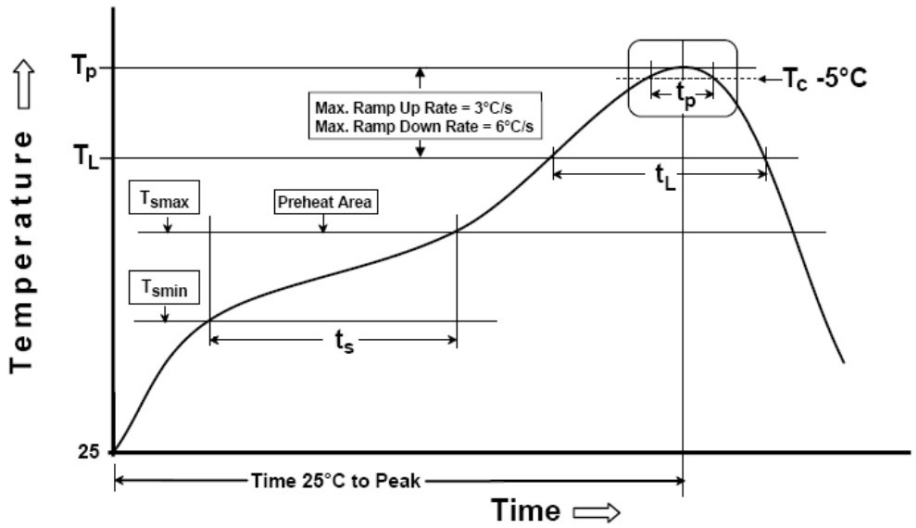

Figure 9-9 Recommended reflow profile

NOTE

The above reflow profile is for MSL classification only, not the recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameter in above table.

- The peak temperature package can sustain depends on its volume and thickness. The reason is that, engineering studies have shown that, thin, small volume SMD packages reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, technical and/or business issues normally require thin, small volume SMD packages to be classified at higher reflow temperatures.
- The different peak temperature for different package volume / thickness is listed as following table:

Table 9-3 Pb-free Process-Package Classification Reflow Temperature

Package Thickness	Volume < 350 mm3	Volume 350 – 2000 mm3	Volume > 2000
＜1.6 mm	260 +0 /-5℃	260 +0/-5 ℃	260 +0 /-5℃
1.6 – 2.5 mm	260 +0 /-5℃	250 +0/-5 ℃	245 +0/-5 ℃
≧ 2.5 mm	250 +0 /-5℃	245 +0/-5 ℃	245 +0/-5 ℃

- Reflow Condition Recommendation For SMT Process
  - In SMT process, the reflow temperature profile for manufacturing should be recommended by solder paste supplier, and the peak temperature should not be higher than the lowest peak temperature used for the MSL classification for the components on board.
  - The reflow temperature profile defined for MSL classification in J-STD-020 is not recommended to be used for

real SMT process unless approved by solder paste supplier. Basically, the reflow profile used for MSL classification is for classification only and regardless of the solder paste itself. Thus the temperature profile is only to “simulate” the reflow process in real case, but not a recommendation for that. The real case still depends on solder paste itself.

Revision History

Date	Version	Description	Modified by
2022-09-13	v1.0	Initial release	Ziliang_yan
2023-07-27	V1.1	Typo correction	Ziliang_yan
2025-03-25	V1.2	Update layout guide for RF trace	Ziliang_yan