RTL8710E/RTL8713E Hardware Design Guide

This document provides the Hardware design guide and notes

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed hardware design information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Contents

1 Introduction

This document provides the Hardware design guide and notes for the RTL8710E & RTL8713E series. Please refer to RTL8710E_RTL8713E_PCB_Layout_and_Assembly_Guide_v1.1.pdf for layout and assembly guide.

2 Power supplement

2.1 Power Structure

Only an external typical 3.3V power supply is required for the chip, all the other required voltages can be converted and output by embedded three low-dropout regulators (LDO) and one DC-DC switching regulator (DCDC).
Embedded DC-DC and LDO have voltage-scaling and mode-switching function, which can effectively reduce power consumption. It is suggested to use embedded DC-DC and LDO powering RTL8713E.
There are two options for power supply, the block diagrams are summarized in Figure 2-1 and Figure 2-2.
The power supply option is determined by the level of trap pin PSO_SEL during the process of power on. The peripheral circuit needs to match the level of trap pin PSO_SEL to prevent damage to the circuits.
The difference between option 1 and option 2 is the power supply solution for digital core and Wi-Fi & BT RF circuits.

- If the digital core circuit is the main power consumption circuit in the application scenario, it is recommended to choose option 1 to achieve a lower overall power.
- If the Wi-Fi & BT RF circuit is the main power consumption circuit, option 2 is recommended to achieve a lower overall power.

2.1.1 Power supply option 1

When PSO_SEL is low during power on, IC is supposed to be powered by option 1.

- DCDC: DCDC outputs typical 0.9V or 1.0V, which is controlled by software based on application requirements, for digital core circuits.
- LDO core (LDOC): LDOC is not used but its input and output pins are connected to 0.9V or 1.0V for leakage consideration.
- LDO memory (LDOM): LDOM outputs typical 1.8V for PSRAM, Audio Codec and RF circuits.

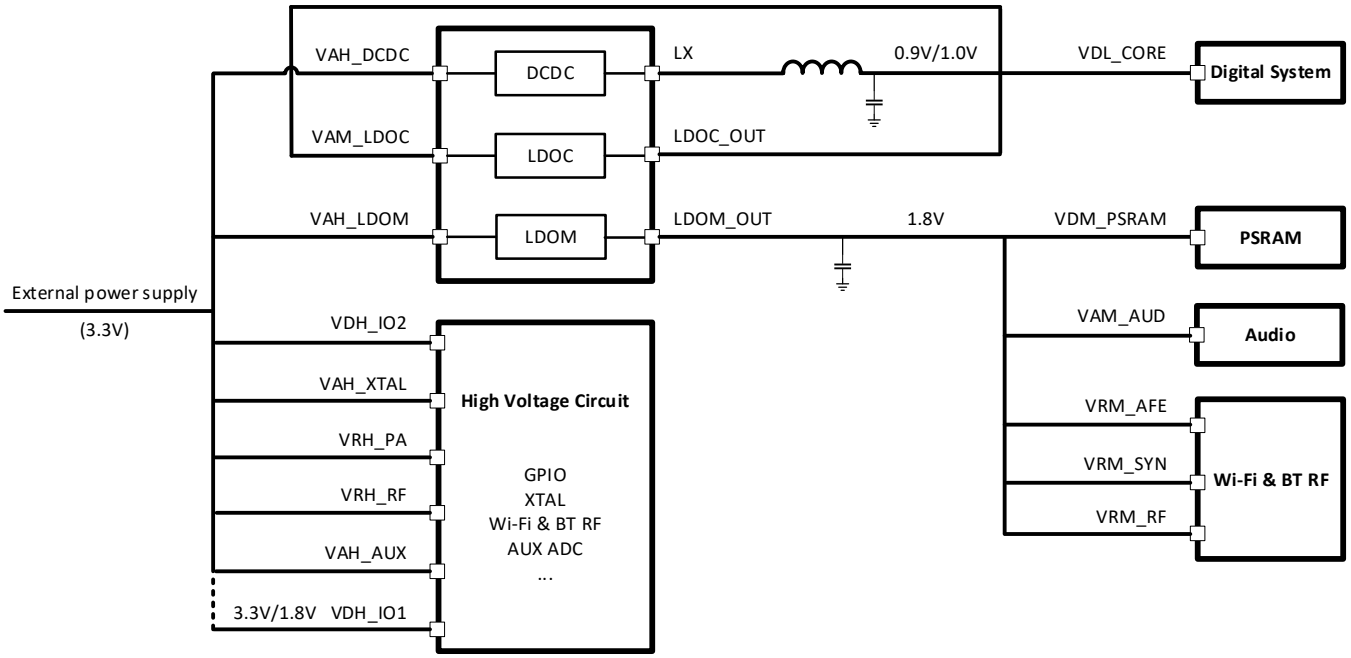


Figure 2-1 Power structure (power supply option 1)

2.1.2 Power supply option 2

When PSO_SEL is high during power on, IC is supposed to be powered by option 2.

- DCDC: DCDC outputs typical 1.25V or 1.35V for RF circuits and LDOC input.
- LDO core (LDOC): LDOC outputs typical 0.9V or 1.0V for digital core circuits.
- LDO memory (LDOM): LDOM outputs typical 1.8V for PSRAM and Audio Codec circuits.

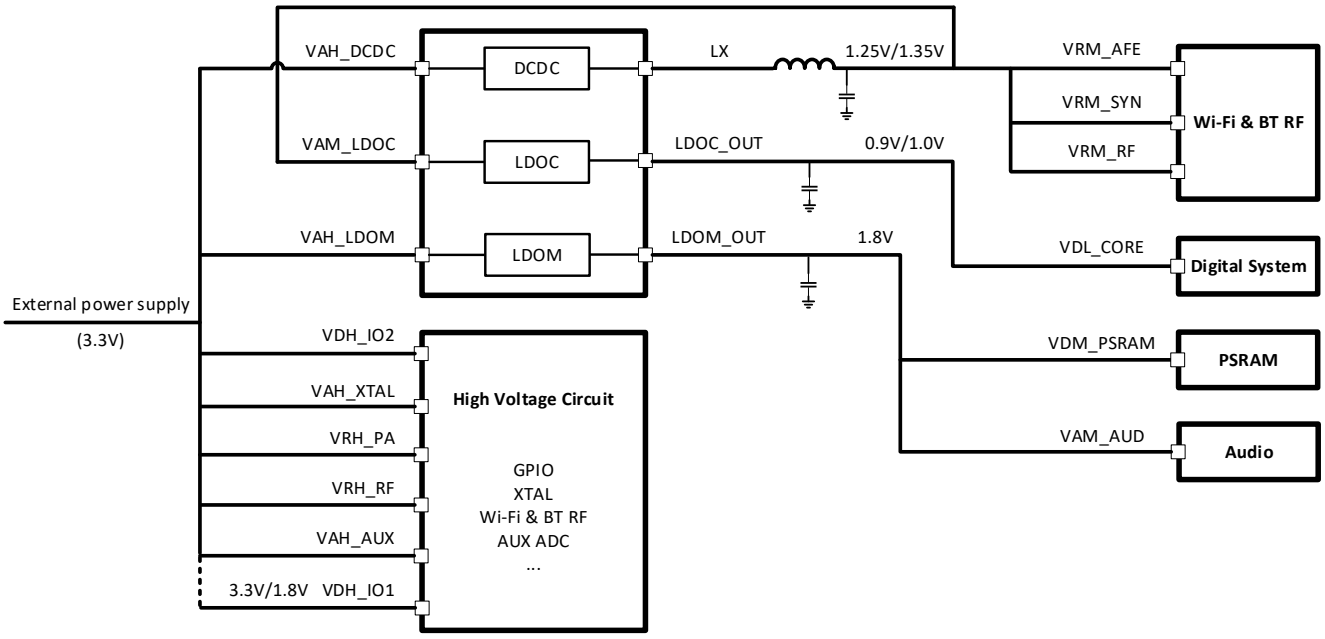


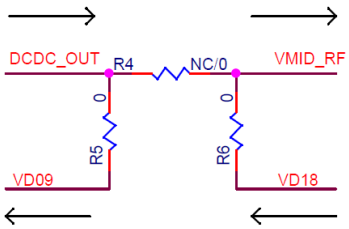
Figure 2-2 Power structure (power supply option 2)

2.1.3 Options in HDK for power supply option switch

In HDK, several 0ohm resistors are reserved for power supply option switch as in below picture. Under normal use, users can choose a specific power supply option and correctly connect the power supply pin without reserved 0ohm resistors.

```
For Power Supply Option1
R4  NC
R5,R6   Placed
R2 Placed (PA22 Pull_L)
R3 NC
```

```
For Power Supply Option2
R4  Placed
R5,R6   NC
R2 NC
R3 Placed (PA22 Pull_H)
```



2.1.4 Power supply for I/O Pins

Generally, VDH_IO is powered by typical 3.3V. However, VDH_IO1 can support 1.8V or 3.3V power supply.

- PA23~PA31 and PB0~PB10 are powered by VDH_IO1 which support 1.8V/3.3V IO power.

Typical 1.8V power output from LDOM can be used to powering VDH_IO1 if needed.

Because embedded LDOM have mode-switching function, which means it will switch between normal mode supporting higher power consumption and low power mode supporting lower power consumption. Mode-switching function is operated by SW according to the state of the chip. Addition safe maximum power current that can be provided by LDOM to IO is 10mA. If more power current is needed, please use power from other power sources.

2.2 Capacitors and Inductance for Power Pins

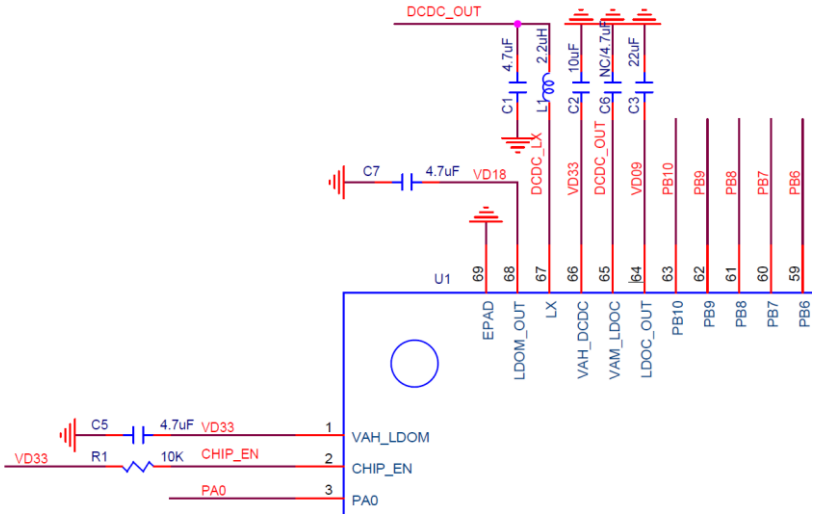
Generally, for DCDC, LDO input and output, and RF PA power pins, large capacitor should be placed. For other power pins, 0.1uF capacitor is needed.

2.2.1 DCDC and LDO in Power supply option 1

Generally, tolerance of capacitors for DCDC and LDO needs to be within +/-20%. Suitable capacitor types need to be selected based on the actual operation temperature range.

- C2, C1 are for DCDC input and output, capacitor 10uF and 4.7uF is recommended.
- C6, C3 are for LDOC input and output. In power supply option 1, LDOC is not working, C6 is not needed. Because LDOC output and actual power pin for digital circuits is co-bonded, C3 is needed. Capacitor 22uF is recommended.
- C5, C7 are for LDOM input and output, capacitor 4.7uF and 4.7uF is recommended
- L1 is power inductor for DCDC regulator. You should choose the inductor carefully. The inductor specifications recommended are as follows.

	Inductance (uH)	Tol. (%)	Saturation Current, ⊿L=30%(mA)	Temperature Current, ⊿T=40℃(mA)	Rdc(Ω) typ.
L1	2.2	20	>= 950	>= 950	0.1

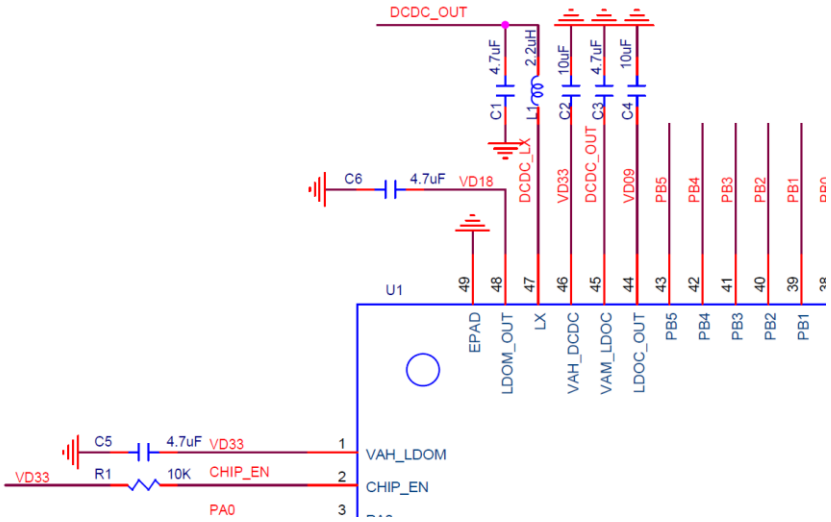


2.2.2 DCDC and LDO in Power supply option 2

Generally, tolerance of capacitors for DCDC and LDO needs to be within +/-20%. Suitable capacitor types need to be selected based on the actual operation temperature range.

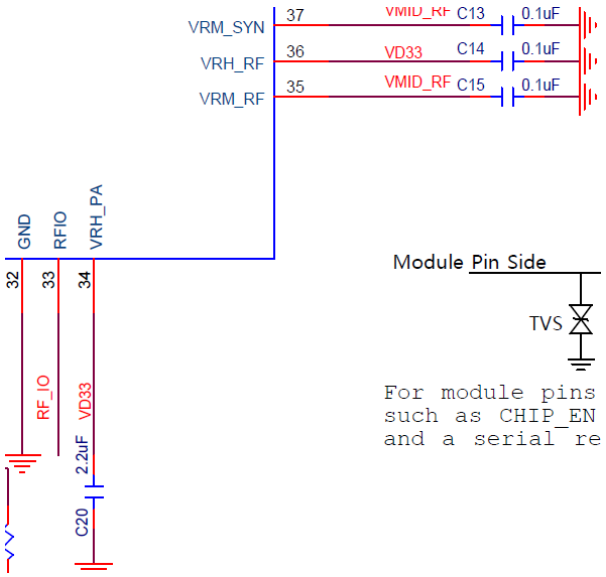
- C2, C1 are for DCDC input and output, capacitor 10uF and 4.7uF is recommended.
- C3, C4 are for LDOC input and output, capacitor 4.7uF and 10uF is recommended.
- C5, C6 are for LDOM input and output, capacitor 4.7uF and 4.7uF is recommended
- L1 is power inductor for DCDC regulator. You should choose the inductor carefully. The inductor specifications recommended are as follows.

	Inductance (uH)	Tol. (%)	Saturation Current, ⊿L=30%(mA)	Temperature Current, ⊿T=40℃(mA)	Rdc(Ω) typ.
L1	2.2	20	>= 950	>= 950	0.1



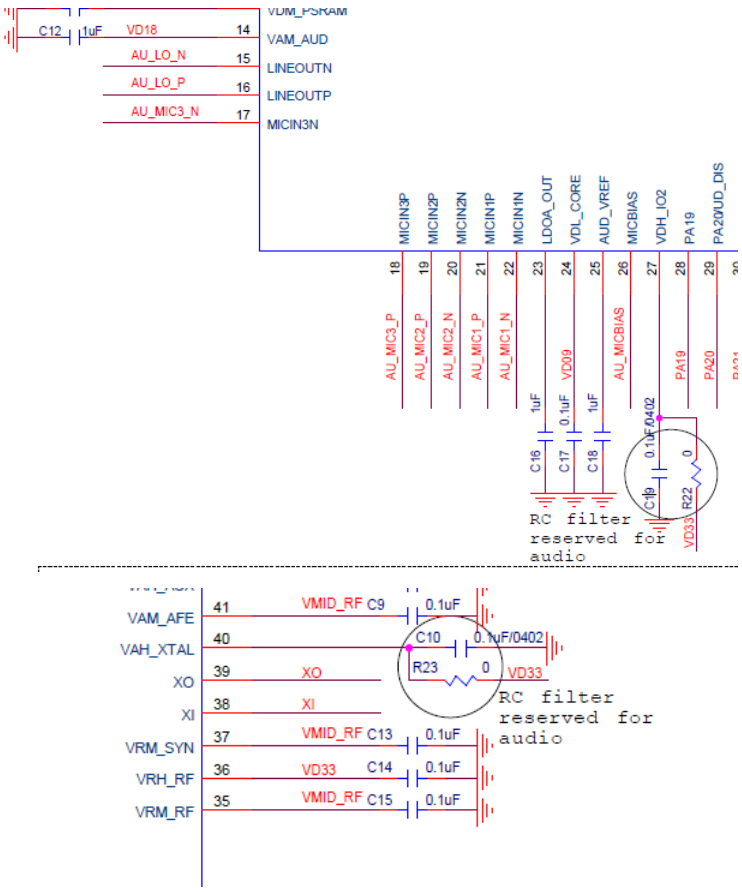
2.2.3 RF Pins

- C20 is for RF PA, Capacitor 2.2uF is recommended.



2.2.4 Audio Pins

- C12 and C16 are audio power input and output, capacitor 1uF is recommended.
- R22 and R23 are reserved resistors used to filter out possible noise to VDH_IO2 and VAH_XTAL, the noise on VDH_IO2 and VAH_XTAL can affect the performance of audio circuits.



2.3 External Voltage Regulator Module recommendation

- VXH[1] is the main power supply for RF, embedded DC-DC switching regulators, etc. Recommended specification for external VRM is listed in
- Table 2-1.
- The output voltage of external voltage regulator module can be from 2.97 to 3.63V. Output voltage noise is included in output voltage range.
- The stability of the output power supply is important for RTL8713E. Suggested output voltage ripple should be under +/-100mV. Output voltage ripple should be considered in all possible working states such as WIFI initialization, WIFI TRX, etc. If the VXH is shared with other high power consuming circuits, such as audio amplifiers, IR circuits, etc., output voltage ripple also needs to be under +/-100mV during the operation of these circuits.
- Continuous output current should be higher than 0.8 A, which excluding power consumption in circuits other than RTL8713E.
- Suggested output voltage rise time needs to be not faster than 0.1ms, more specific power sequence can be found in datasheet.

Table 2-1 External VRM recommended specification

Symbol	Parameter	Operation conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	Including $V_{OUT-RIPPLE}$	2.97	3.3	3.63	V
$V_{OUT-RIPPLE}$	Output voltage ripple	Including all possible operation conditions[1]			+/- 100	mV
I_{OUT}	Continuous output current	Excluding power consumption in circuits other than RTL8713E.	0.8			A
T_{RISE}	Output voltage rise time		0.1	1		ms

NOTE

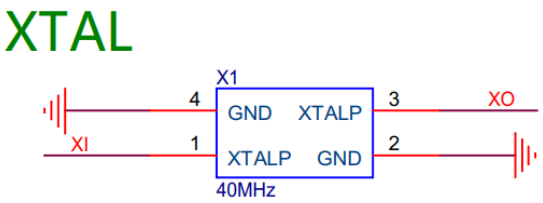
[1] VXH refers to typical 3.3V power supply including VAH_LDOM, VDH_IO2, VRH_PA, VRH_RF, VAH_XTAL, VAH_AUX and VAH_DCDC.

3 Chip Enable Pin

The CHIP_EN pin needs to remain in a high state when the chip is powered on. If the chip needs to be reset through CHIP_EN pin, it is necessary to ensure that the CHIP_EN is pulled down by at least 0.1ms. For more specific sequences, please refer to the datasheet for Power Sequence.

4 Crystal Characteristics

The chip has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.
Please connect crystal XI/XO to main IC directly. There is no need to add extra capacitors on net XI/XO.



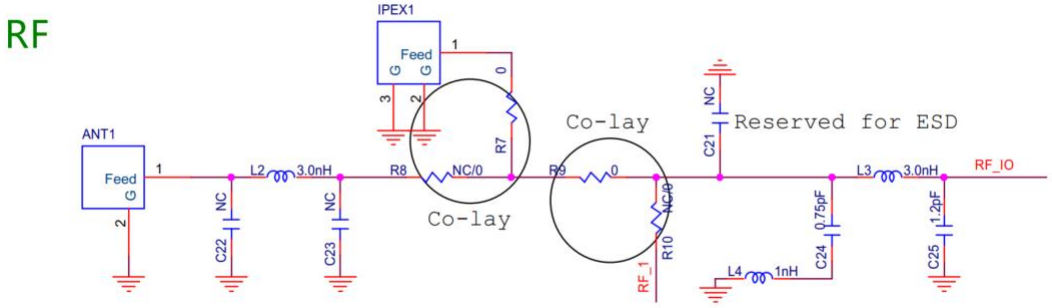
The characteristic requirements of external crystal are listed in Table 4-1 .

Table 4-1 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

5 RF Circuit

- Pi-shape matching (C25/L3/C24/L4) should be placed at RFIO to tune RF impedance and harmonics rejection. The LC values for this pi-shape matching should be fine-tuned for different PCB design.
- A TVS (C21) is reserved for ESD protection.
- R8 and R7 are co-lay in our HDK for selecting RFIO path to RF connector (IPEX1) or printed antenna (ANT1).
- R9 and R10 are co-lay in our HDK for selecting RFIO path to module pin or RF connector/antenna.
- Pi-shape circuit (C22/L2/C23) is reserved for antenna matching.
- You can add a RF test point between R8 and C21 for RF test in your mass production.
- The recommended tolerance of the RF inductors is ±0.3nH or better, and tolerance of the RF capacitors is ±0.1pF or better.



6 I/O Pins Characteristics

6.1 Features

The following electrical properties are configurable for standard I/O pins:

- Function ID
- Internal Pull-up/Pull-down Resistor
- Driving strength
- Schmitt trigger
- Shutdown & RESET
- Open drain mode

6.2 Functional Description

The I/O diagram is given in Figure 6-1. There are various types of I/Os within the chip, different I/Os have different configuration.

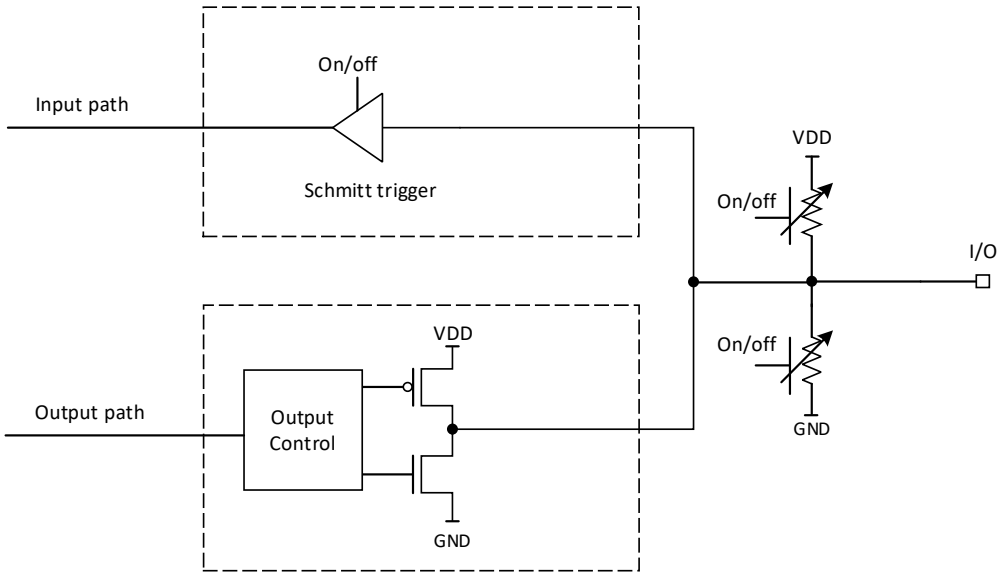


Figure 6-1 I/O diagram

6.2.1 I/O Types

All I/Os are listed in Table 6-1. The HBM of all I/Os is above 3.5KV.

Table 6-1 I/O Types

Pin name	I/O power pin	Driving (mA)[1]		Internal pull resistor (kΩ)[2]			Internal pull resistor available in deep-sleep mode[3]?
		1.8V (±10%)	3.3V (±10%)	Min.	Typ.	Max.	
PA0~PA13[4]	VAH_LDOM	-	8/16	40	80	120	Y
PA14~PA18[4]	VDH_IO2	-	8/16	2.3/5	4.7/10	7.1/15	Y
PA19~PA22[4]	VDH_IO2	-	4/8	40	80	120	Y
PA28~PA31/PB0~PB5[5]	VDH_IO1	1/2	4/8	40	80	120	Y
PA23~PA27/PB6~PB10[5]	VDH_IO1	2/4	8/16	2.3/5	4.7/10	7.1/15	Y
PB11~PB19[6]	VAM_AUD	1/3	-	PU:185 PD:52	PU:300 PD:100	PU: 431 PD:165	N

NOTE

[1] The I/O powers supported by different I/Os are different, and the driving capability is related to the I/O powers. Refer to Table 6-4 for V_{OH} and V_{OL}. Different drive capabilities can be controlled by registers. For example, 4/8 refers to the driving capability of 4mA or 8mA, which can be adjusted through registers.
[2] Except for PB11~PB19, the pull-up and pull-down values of other I/Os are the typical values at 3.3V. The values at 1.8V are twice the typical values at 3.3V. The range is ±50%. Different resistor can be controlled by registers. For example, 4.7/10 refers to the internal pull resistor of 4.7kΩ or 10kΩ, which can be adjusted through registers.
[3] In deep-sleep mode, since VAM_AUD is powered off, PB11~PB19 are in floating state and the internal resistors of these pins are unavailable. If circuit connected with these GPIOs needs to be pulled high or low state, external resistors on PCB are needed. In other mode except deep-sleep, internal resistors of all GPIOs are available.
[4] The pins of this group only support 3.3V I/O power.
[5] The pins of this group support 1.8V/3.3V I/O power.
[6] The pins of this group only support 1.8V I/O power.

6.2.2 IOCTRL Register

Each I/O pin has one IOCTRL register assigned to control the pin's electrical characteristics. I/O Register base address 0x4100C800. For example, the address of the register of the PA0 GPIO is 0x4100C800, the address of the register of the PA1 GPIO is 0x4100C804. The bit[7:0] field in the GPIO register can be set to GPIO (typically value 000) or a special function.

- For pins set to GPIO, the GPIO IP registers determine whether the pin is configured as input or output.
- For any special function, the pin direction is controlled automatically depending on the function.
- For specific information about PINMUX function, please refer to the PINMUX documentation.

Table 6-2 IOCTRL register

offset	Bit	Access	INI	Symbol	Description
0h	[15]	R/W	0h	GPIO_BIT_SHUT_DOWN	GPIO shutdown Only when the shutdown signals of the entire group of IOs are all 1, will all the IOs of this group be disabled. 1: disable GPIO 0: enable GPIO
	[12]	R/W	1h	GPIO_BIT_SCHMITT_TRIGGER_EN	GPIO Schmitt control 1: enable Schmitt trigger 0: disable Schmitt trigger
	[11]	R/W	1h	GPIO_BIT_DRIVING_STRENGTH	GPIO driving ability control. 1: high 0: low The actual driving current is depend on GPIO type.
	[10]	R/W	0h	GPIO_BIT_PUPDC	Some GPIO may have two type of PU/PD resistor, this bit can select it. 1: small resistor 0: big resistor
	[7:0]	R/W	0h	GPIO_BIT_FUNCTION_ID	GPIO PINMUX function ID selection

The PU/PD of the GPIO in Active & Sleep mode is controlled by the IOCTRL register. Allows selection of on-chip pull-up or pull-down resistors for each pin. Please refer to the IOCTRL register table for specific information.
IO internal pull up and pull down are controlled by separate registers. The 32 bits of each register control the status of 32 IOs respectively. Refer to Table 6-3 for details

Table 6-3 I/O pull up & pull down register

offset	Bit	Access	INI	Symbol	Description
100h	[31:0]	R/W	100013h	PA_PU	PA0~PA31 pull up enable when system is in active.
104h	[19:0]	R/W	0h	PB_PU	PB0~PB19 pull up enable when system is in active.
108h	[31:0]	R/W	0h	PA_PD	PA0~PA31 pull down enable when system is in active.
10Ch	[19:0]	R/W	0h	PB_PD	PB0~PB19 pull down enable when system is in active.
110h	[31:0]	R/W	0h	PA_PU_SLP	PA0~PA31 pull up enable when system is in sleep.
114h	[19:0]	R/W	0h	PB_PU_SLP	PB0~PB19 pull up enable when system is in sleep.
118h	[31:0]	R/W	0h	PA_PD_SLP	PA0~PA31 pull down enable when system is in sleep.
11Ch	[19:0]	R/W	0h	PB_PD_SLP	PB0~PB19 pull down enable when system is in sleep.

NOTE

- *GPIO PU&PD register base address 0x4100C800.*

6.2.3 Function ID

Change the I/O function ID through GPIO_BIT_FUNCTION_ID in Table 6-2, refer to the PINMUX documentation for details.

6.2.4 I/O Internal Pull Resistor Control

The PU/PD of the I/O in Active & Sleep mode is controlled by the PU&PD register. Allows selection of on-chip pull-up or pull-down resistors for each pin. For Specific information, please refer to the I/O PU&PD register table (Table 6-3).
Pull-up and Pull-down resistor's value is different between different I/Os. The resistor value is changed by controlling the GPIO_BIT_PUPDC of register table (Table 6-2). For I/Os with only one resistance value, GPIO@_pupdc is not valid.

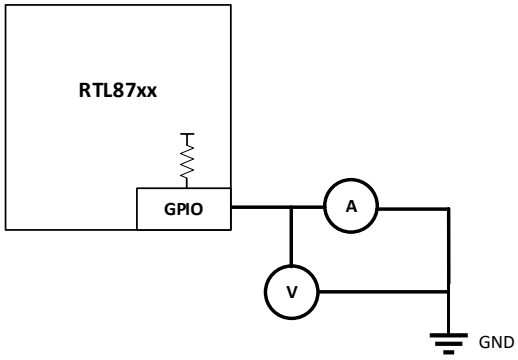


Figure 6-2 I/O Pull up resistor test

I/O pull-up resistor test procedure:
(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 1 for pull-up and 0 for pull-down (Table 6-3).
(3) For GPIOs with multiple pull-up resistance values, it is necessary to change the configuration of the register GPIO_BIT_PUPDC and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is V_1.
(5) According to Figure 6-2, only connect the ammeter to test. At this time, the current value is I_1, and the pull-up resistor is $R_{pu}=V_1/I_1$.

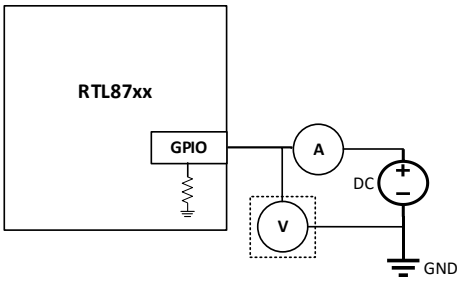


Figure 6-3 I/O Pull down resistor test

I/O pull-down resistor test procedure:
(1) Configure the GPIO to be tested as input mode.
(2) Configure the GPIO registers to be tested as 0 for pull-up and 1 for pull-down (Table 6-3).
(3) For GPIOs with multiple pull-down resistance values, it is necessary to change the configuration of the register GPIO_BIT_PUPDC and test them separately.
(4) When the ammeter is not connected, measure the voltage of the GPIO pin to be tested, and the voltage value is 0V.
(5) According to Figure 6-3, use an external power supply to provide the same voltage (V_2) as the GPIO power, and measure the current (I2) at this time, and the pull-up resistor is $R_{pd}=V_2/I_2$.

6.2.5 I/O Driving Strength

The I/O driving strength can be configured through GPIO_BIT_DRIVING_STRENGTH in the IOCTRL register. I/O driving strength is different between different I/O types.
GPIO output high driving strength test procedure:
(1) Configure the GPIO to be tested as output mode.

(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.85*VDDIO.
(3) Set the driving Strength to high or low through GPIO_BIT_DRIVING_STRENGTH.
(4) I_{HIGH} is the driving strength of GPIO output high.

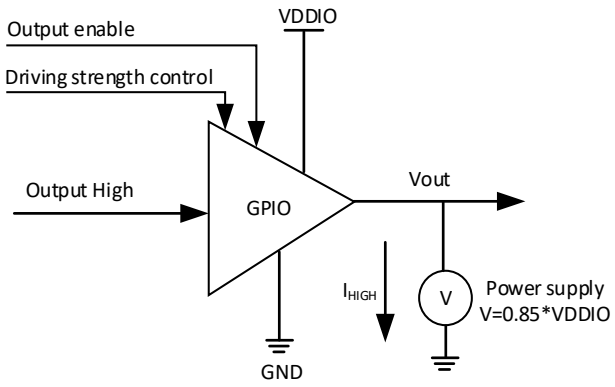


Figure 6-4 GPIO output high driving strength test

GPIO output low driving strength test procedure:
(1) Configure the GPIO to be tested as Output mode.
(2) Connect the power supply that can be poured back to the pin of the GPIO to be tested, and set the power supply voltage to 0.15*VDDIO.
(3) Set the driving Strength to high or low through GPIO_BIT_DRIVING_STRENGTH.
(4) I_{LOW} is the driving strength of GPIO output Low.

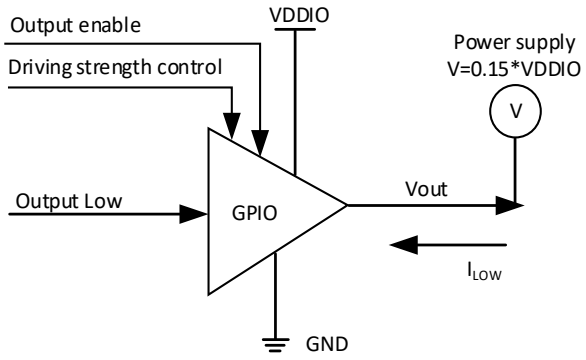


Figure 6-5 GPIO output low driving strength test

6.2.6 I/O Schmitt Trigger

The I/O pin contains a Schmitt trigger as a digital function, which can be selectively disabled by setting GPIO_BIT_SCHMITT_TRIGGER_EN in the IOCTRL register. Schmitt trigger is effective when GPIO is used as input function. The function of Schmitt trigger is to eliminate noise and jitter in the input signal and provide a stable output signal.
Figure 6-6 shows the pin voltage status seen by GPIO when Schmitt trigger is enable or disable when GPIO is in its input function. If the Schmitt trigger is disabled in IOCTRL register, VIH=VIL=0.5*VIO.

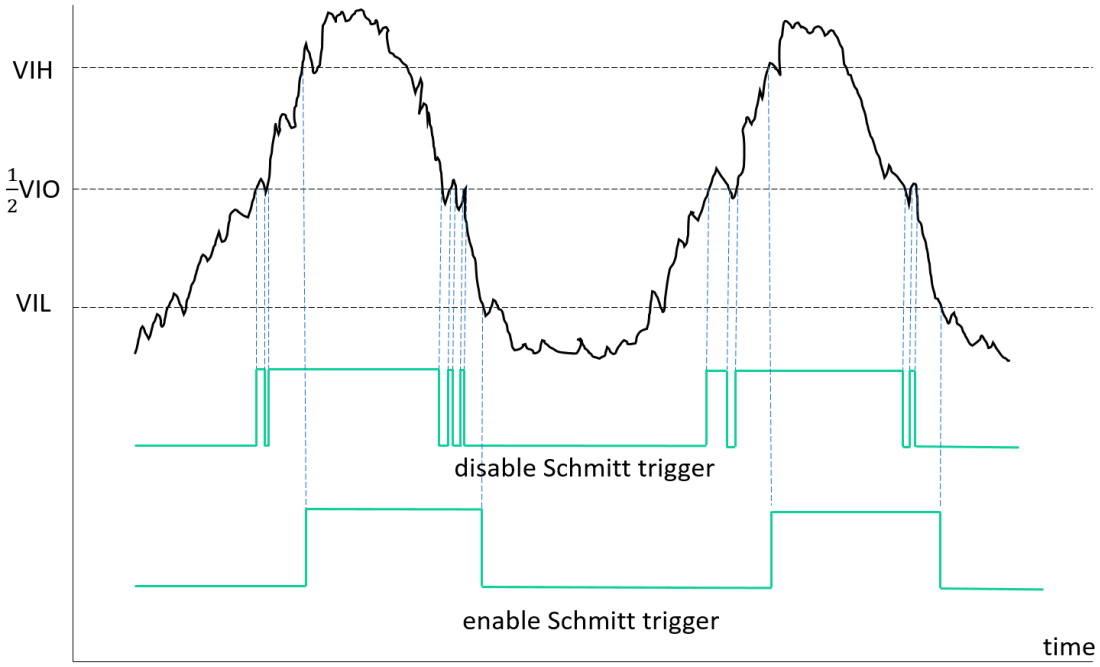


Figure 6-6 The voltage seen by GPIO when Schmitt trigger is enabled or disabled

The specifications of digital IO pin DC characteristics are shown in Table 6-4.

Table 6-4 Digital IO pin DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIL	IO input low level voltage	VIO=1.8V±10%	-0.3	-	0.35*VIO	V
		VIO =3.3V±10%	-0.3	-	0.8	
VIH	IO input high level voltage	VIO=1.8V±10%	0.65* VIO	-	-	
		VIO=3.3V±10%	2	-	-	
VOL	IO output Low level voltage	VIO=1.8V±10%,IOL Max	-	-	0.15*VIO	
		VIO=3.3V±10%,IOL Max	-	-	0.15*VIO	
VOH	IO output high level voltage	VIO=1.8V±10%,IOH Max	0.85*VIO	-	-	
		VIO=3.3V±10%,IOH Max	0.85*VIO	-	-	

NOTE

- *VIO is the power supply for IO pin.*
- *Refer to Table 6-1 for IO driving strength.*

6.2.7 I/O Shutdown & RESET

The power of I/O can be shut down through the GPIO_BIT_SHUT_DOWN bit in the IOCTRL register. You can use this function to conserve power.

For I/O shutdown, only when the whole group I/O shut down signals are all 1, the I/O SHDN will pull down to shut down the group I/O. Customer can also directly control the Group shutdown register and directly control the I/O shutdown of this group. For Specific information, please refer to the I/O SHDN&RSTB register table.

- When RSTB is set to 0, the I/O is in tri state. At this time, the level of the I/O is determined by the external pull-up and pull-down. If the external pull-down is connected, the I/O level is low. If the external pull-up is connected, the I/O level is high.
- When SHDN=1 and RSTB=1, the PU/PD state of the I/O is determined by register configuration.
- When RSTB=1, SHDN changes from 1 to 0, the state of I/O will latch the current state. At this time, the change of the I/O pull-up/pull-down register will not change the state of the I/O pull resistor.

Table 6-5 I/O SHDN&RSTB register

Address	Bit	Access	INI	Symbol	Description
0x4100C000	[25]	R/W	0	LPGPIO_RSTB	1: Release LP I/O RSTB33 (except group A) 0: Global Assert LP I/O RSTB33
	[24]	R/W	0	LPGPIO_SHDN	1: Global Enable LP I/O (except group A) 0: Shutdown LP I/O

					Note: Default value must be fixed after AON PMC done.
	[19]	R/W	1	GROUP_D_RSTB	1: Enable group D I/O 0: Reset I/O
	[18]	R/W	1	GROUP_C_RSTB	1: Enable group C I/O 0: Reset I/O
	[17]	R/W	1	GROUP_B_RSTB	1: Enable group B I/O 0: Reset I/O
	[16]	R/W	0	GROUP_A_RSTB	1: Enable group A I/O 0: Reset I/O
	[11]	R/W	1	GROUP_D_SHDN	1: Enable group D I/O 0: Shutdown I/O
	[10]	R/W	1	GROUP_C_SHDN	1: Enable group C I/O 0: Shutdown I/O
	[9]	R/W	1	GROUP_B_SHDN	1: Enable group B I/O 0: Shutdown I/O
	[8]	R/W	0	GROUP_A_SHDN	1: Enable group A I/O 0: Shutdown I/O

NOTE

- *GROUP A: PA0~PA1*
- *GROUP B: PA2~PA13*
- *GROUP C: PA14~PA22*
- *GROUP D: PA23~PA31 & PB0~PB10*
- *GROUP E: PB11~PB19*

6.2.8 Open Drain Mode

The I/O is default to push pull mode, and can be configured to implement open drain mode. For more details, refer to the software APIs.

6.3 I/O Pins Internal Pull Resistor Control Configuration

Each I/O has an Internal Pull-up and Pull-down Resistor. Please refer to section 6.2 for details. This section describes how to configure it. During the process of boot, sleep and deep-sleep, I/O pull control is needed, and the chip will load the I/O internal pull status of each I/O from the “pinmapcfg.c” file.

The correct configuration of pinmap can achieve low power consumption. Otherwise, the unsuitable configuration may lead to leakage.

Principles for I/O internal control configuration:

1. If the I/O is not used, it is recommended to set it to pull down.
2. If I/O is used as input, it cannot be left floating. please refer to the following chapters for configuration of different functions.
3. If I/O is used as output, please refer to the following chapters for configuration of different functions.

In the SDK, customers should set the internal pull status of I/O according to the above rules.

In the “pinmapcfg.c” file, PMAP_TypeDef pmap_func[] should be configured. In which,

- Pin Name: indicates the I/O.
- Func PU/PD: is used to configure the I/O internal pull status when the IC is in active mode.
- Slp PU/PD: is used to configure the I/O internal pull status when the IC is in sleep mode.

The following configuration is only applicable to RTK EVB, and customers need to configure it according to the external circuit.

```
const PMAP_TypeDef pmap_func[]=
{
//Pin Name      Func PU/PD              Slp PU/PD
{_PA_0,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_1,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_2,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PA_3,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PA_4,         GPIO_PuPd_UP,           GPIO_PuPd_UP},          //flash cs pin
{_PA_5,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PA_6,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_7,         GPIO_PuPd_UP,           GPIO_PuPd_UP},
{_PA_8,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_9,         GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_10,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_11,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
{_PA_12,        GPIO_PuPd_DOWN,         GPIO_PuPd_DOWN},
```

```
{_PA_13,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_14,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_15,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_16,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_17,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_18,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_19,        GPIO_PuPd_UP,       GPIO_PuPd_UP},      //log_RX need pull up
{_PA_20,        GPIO_PuPd_UP,       GPIO_PuPd_UP},      //log_TX sleep need pull up
{_PA_21,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_22,        GPIO_PuPd_NOPULL,   GPIO_PuPd_NOPULL},  //swr_vlotage_sel,for RTK EVB HW set:QFN68 PD,QFN48 PU
{_PA_23,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_24,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_25,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_26,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_27,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_28,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_29,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_30,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PA_31,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_0,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_1,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_2,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_3,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_4,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_5,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_6,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_7,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_8,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_9,         GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_10,        GPIO_PuPd_DOWN,     GPIO_PuPd_DOWN},
{_PB_11,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},    //PB11~PB19 audio pin
{_PB_12,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_13,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_14,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_15,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_16,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_17,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_18,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PB_19,        GPIO_PuPd_NOPULL,   GPIO_PuPd_DOWN},
{_PNC,          GPIO_PuPd_KEEP,     GPIO_PuPd_KEEP},    //table end
}
```

There are four states of the I/O.

- GPIO_PuPd_UP: Indicates that the I/O is through the internal resistor pulled up to VDDIO.
- GPIO_PuPd_DOWN: Indicates that the I/O is through the internal resistor pulled down to GND.
- GPIO_PuPd_NOPULL: Indicates that the I/O does not have an internal pull-up or pull-down configured.
- GPIO_PuPd_KEEP: Indicates that the I/O will maintain the last status.

The following section illustrates the recommendation of I/O status configurations according to the function of different pins.

6.3.1 Normal GPIO

When a pin is used as a normal GPIO connecting with external circuit, the GPIO PU/PD status depends on the state of the external circuit. If the GPIO is used to driver LED, and pin status is 'External pull up', the GPIO status need to be 'PULL UP' in sleep and DSLP mode. Configure the state of the internal PU/PD according to the GPIO external circuit.

Table 6-6 Normal GPIO status

I/O Type	Pin Status	active PU/PD	Sleep PU/PD
Input	External Pull UP	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP / GPIO_PuPd_NOPULL
Input	External Pull Down	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL
Input	Floating	GPIO_PuPd_DOWN	GPIO_PuPd_DOWN

Output	Output High	GPIO_PuPd_UP / GPIO_PuPd_NOPULL	GPIO_PuPd_UP
Output	Output Low	GPIO_PuPd_DOWN / GPIO_PuPd_NOPULL	GPIO_PuPd_DOWN

6.3.2 LOGUART Pin

The pins PA19 and PA20 are fixed to LOGUART function. The status is listed in Table 6-7.

Table 6-7 LOGUART IO status

Pin Function	Pin Name	Func PU/PD	Slp PU/PD
UART_LOG_RXD	PA19	GPIO_PuPd_UP	GPIO_PuPd_KEEP
UART_LOG_TXD	PA20	GPIO_PuPd_UP	GPIO_PuPd_KEEP

6.3.3 ADC & Cap-touch Pin

For PA28~PB5, if customer need to configure it for ADC or cap-touch function, customers need to configure IE to 0 first, and configured as internal no pull.

Table 6-8 GPIO IE Register Table

address	Bit	Access	INI	Symbol	Description
0x4100C9F8	[9:0]	R/W	3FFh	ADC/ Cap-Touch GPIO IE	PA28~PA31 & PB0-PB5 IE signals

If the customer needs to configure other functions, IE needs to be set to 1. For other configurations, please refer to 6.3.1.

6.3.4 SWD Pin

When a pin is configured as SWD function, the GPIO status is listed in Table 6-9.

Table 6-9 SWD IO status

Pin Function	Func PU/PD	Slp PU/PD
SWD_DATA	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SWD_CLK	GPIO_PuPd_UP	GPIO_PuPd_KEEP

If the SWD pin (PA21&PA22) needs to be used as a non-SWD function, in addition to switching the function id of the GPIO, the SWD function needs to be disabled.

Table 6-10 SWD pin function

address	Bit	Access	INI	Symbol	Description
0x4100C9F4	[3]	R/W	1h	KM4_SWD_SEL	select the share SWD signal to KM4 connection write the inverse value to take effect
	[0]	R/W	1h	SWD_PMUX_EN	1: Enable SWD pin (PA21&PA22) mux enable function 0: Disable

6.3.5 Flash Pin

When a pin is configured as SPI_FLASH function, the GPIO status are listed in Table 6-11.

Table 6-11 Flash pin IO status

Pin Function	Func PU/PD	Slp PU/PD
SPI_DATA_X	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CS	GPIO_PuPd_UP	GPIO_PuPd_KEEP
SPI_CLK	GPIO_PuPd_DOWN	GPIO_PuPd_KEEP

6.3.6 Audio Pin

1) The PB11~PB19 is used as the audio function by default.

2) If configured as audio function, the internal pull-up or pull-down function is invalid.
3) In deep-sleep mode, since VAM_AUD is powered off, PB11~PB19 are in floating state and the internal resistors of these pins are unavailable.

If the audio pin needs to be used as a non-audio functions, customers need to configure the audio pin IE to 1 first.

Table 6-12 Audio pin IE Register Table

address	Bit	Access	INI	Symbol	Description
0x4100C9D8	[8:0]	R/W	0h	Audio pin input enable	Audio share GPIO (PB11-PB19) input enable.

If audio pin needs to be used as a non-audio functions, audio operations need to be muted. The IO power of the audio pin is 1.8V. Refer to Table 6-13 for the process of audio pin mute, which is implemented by software API. Please refer to Chapter 8 for details.

Table 6-13 Mute configuration

Step	Mute control	Register configuration
1	Enable Function	Sets Register 0x4100C204 bit[22]=1'b1,bit[10]=1'b1
2	Enable clock	Sets Register 0x4100C20C bit[19]=1'b1
3	Clock selection	Sets Register 0x4100C218 bit[17] =1
4	Mute MIC	Sets Register 0x4102210C bit[17:14]=4'b1111, 41022110 bit[8] = 1'b1

6.4 I/O Pins Output Description

If customers need to use I/O to drive other devices, such as LEDs, they should first set the I/O to output 1 or 0, and then set the I/O to output mode. Because if you set the I/O to output mode without first setting output 1 or 0, the I/O will output 0 first, which may cause the LED light to flash due to the incorrect status of the I/O output.
After the system enters sleep mode (PG or CG), the status of the I/O output will maintain the status before sleep. For example, before sleep, the I/O is set to output 1. After the system enters PG or CG, this I/O will still remain output 1 unchanged.
However, if the system enters deep sleep, the status of the I/O output set under active will become invalid. For example, if the I/O in active is set to output 1, and the system enters deep sleep, the I/O will not be able to maintain the output 1 state.

7 PINMUX Instructions

7.1 Introduction

RTL8713E and RTL8710E provides a PINMUX circuit to maximize the user's freedom of use under limited pin-out conditions. Each pin can be connected to different internal IP circuits through configuration. For the specific correspondence between each pin and IP circuit, refer to the provided PINMUX document.
Before users apply the chip for further development, please read the following precautions about PINMUX to avoid inconvenience due to unexpected behavior.

7.2 Trap Pins

When user power on the chip, the internal circuit will latch several pins conditions to decide whether enter into different mode. The trap pins and their descriptions are as below.

Table 7-1 Trap pin description and precautions

Pin name	Trap pin name	Descriptions	Note
PA1	TM_DIS	Enter test mode during power on procedure. (Internal use)	Please make sure that the pin is in the pull-up state during normal use. 1: Normal mode 0: Test mode
PA20	UD_DIS	Enter flash download mode during power on procedure.	Download flash content in this mode through LOGUART. 1: Normal mode, 0: UART download mode.
PA22	PSO_SEL	Select SWR_CORE output voltage level	SWR_CORE output voltage correspondence. 1:1.25V, 0:0.9V.

NOTE

The Trap pin needs to select the external pull-up and pull-down voltages according to the IO power supply.

7.3 Wake Pins

PA0 and PA1 are directly connected to the wake up circuit which is used to wake up system from deep-sleep state. When users need to use other functions on this pin, please disable the wake up function.

7.4 Function Mux

7.4.1 Function ID 0-19

For functions whose ID number among 0-19, each pin can only be connected to a fixed signal of a certain IP. The functions that can be configured on each pin are very limited, but a dedicated design can maximize the performance of each IP.

NOTE

For example, function id 6 and function id 32-35 are both SPI functions. Since function id 6 is a dedicated pin, the maximum speed of the SPI function reaches 50MHz (Master mode) and the maximum speed of the pins (full-cross pins) corresponding to function id 32-35 is only 12.5 MHz (Master mode).

Take PA0 as an example. If users configure function ID of PA0 to 1, then the pin will be directly connected to the UART1_TXD signal of the UART1 IP via PINMUX. Please refer to the PINMUX document for the specific function distribution available on each pin.

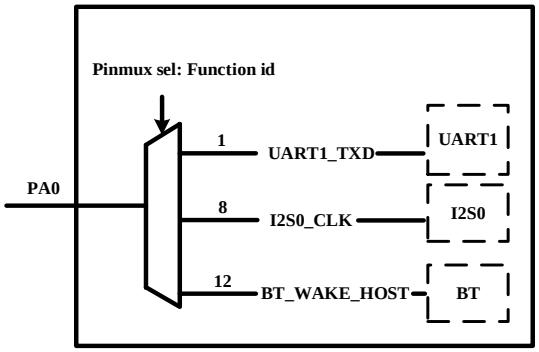


Figure 7-1 Schematic diagram of PINMUX connection of PA0

7.4.2 Function ID 20-67

For functions whose ID number is after 20, each pin can be connected to different signals of a certain IP. This method maximizes the freedom of use, but the scope of use and some IPs' performance (max transfer speed) is limited.

NOTE

These function IDs can only be configured in PA8-PA31 and PB0-PB10.

Take PA8 as an example. According to the PINMUX document, users can connect PA8 with the UART0_TXD signal of UART0 by configuring the PA8 function ID as 20. Users can also configure the PA8 function ID as 21, and connect PA8 with the UART0_RXD signal of UART0. For details, please refer to the PINMUX documents.

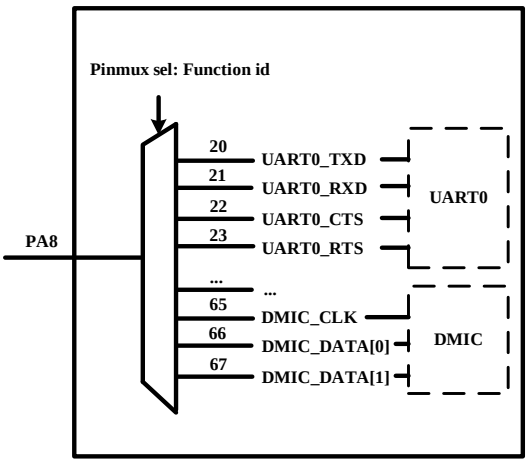


Figure 7-2 Schematic diagram of PINMUX connection of PA8

7.5 Audio Function

For RTL8713E, if users use PB11-PB19 as audio function and digital function simultaneously, it's necessary to pay attention to the layout of digital function as far as possible from the trace of audio function to avoid interference.

7.6 PINMUX Signal Descriptions

For all signal descriptions, please refer to PIMUX documentation for details.

8 Audio

Chapters 13.1 to 13.5 are only valid for RTL8713E.

8.1 Line-out

Line-out supports differential output mode. Users can select the mode by setting the related registers.
In line-out differential mode, both N-end and P-end drive the available analog audio signal. This application is mainly used to provide clean audio for external power amplifiers (Class-AB/Class-D).

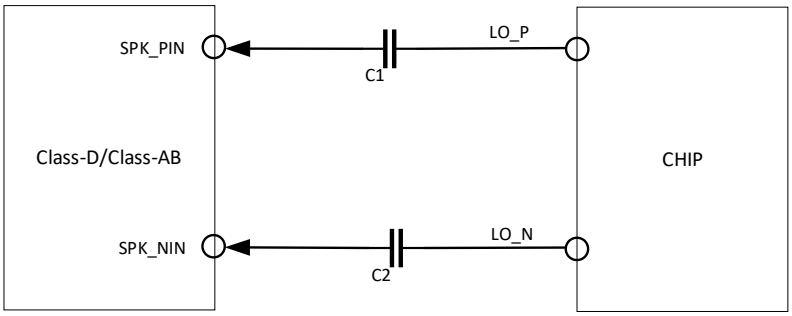


Figure 8-1 Differential mode connection with audio power amplifiers

8.2 Line-in

Line-in has 0dB gain preamplifier, its input signal often has a large output power. It often connects to the audio output of equipment such as electric guitar, electronic organ, and synthesizer.
Connect the left channel of line-in signal to MICx_L, and the right channel to MICx_R accordingly.
In order to obtain good low-frequency recording performance, it is recommended that capacitor C1 /C2 be at least 0.47uF

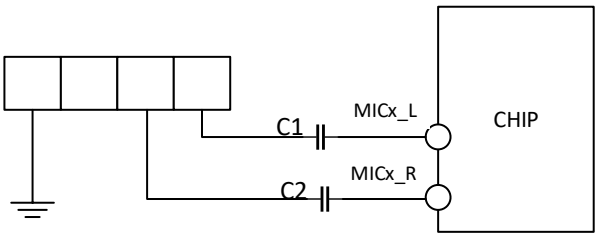


Figure 8-2 Line-in mode connection

8.3 AMIC-in

The amplitude of the signal collected by analog microphone (AMIC-in) is very small, a preamplifier is necessary, AMIC-in supports differential mode and single-ended mode.

8.3.1 AMIC-in Single-ended Mode

Connect MICx_P with a single-ended analog microphone, while MICBIAS provides the microphone bias voltage.
In order to obtain good low-frequency recording performance, it is recommended that capacitor C1 be at least 0.47uF

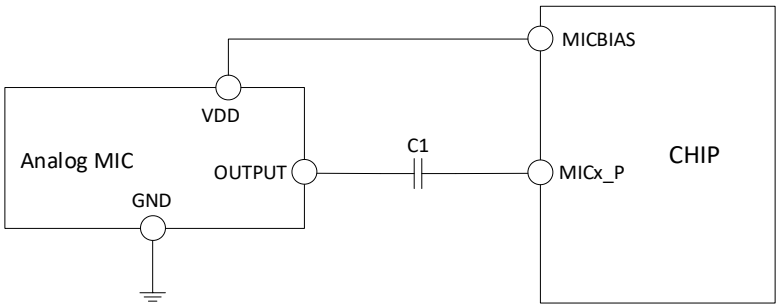


Figure 8-3 AMIC-in single-ended mode connection

8.3.2 AMIC-in Differential Mode

Connect MICx_P/MICx_N with a differential analog microphone, while MICBIAS provides the microphone bias voltage.
In order to obtain good low-frequency recording performance, it is recommended that capacitor C1 /C2 be at least 0.47uF

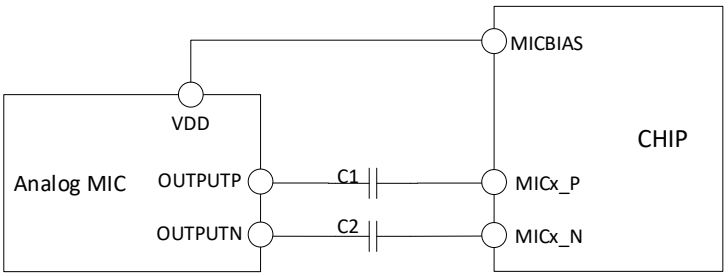


Figure 8-4 AMIC-in differential mode connection

8.4 Microphone Array

In a two-microphone smart voice application, two ADCs are used to collect the speaker's voice, and one ADC is used to collect the reference sound of echo cancellation.

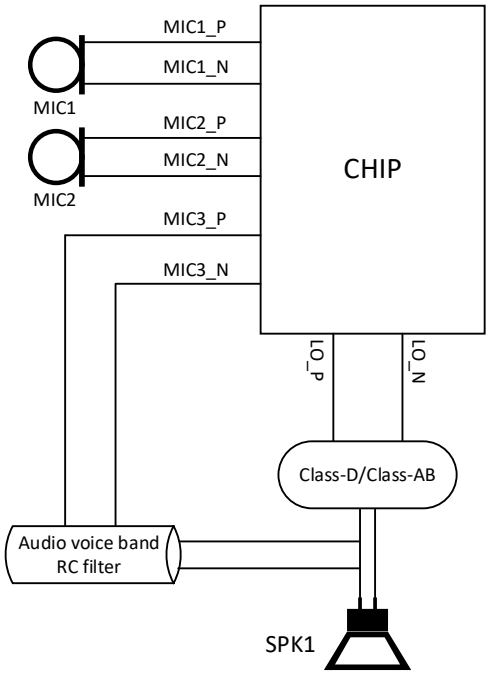


Figure 8-5 Two-microphone smart voice application

8.5 Audio Pad

Audio Pad can be used as digital path or analog path, and Audio pad share status can be changed by the interface:

```
APAD_InputCtrl(u8 PinName, u32 NewState)
```

- ENABLE: enable digital path
- DISABLE: disable digital path

8.5.1 LINEOUT Pad

If LO_P/LO_N pad (PB16 & PB17) are used as digital I/O functions, LINEOUT should be powered down.
When audio playback is running , LINEOUT will be powered on. Users can call the following interface to power down LINEOUT.

```
AUDIO_CODEC_SetLineOutPowerMode (u32 channel, u32 powermode)
```

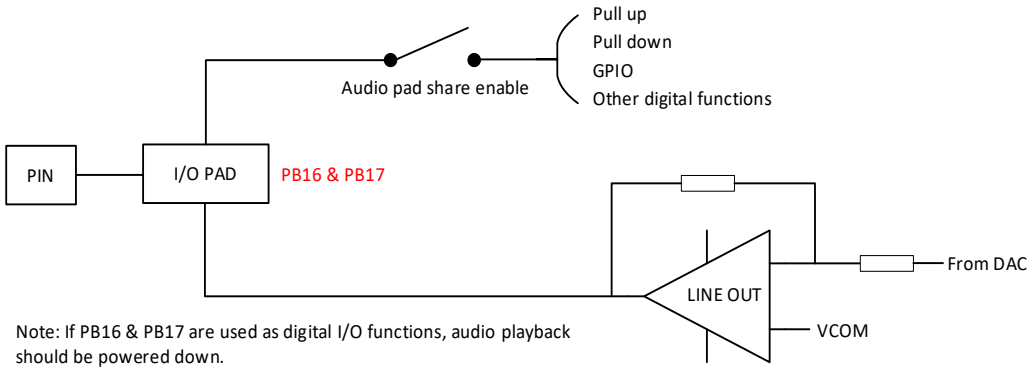


Figure 8-6 AOUT pad

8.5.2 MIC_BIAS Pad

If MIC_BIAS pad (PB15) is used as digital I/O function, MIC_BIAS should be powered down.
When audio record is running , MIC_BIAS will be powered on. Users can call the following interface to power down MIC_BIAS.

```
AUDIO_CODEC_SetMicBiasPowerMode(u32 powermode)
```

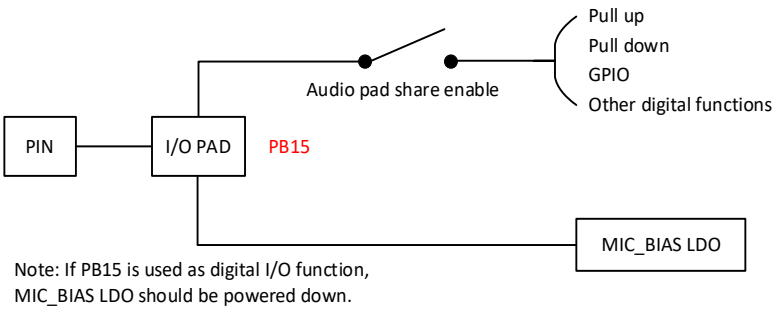


Figure 8-7 MIC_BIAS pad

8.5.3 MIC Pad

If MIC pad (PB11~PB14, PB18~PB19) are used as digital I/O functions, MICBST should be mute.
When audio record is running, MICBST will be unmute. Users can call the following interface to mute MICBST.

```
AUDIO_CODEC_SetMicBstChnMute(u32 amic_sel, u32 type, u32 newstate)
```

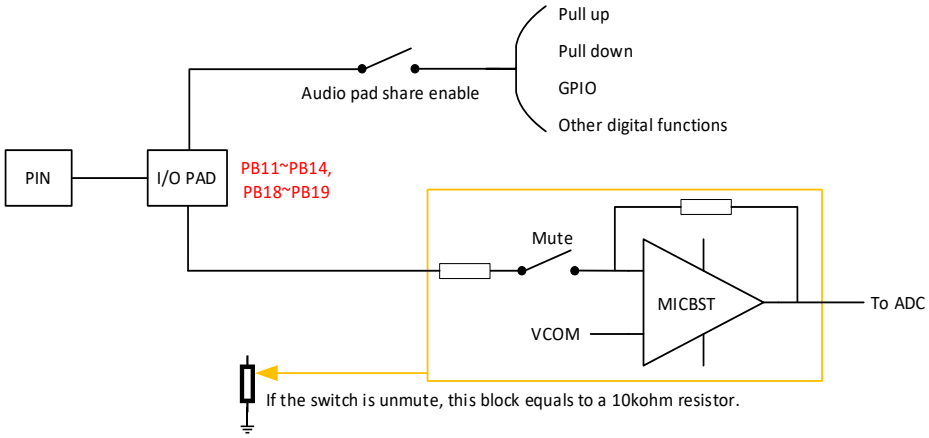


Figure 8-8 MIC pad

8.6 DMIC-in

Digital microphone (DMIC) records audio data. It is integrated with ADC internal, and can directly output digital signal. DMIC-in supports mono mode and stereo mode.

8.6.1 DMIC-in Mono Mode

Tie the L/R of a digital microphone to ground or VDD if only one digital microphone is placed.

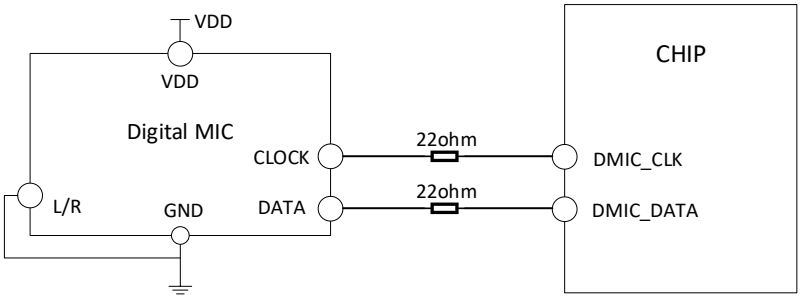


Figure 8-9 DMIC-in mono mode connection

For layout design, DMIC_CLK and DMIC_DATA should add ground isolation on both sides of the routing.

Figure 8-10 DMIC-in layout

8.6.2 DMIC-in Stereo Mode

Tie the L/R of two digital microphones to ground and VDD respectively if a stereo microphone is needed. The two microphones share the DMIC_DATA according to the rising/falling edge. DMIC_CLK and DMIC_DATA layout design refer to Figure 8-10.

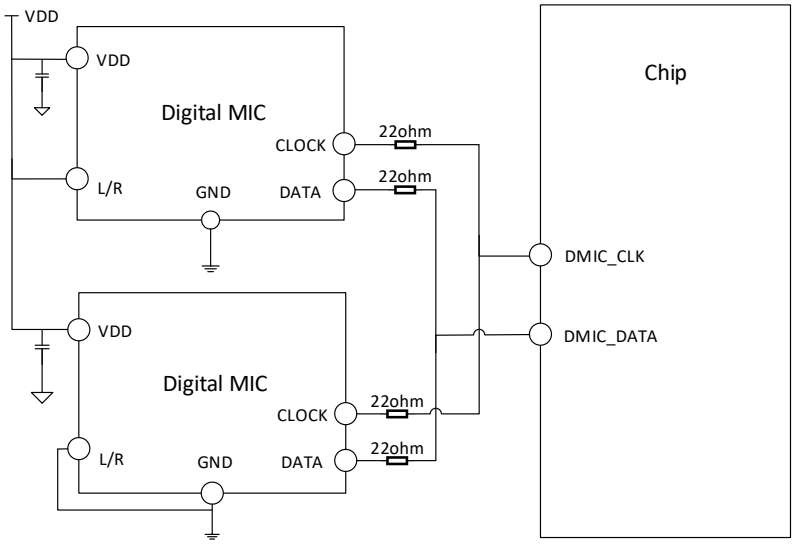


Figure 8-11 DMIC-in stereo mode connection

8.7 I2S layout

Reserve 22ohm resistors on the clock and data paths of I2S. If the layout space allows, increase ground isolation for clock and data as much as possible.

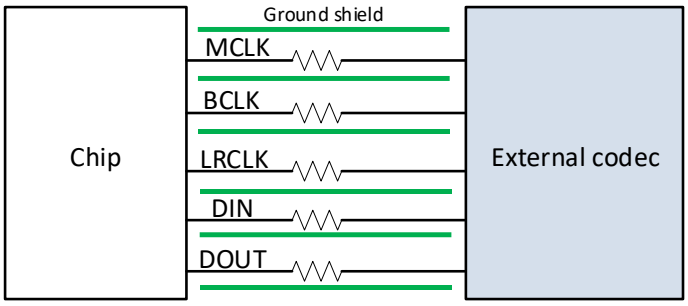


Figure 8-12 I2S layout

8.8 ECM AMIC-in

The ECM (electret microphone) AMIC-in connection of audio codec is illustrated in Figure 8-13 AMIC-in connection. The capacitor between analog microphone and IC should be 0.47uF. A larger capacitance value makes a longer period needed for capacitor charging.

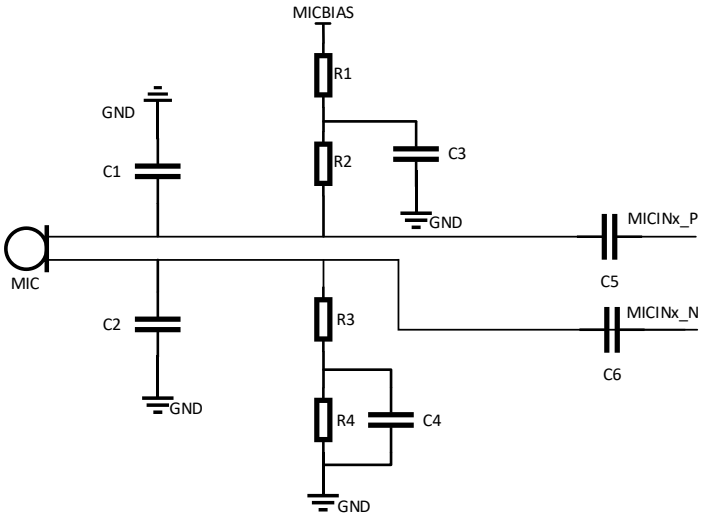


Figure 8-13 AMIC-in connection

MICBIAS connects to the positive side of microphone through R1/R2/R3/R4 resistors to offer bias voltage.

- Connect the negative side of microphone to MICN through a 0.47uF capacitor at differential mode.
- The value of the capacitor C5/C6 can be selected larger, in order to obtain a lower frequency audio signal. Fc=1/2*pi*5K*C5
- R4/C4 and R1/C3 are two low pass filter and are used to suppress noise on the power supply and ground. The values of these components need to be determined after actually testing the circuit board

8.9 AEC reference circuit

The following reference circuit is used in the intelligent voice application circuit. SPK_P/N is the output circuit of the power amplifier, and MICINx_P/N is the microphone amplifier input.

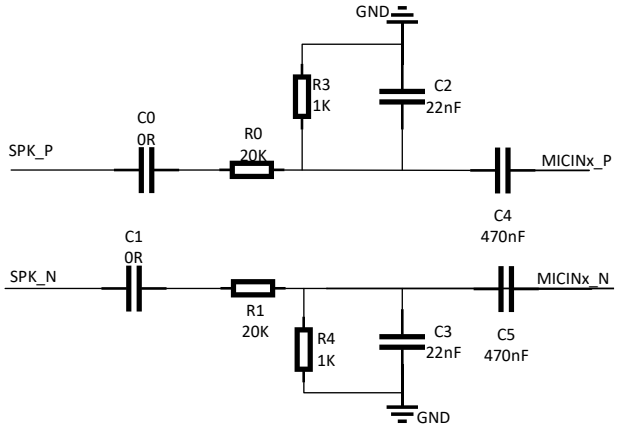


Figure 8-14 AEC reference circuit

- Vaec is AEC reference circuit output,Vspk is AEC reference circuit input，Vaec=Vspk*R3/(R0+R3)
- R0/R3/C2 are low pass filter,-3dB Cut-off Frequency:f=1/2π（R0//R3）C2
- C0/C1 select 0.1uF for low power application
- The capacitance value of C4/C5 can be modified. This capacitance forms a high-pass filter with the 10Kohm input impedance of the MICIN amplifier. The cut-off frequency Fc=1/2*pi*10K*C
- R0/R3 is a voltage divider circuit. Its value can be adjusted according to the maximum output amplitude of the power amplifier and the maximum allowable input amplitude of MICIN (1.5vpp). The corresponding C2 should also be adjusted based on the cut-off frequency in f=1/2π（R0//R3）C2. The adjustment method of R1/R4/C3 is the same

8.10 Intelligent voice application suggestions

8.10.1 Microphone unit performance requirements

- MIC recommends that silicon microphones are preferred for better consistency.
- MIC recommends the following parameters:
  - Sensitivity: analog silicon microphone -38dBV ~ -42dBV/±1.5dBV;
  - Signal-to-noise ratio (SNR): ≥60dB
  - Total harmonic distortion (THD): ≤ 1% (1kHz)
  - Acoustic overload point (AOP): ≥120dB SPL
  - Free field spectrum (within 100-10kHz) response fluctuation < 3dB

8.10.2 Speaker performance requirements

Choose speakers with low harmonic distortion.
Recommendation: 100 ~ 200Hz THD≤5% at rated power, 200 ~ 8000Hz THD≤3%

8.10.3 Structural design suggestions

- When designing the speaker cavity, avoid abnormal sound and vibration caused by structural resonance. When the speaker cavity is installed in the whole machine, it must be treated with shock absorption. The cavity must be at least 2mm away from other components, and the speaker diaphragm, passive diaphragm and other components must be at least 5mm away.
- It is recommended that the speaker and microphone be placed in different cavities, and the cavities are sealed with good performance sealing materials to prevent crosstalk inside the structure.
- MIC must be internally soundproofed with the SPK sound cavity to prevent the sound emitted by SPK from being directly transmitted to the MIC through the internal space of the machine. Silicone is generally used for sound insulation and shock absorption. The hardness of silicone needs to be designed according to the actual structure and the compression amount. Generally, it is required to be as soft as possible. MIC should be away from interference (exhaust fan) or vibration (speaker vibration, structural vibration) to avoid structural vibration causing a greater impact on MIC.
- For electret microphones, the protection of the microphone should be considered during the structural design and production process to avoid the loss of microphone consistency caused by extrusion. The microphone needs to be isolated from the solid surface by a silicone cover to reduce the vibration and sound transmission of the shell and to seal it.

The air tightness and distortion test methods of the speaker can be obtained from RTK after the machine is installed.

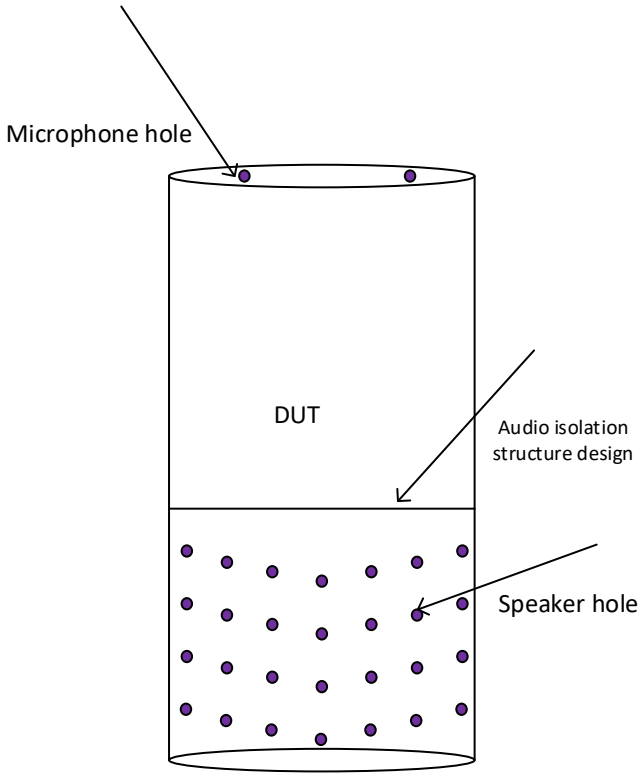


Figure 8-15 Speaker structure design reference diagram

8.10.4 Machine audio test method

The airtightness test audio document is as follows， password is RTK

https://drive.google.com/file/d/1GWCvCMDbhgdsBnC-_mbdv-CpNqg87NyR/view?usp=sharing

- External airtightness test process

1. Use an external speaker to play white noise at an appropriate volume, and use the microphone on the DUT to record. Record the state where the clay does not plug the microphone hole and the state where the microphone hole is plugged. The audio energy recorded in the two states must differ by more than 15dB.

- Internal airtightness test:

Use the DUT speaker to play white noise at the maximum volume, and use the microphone on the DUT to record. Record the state where the clay does not plug the microphone hole and the state where the microphone hole is plugged. The audio energy recorded in the two states must differ by more than 15dB.

- Confirmation of speaker distortion:

Use the speaker on the DUT to play the swept frequency audio, and use the microphone on the DUT to record. The distortion of the recording file must meet the following requirements: 100 ~ 200Hz THD≤5% at rated power, 200 ~ 8000Hz THD≤3%

Sweep frequency audio file path， password is RTK

https://drive.google.com/file/d/1NyBgWgtf87HBCK5eW3rjHei0r04xcFzX/view?usp=sharing

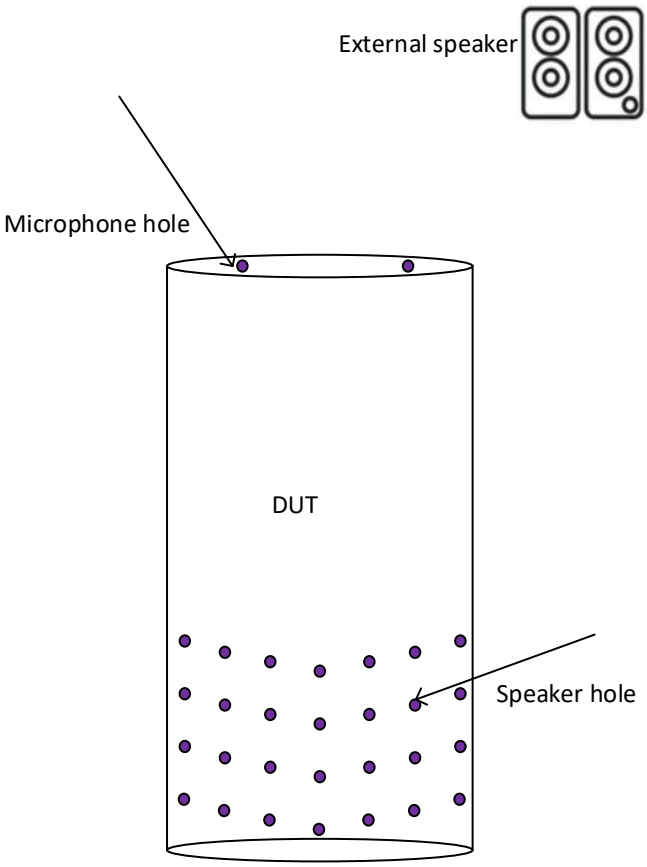


Figure 8-16 test scenario

9 General purpose ADC

The General purpose ADC (GP-ADC) and Capacitive Touch Sensor multiplexes pin. The signal sampling of Capacitive Touch Sensor itself is also done through GP-ADC, and both of them are sensitive analog signal sensors, so we need to pay special attention to interference.

9.1 Net arrangement

GP-ADC has multiple channels that use a set of fixed pins of IC. Care should be taken to avoid using GPIO in the same group of GP-ADC as high-speed signal ports (I2C, SPI, etc.), as shown in Figure 9-1. If unavoidable, it is necessary to set it reasonably on the software to ensure that the high-speed signal has no action while GP-ADC sampling.

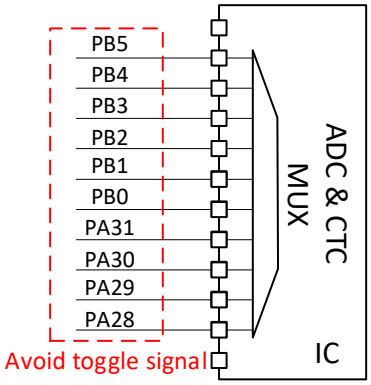


Figure 9-1 GP-ADC net arrangement

In addition, even if the high-speed signal is not arranged in the same set of the GP-ADC GPIO, it should not be arranged adjacent to the pin of the GP-ADC.

9.2 Input impedance

In order to measure the voltage of 0 to 3.3V, a voltage divider is added to the front end of the GP-ADC. The resistance is fixed and cannot be modified, and the accurate resistance value can be obtained by reading the calibration value written in each IC.
Due to the divider resistor, the input resistance of the GP-ADC will be affected by it, and the typical value is 491kohm. It is necessary to pay attention to this situation in application. Take as an example, when the external resistance R2 of GP-ADC is about equal to the internal resistance R, there will be a deviation in the voltage collected by GP-ADC. If R2 is a thermistor, the temperature measurement may be inaccurate.
Therefore, when designing the external circuits, we should consider:
1) R2 should be sufficiently small (less than 1 / 100 of R) to minimize the impact of internal resistance.
2) If the requirements (1) cannot be met, the Rin value of the IC can be obtained through the API and incorporated into the circuit design.
Typically GP-ADC normal channel are used to measure the voltage of different sensor, such as NTC thermistor. The simplified block is as follows:

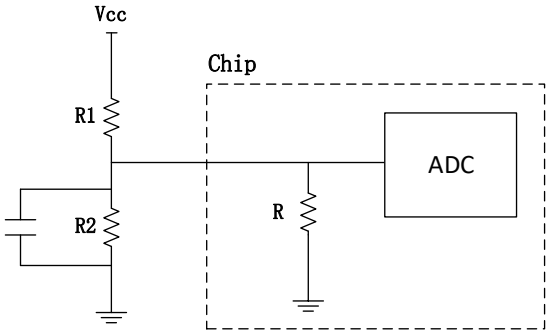


Figure 9-2 simplified application block

There is a 500 kohm resistor to ground inside the chip which will affect the accuracy of GP-ADC with the combination of peripheral circuit. The ideal input voltage to GP-ADC is:

$$V_{\text{ideal}} = V_{\text{cc}} \times R_2 / (R_1 + R_2) = 3.3 \times \frac{R_2}{R_1 + R_2}$$

But the actual input voltage to GP-ADC is:

$$V_{\text{actual}} = V_{\text{cc}} \times \frac{R_2 // R}{R_2 // R + R1} = V_{cc} \times \frac{R_2}{R_2 + R_1 \times R_2 / R + R_1}$$

Compare the two formals, Vactual is smaller than Videal due to the impact of internal R. And the greater the ratio of R1xR2/R is, the greater the error between Vactual and Videal is. What's more, the resistance of internal R vary differently in multi chips which also can impact the accuracy.
For better accuracy, internal R should be calculated and its resistance value will be stored in OTP.
After calibration, if R2 is NTC thermistor, the actual resistance of R2 is:

$$R_2 = \frac{R_1 \times V_{\text{adc}}}{V_{cc} - V_{adc} - V_{adc} \times \frac{R_1}{R}}$$

By the way, it's optional for customers to choose another GP-ADC channel to measure the voltage of Vcc, which can reduce the impact that Vcc changes while GP-ADC Vref doesn't change:

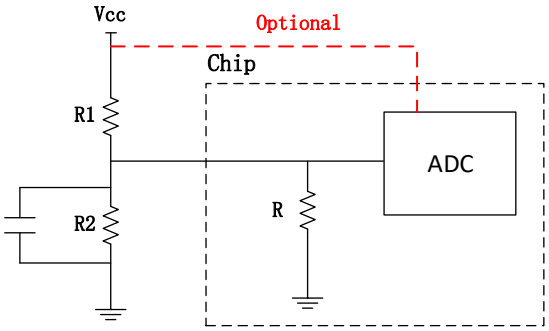


Figure 9-3 Optional application block

R will be connected to the circuit only when the GP-ADC is sampling. Therefore, at the moment when the ADC sampling is turned on, the circuit will be switched, and the parallel C of R2 may slow the transient process of the circuit. There are usually two ways to solve this problem:

1. When the requirement for sampling rate is not high, it can be sampled at intervals, and the interval time needs to exceed the circuit time constant. In this case, the instantaneous value of sampling is the voltage at the beginning of switching, that is, the voltage of the capacitor C. in this case, the circuit design requires that C be greater than 10nF.
2. when the sampling rate is strict and interval sampling is not acceptable, a delay can be added before each sampling of a group of data, which should be greater than 5 times the circuit time constant, and pay attention to clear the conversion result FIFO before reading the data.

9.3 ADC Calibration Principle

To improve the linearity of the input / output characteristics of the ADC, each IC will implement a nonlinear calibration of the ADC in the factory. With the nonlinear calibration, the gain and offset error of the ADC can also be reduced.The user can use the API to directly obtain the exact voltage conversion results that have been calibrated.

After calibration, each IC can find its own value of A, B and C and store them in one time program (OTP). The A and C are stored in the form of binary complement, while B is stored as an unsigned integer. When acquiring ADC code, use the following formula to get the current voltage with unit as mV, here parameter x is ADC code:

$$y = ax^2 + bx + c = \left(\frac{A}{2^{26}}\right)x^2 + \left(\frac{B}{2^{15}}\right)x + \left(\frac{C}{2^{6}}\right)$$

For example, if A, B, and C read from OTP are 0xff66, 0x6f91, and 0x53f, and ADC code is 1800. The original A is 0x809a, parameter a = -(0x9A)/2^26, parameter b = (0x6f91)/2^15, and parameter c = (0x53f)/2^6. So, the current voltage y = 1582mV.

Users can obtain the calibrated results directly through API: ADC_GetVoltage.

10 Capacitive Touch Sensor

10.1 Net arrangement

- It is not recommended to reuse Capacitive Touch Sensor pins with other functions. High-speed signal lines (I2C, SPI, etc.) should not appear in the same group of Capacitive Touch Sensor pins. If unavoidable, it needs to be set reasonably on the software to ensure that Capacitive Touch Sensor works with no high-speed signal action
- It is suggested to keep the Capacitive Touch Sensor away from high speed signal and switching power net
- To prevent crosstalk, if only some Capacitive Touch Sensor channels are used, select channels at intervals and disable unselected channels
- Do not design a pull-up or pull-down voltage on the signal line
- Do not design bypass capacitors on the signal line

NOTE

Capacitive Touch Sensor's layout has a great impact on performance. For specific layout rules, please refer to layout guide.

10.2 Series resistance

A resistor is connected in series in each Capacitive Touch Sensor channel (placed near the chip). This resistor and the parasitic capacitance on the signal path form a simple RC filter, which can partially filter out the noise interference and improve the ESD resistance. Due to the different circuit design, the resistance usually can not be accurately selected. The filter effect is poor when the resistance is too small, and the sensitivity is reduced because the resistance is too large. It is recommended to choose a resistance of 47-560 ohms.

In addition to using series resistance to improve ESD resistance, the TVS of each sensor channel should be connected in parallel to attenuate the impact of surge current on the sensor, but the junction capacitor of this TVS should not exceed 0.6 pF.

10.3 Button LED Design

When the button is made into a hollowed-out type, a LED can be added in the middle, and the light and darkness of the LED can be used to judge the situation of touching and leaving the finger. It is suggested that the power supply of LED should add RC filter to slow down the change rate of the level edge.

10.4 Max input Voltage

The Capacitive Touch Sensor is an analog circuit, an ADC sample the input net continuously. The max input voltage of the input net is 0.85V. In particular, the use of too large Mbias can cause a charging voltage exceeding 0.85V, which may cause damage to the ADC.

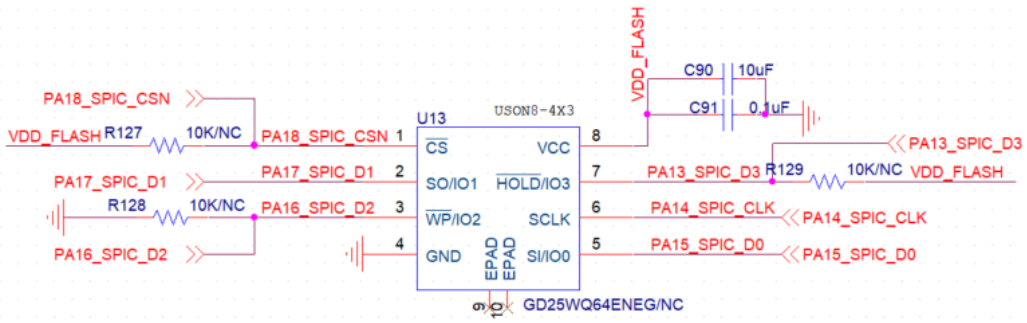
11 Flash SPI

11.1 Flash selection requirements

- Specific part numbers of RTL8710E and RTL8713E need external flash. All the other part numbers including RTL8710E and RTL8713E have embedded NOR flash.
- Flash SPI in RTL8710E and RTL8713E can only operate in typical 3.3V. Users need to select flash with adaptive operating voltage range.
- The compatible flash can be found in Flash AVL. If the expected flash to be used is not in AVL, please contact RTK for more information.
- Flash SPI can only be configured as master with Max. clock frequency: 100MHz.

11.2 Schematic reference design

- Suggest CS pin reserving an pull up 10K resistor so that the CS pin has a certain high level state to avoid bus floating. . If internal pull-up is configured, the external pull-up resistance can be NC.
- For dual SPI and standard SPI mode，suggest WS pin and Hold pin reserving an pull up 10K resistor so that the WS pin has a certain high level state to avoid bus floating. If internal pull-up is configured, the external pull-up resistance can be NC.
- Vcc requires a filtering capacitor connected to ground, usually one large and one small capacitor connected in parallel, such as 10μF and 0.1μF.



12 I2C

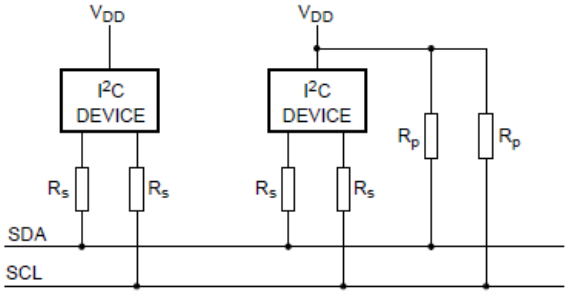
12.1 Schematic reference design

- Part of the pads used for I2C can switch to 4.7K pull-up resistor internally (PA19~PA27, PA30, PA31, PB0~PB12). However, the internal pull-up resistance value of other pads is too large and not suitable for I2C communication. Suggest users to reserve pull-up resistors externally to adjust the resistance value according to their own needs.
- Different speed modes have requirements for the maximum allowable load of the I2C bus. In standard , fast and 1.7M high speed modes, the bus load cannot exceed 400pF, and in 3.4M high speed mode, the bus load cannot exceed 100pF.

- Calculation method for pull-up resistance of I2C bus:
  The voltage value of IO Power determines the minimum value of pull-up resistance. When IO Power is 3.3V, the minimum allowable value of pull-up resistance is 1K, and when IO power is 1.8V, the minimum allowable value of pull-up resistance is 0.5k. The size of the bus load determines the maximum allowable pull-up resistance, and the calculation formula is as follows:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

  In the formula, t_r represents the maximum signal rise time allowed under different speed modes (Standard: 1000ns, Fast: 300ns, High Speed: 80ns), and C_b represents the bus load.
- The I2C protocol also defines resistors Rs connected in series on SDA and SCL lines. The function of this resistor is to effectively suppress interference pulses on the bus from entering the slave device and improve reliability. The selection of this resistor is generally around 100~200 Ω. This resistor is not necessary and can be used in harsh noise environments.



13 General SPI

13.1 Introduction

- The chip supports Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol.
- Master or slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps

NOTE

1. When the chip is configured as Master, SPI supports transmission with a maximum baud rate of 50Mbps. But when the chip is configured as Slave, whether it can support a maximum baud rate of 50Mbps is controlled by the connected master. Due to the path delay and pad delay of internal signals in the master and slave devices, as well as some delays that may be introduced by pads or PCBs, the connected master needs to support delayed sampling function in order to correctly receive data sent by the slave at 50Mbps baud rate.

2. Dedicated SPI does not allow cross group use.

13.2 Schematic reference design

- Generally, four signal wires (CS, CLK, MISO, and MOSI) can be directly connected to external device.
- Users can pull CS pin up to Vcc by a 10K resistor, so that the CS pin has a certain high level state to avoid bus floating.
- Users also can place resistors connected in series on four signal lines to reduce signal reflection. User can choose the resistance value based on actual usage scenarios, and it is recommended to use around 27R resistors.

14 SWD

14.1 Introduction

Debug Interface supports Arm® standard bi-directional Serial Wire Debug (SWD) to pass data to and from the debugger and the target system in a highly efficient and standard way. It provides a probe interface consisting of two signals—TCK and TMS. The TMS signal is bidirectional and carries control information to the adapter and data in both directions. The TCK signal (max baud rate: 20MHz) is sourced from the probe.

14.2 Schematic reference design

- Suggest ground shielding between SWDCLK and SWDIO signal traces to avoid signal crosstalk.
- It is recommended to connect a 22R damping resistor in series at the source of both SWDIO and SWDCLK signals to suppress signal reflection.
- It is recommended to connect one ESD protection device in parallel on each of the SWDIO and SWDCLK signal traces, as manual hot swapping is required during debugging.
- According to the SWD standard, it is recommended to configure the SWD data pad to pull-up state after power on.

NOTE

Port PB0 and port PB1 are default configured as SWD interface but users can configure relevant register to switch these two ports to other functions. If users use PB0 and PB1 for other functions except SWD and connect the two ports to external circuits, users must avoid SWD toggle behavior with a risk of misidentification before switching off the SWD function from the two ports.

15 Revision History

Date	Version	Description
2024-04-30	R00	Initial release
2024-06-17	R01	Modify the content of Chapter 6.
2024-06-20	R02	Modify the content of Chapter 6 and Chapter 8.
2025-08-05	R03	Add chapter 8.8/8.9/8.10